MPM3632C

18V Input, 3A Module, Synchronous, Forced CCM, Step-Down Converter with Integrated Inductor

The Future of Analog IC Technology

DESCRIPTION

The MPM3632C is a step-down, regulator module integrated with a synchronous, rectifying power MOSFET, inductor, and three capacitors. The MPM3632C offers a very compact solution that requires only input and output capacitors to achieve 3A of continuous output current with excellent load and line regulation over a wide input range. The MPM3632C operates at a fixed 3MHz switching frequency and employs constant-on-time (COT) control, which provides a fast load transient response.

The MPM3632C eliminates design and manufacturing risks while improving the time to market dramatically.

Full protection features include output over-voltage protection (OVP), over-current protection (OCP), and thermal shutdown.

The MPM3632C is available in a space-saving QFN-20 (3mmx5mmx1.6mm) package.

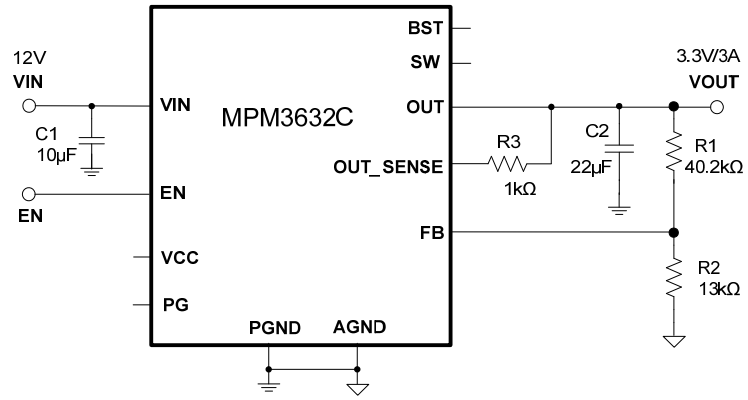
FEATURES

- Complete Switch-Mode Power Supply
- 3MHz Switching Frequency
- Wide 4V to 18V Operating Input Range
- Output Adjustable from 0.8V
- Internal Fixed Soft-Start Time
- 3A Continuous Output Current
- Forced CCM for Low Output Ripple
- Power Good (PG) Indicator
- Hiccup Over-Current Protection (OCP)
- Output Over-Voltage Protection (OVP)
- Thermal Shutdown
- Fast Transient Response
- Available in a QFN-20 (3mmx5mmx1.6mm) Package
- Total Solution Size: 7mmx7.9mm

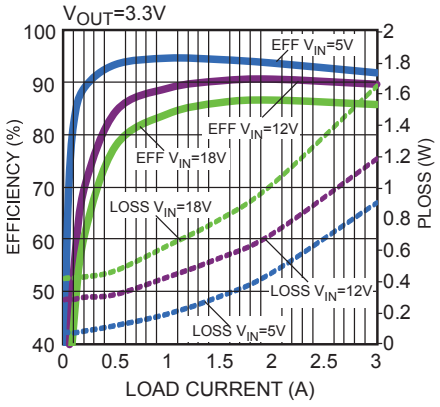
APPLICATIONS

- Server Systems
- Medical and Imaging Equipment
- Distributed Power Systems
- Point-of-Load for FPGA, ASICs, DSPs
- Space-Constrained Applications

TYPICAL APPLICATION



Efficiency &Ploss vs. Load Current



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MPM3632CGQV-UC	QFN-20 (3mmx5mmx1.6mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g.: MPM3632CGQV–UC-Z).

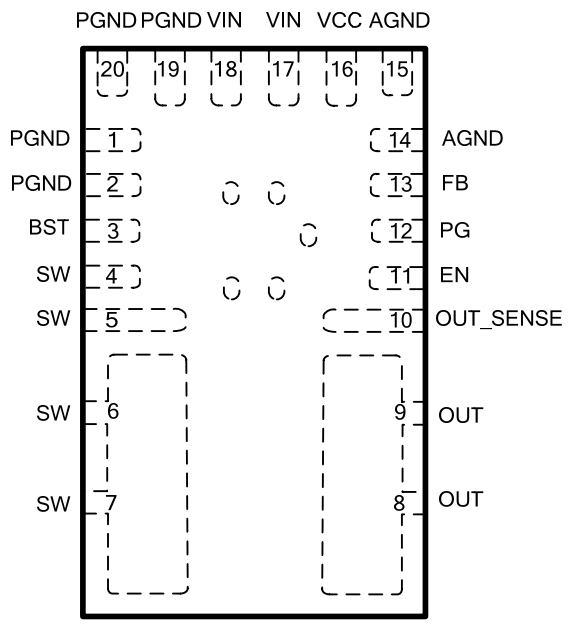
TOP MARKING

MPYW
3632
CLLL
M

MP: MPS prefix
Y: Year code
W: Week code
3632C:Part number
LLL: Lot number
M: Module

PACKAGE REFERENCE

TOP VIEW



QFN-20 (3mmx5mmx1.6mm)

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to 20V
V_{SW} ..... -0.6V (-5V for <10ns) to V_{IN} + 0.7V (22V for <10ns)
V_{BST} ..... V_{SW} + 4V
V_{EN} 18V
V_{OUT} 6.5V
V_{PG} 5.5V
All other pins ..... -0.3V to 4V
Continuous power dissipation (T_A = +25°C) (2) 2.7W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to 150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 4V to 18V
Output voltage (V_{OUT}) ..... 0.8V to 5.5V
Operating junction temp. (T_J) ..... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
QFN-20 (3mmx5mmx1.6mm)	46	10	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C (5), typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V			15	µA
Supply current (quiescent)	I_Q	No switching, V_{FB} = 0.85V		1200		µA
HS switch on resistance	$HS_{RDS(ON)}$	V_{BST-SW} = 3.3V		36		mΩ
LS switch on resistance	$LS_{RDS(ON)}$	V_{CC} = 3.3V		18		mΩ
Inductor DC resistance	L_{DCR}			25		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 12V			1	µA
Switching frequency	F_{SW}	V_{OUT} = 3.3V	2700	3000	3300	kHz
		V_{OUT} = 1.2V	2700	3000	3300	kHz
Low-side valley current limit	I_{LIMIT1}		3.0	3.3	3.9	A
Low-side negative current limit	I_{LIMIT2}	OVP condition		-2.5		A
ZCD threshold	I_{ZCD}		-100	50	200	mA
Minimum on time (6)	T_{ON_MIN}			25		ns
Minimum off time	T_{OFF_MIN}			80		ns
Feedback voltage	V_{REF}	T_J = -40°C to +125°C	788	800	812	mV
Output over-voltage rising threshold	V_{OVP}		110%	115%	120%	V_{REF}
OVP hysteresis	V_{OVP_HYS}			5%		V_{REF}
OVP delay	T_{OVP}			2		µs
Output pin absolute OV	V_{OVP2}		5.7	6	6.3	V
Absolute OV hysteresis	V_{OVP2_HYS}			100		mV
Absolute OVP delay	T_{OVP2}			2		µs
PG OV threshold rising	$PGOV_{Hi}$	Fault	110%	115%	120%	V_{REF}
PG OV threshold falling	$PGOV_{Lo}$	Good		110%		V_{REF}
PG UV threshold rising	$PGUV_{Hi}$	Good	85%	90%	95%	V_{REF}
PG UV threshold falling	$PGUV_{Lo}$	Fault		80%		V_{REF}
PG deglitch time	PG_{Deg}	Both edges		50		µs
PG sink current capability	VPG	Sink 4mA		0.4	0.6	V
EN rising threshold	V_{EN_RISING}		1.1	1.20	1.224	V
EN falling threshold	V_{EN_FALL}		0.96	1.00	1.04	V
EN to GND pull-down resistor	R_{EN}			1.35		MΩ
VIN UVLO rising	$INUV_{Vth}$		3.2	3.6	3.9	V
VIN UVLO hysteresis	$INUV_{HYS}$			500		mV
VCC regulator	V_{CC}			3.3		V
VCC load regulation		I_{CC} = 20mA		3		%
Soft-start time	T_{SS}	V_{OUT} from 10% to 90%		1.65		ms
Thermal shutdown (6)	T_{SD}			150		°C
Thermal hysteresis (6)	T_{SD_HYS}			20		°C

NOTES:

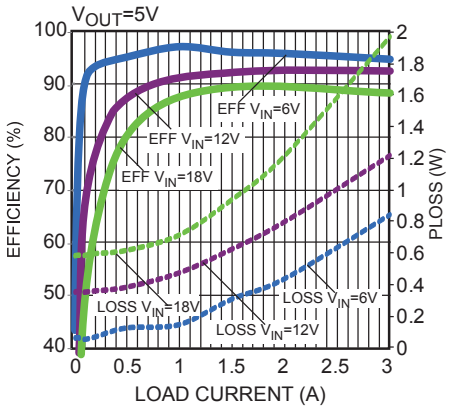
5) Guaranteed by over-temperature correlation, not tested in production.

6) Guaranteed by design.

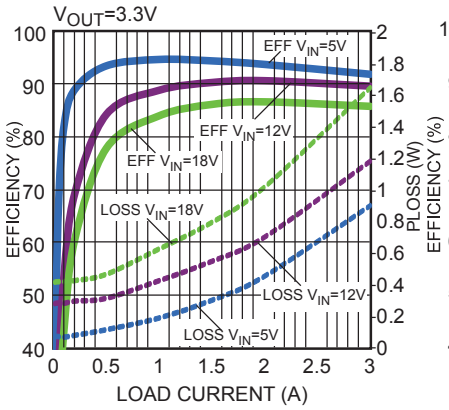
TYPICAL CHARACTERISTICS

Performance waveforms are tested on the evaluation board in the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

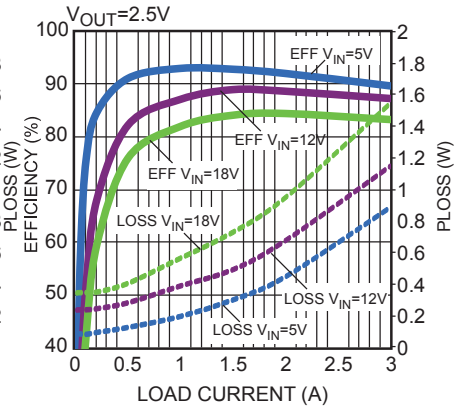
Efficiency &Ploss vs. Load Current



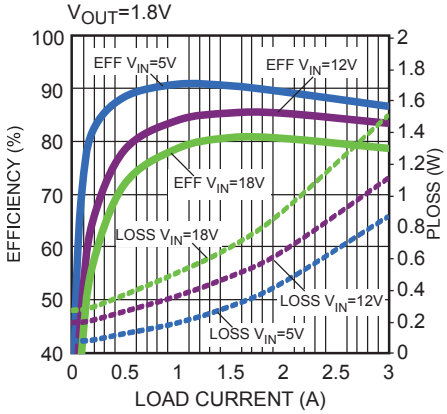
Efficiency &Ploss vs. Load Current



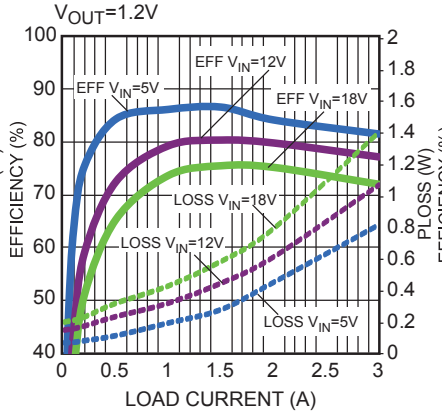
Efficiency &Ploss vs. Load Current



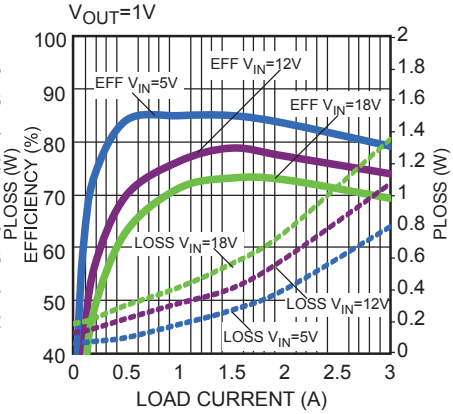
Efficiency &Ploss vs. Load Current



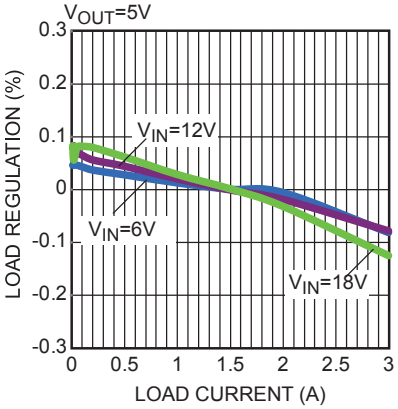
Efficiency &Ploss vs. Load Current



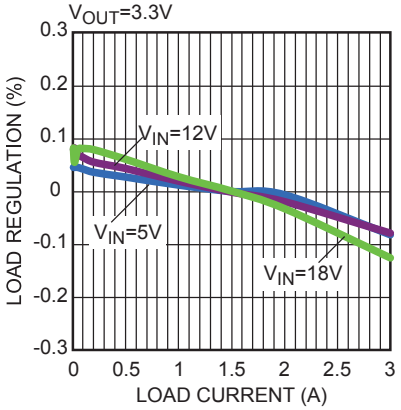
Efficiency &Ploss vs. Load Current



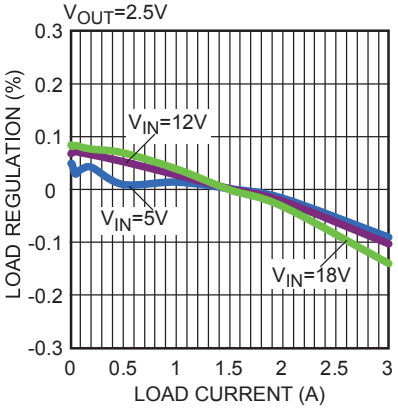
Load Regulation



Load Regulation



Load Regulation

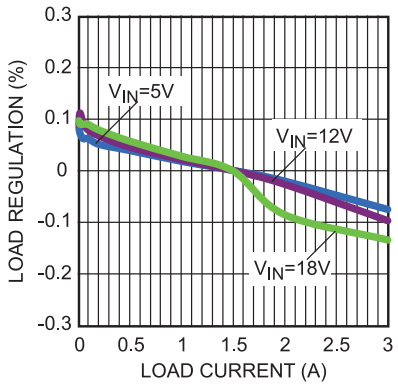


TYPICAL CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

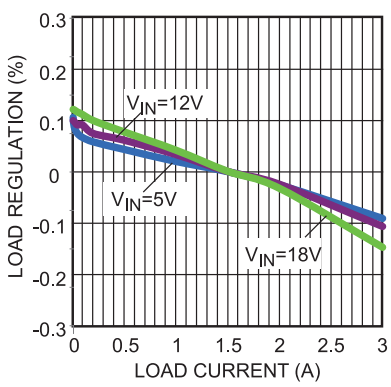
Load Regulation

V_{OUT}=1.8V



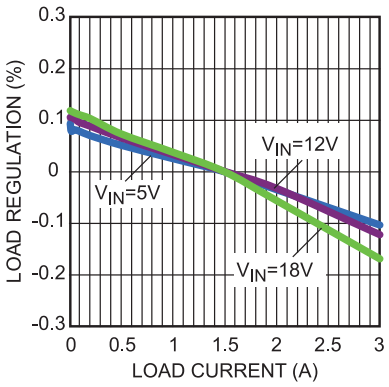
Load Regulation

V_{OUT}=1.2V



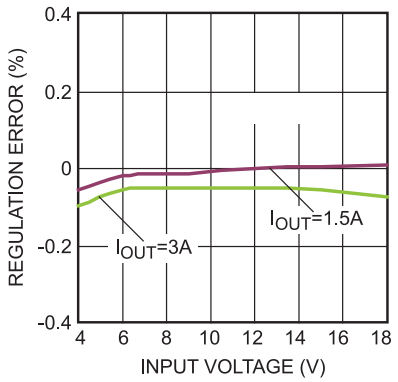
Load Regulation

V_{OUT}=1V



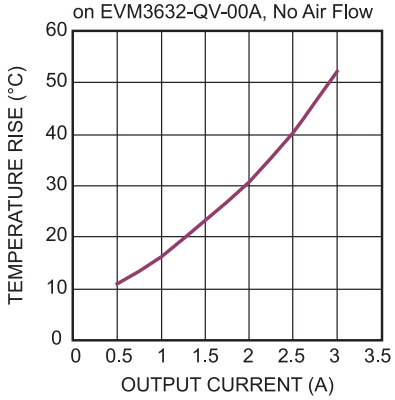
Line Regulation

V_{OUT}=3.3V



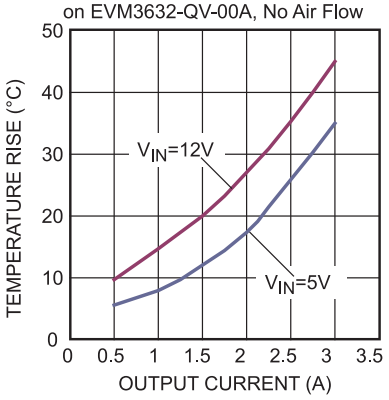
Case Temperature Rise

V_{OUT}=5V, T_A=14°C,
on EVM3632-QV-00A, No Air Flow



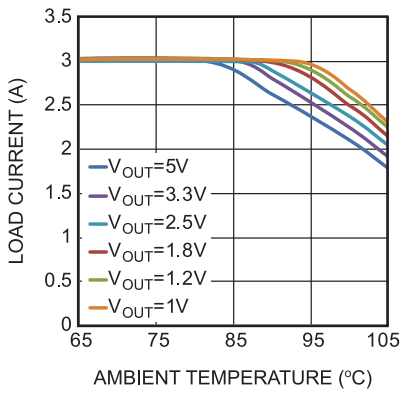
Case Temperature Rise

V_{OUT}=3.3V, T_A=14°C,
on EVM3632-QV-00A, No Air Flow



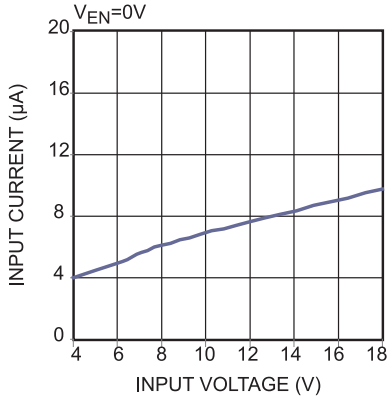
Thermal Derating

V_{iN}=12V

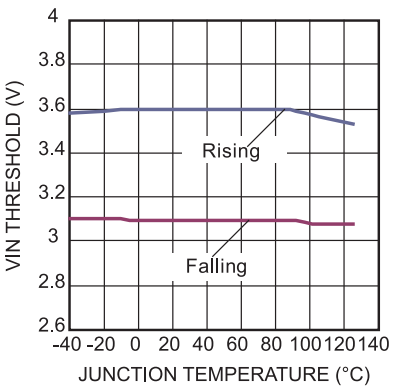


Supply Current After EN Shutdown

V_{EN}=0V



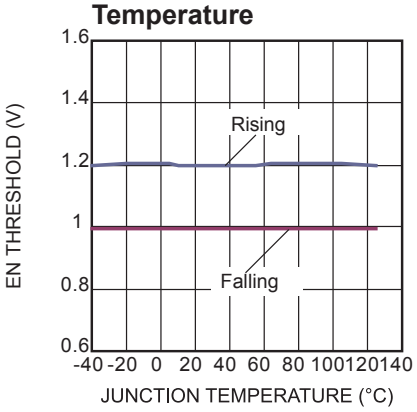
VIN UVLO Threshold



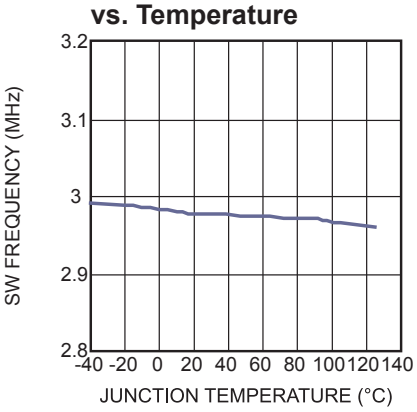
TYPICAL CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

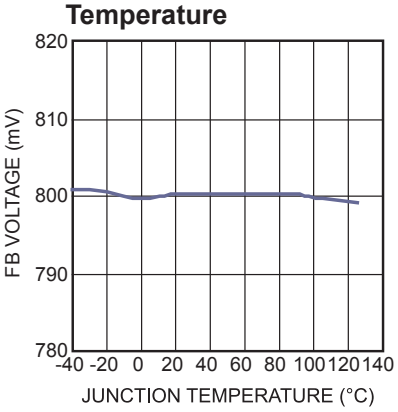
EN Threshold vs. Temperature



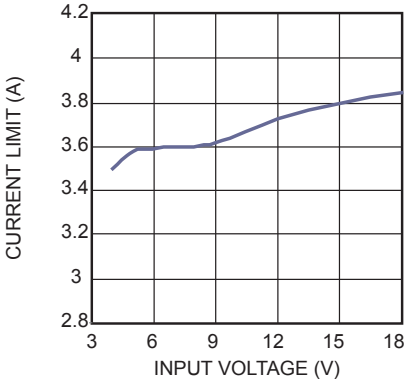
Switching Frequency vs. Temperature



FB Voltage vs. Temperature

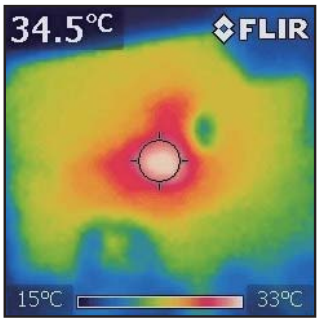


Overload Current vs. Input Voltage



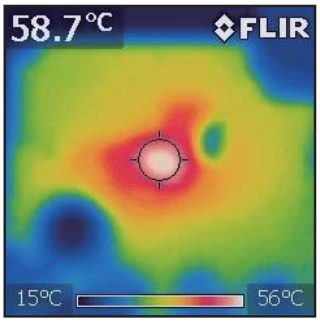
Thermal Test

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=1.5A,
no air flow, measured on EVM3632-QV-00A



Thermal Test

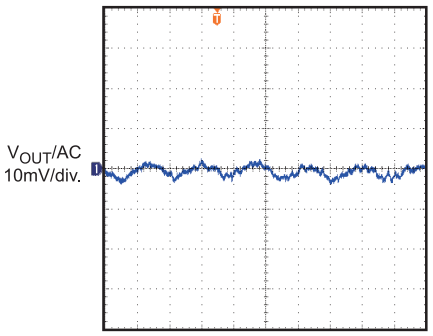
V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A, no air flow,
measured on EVM3632-QV-00A



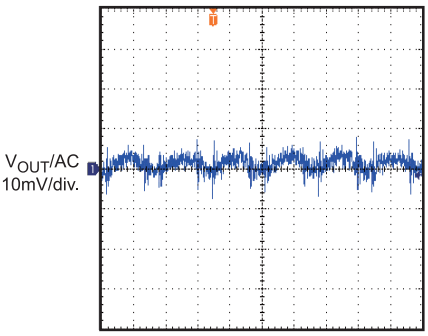
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

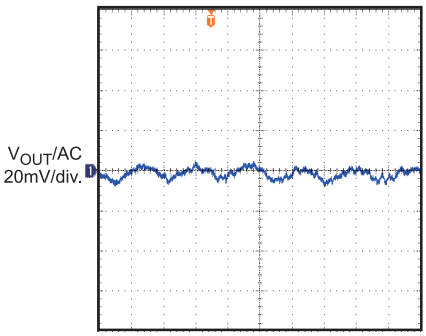
Output Ripple
I_{OUT}=3A, Probe BW=20MHz



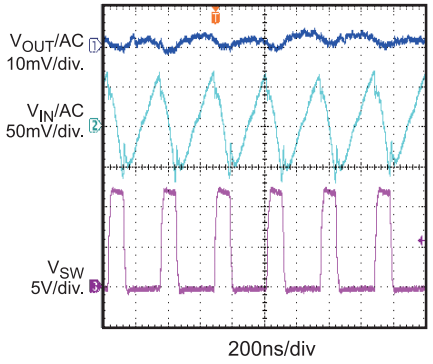
Output Ripple
I_{OUT}=3A, Probe BW=150MHz



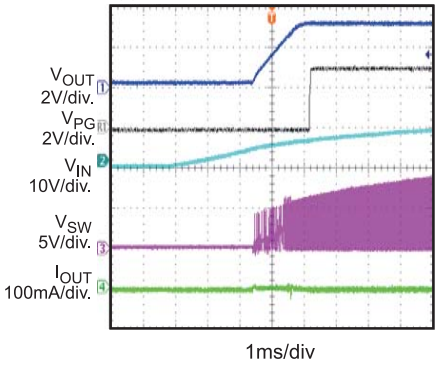
Output Ripple
I_{OUT}=0A, Probe BW=20MHz



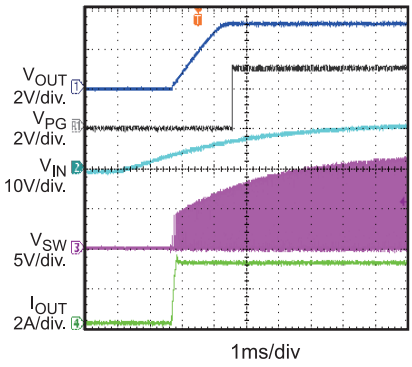
Input vs. Output Ripple
I_{OUT}=3A, C_{IN}=10µF, Probe BW=20MHz



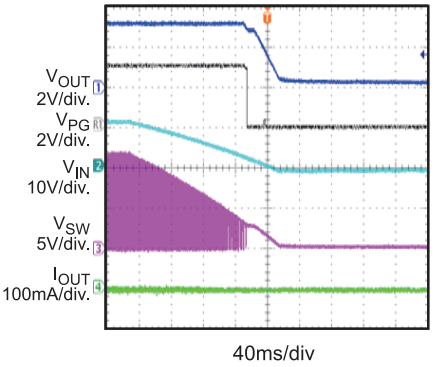
Start-Up through Input Voltage
I_{OUT}=0A



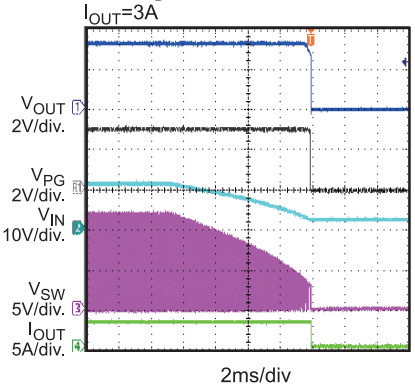
Start-Up through Input Voltage
I_{OUT}=3A



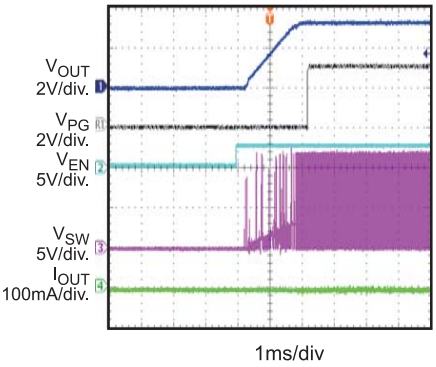
Shutdown through Input Voltage
I_{OUT}=0A



Shutdown through Input Voltage
I_{OUT}=3A



Start-Up through EN
I_{OUT}=0A

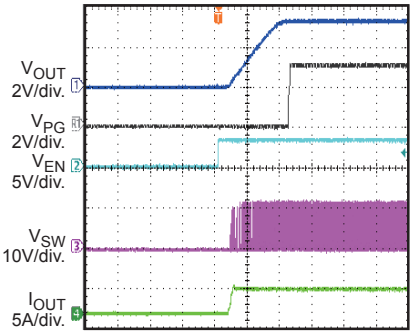


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

Start-Up through EN

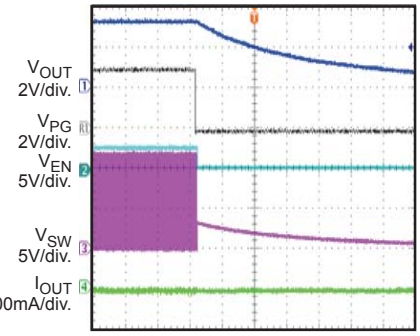
I_{OUT}=3A



1ms/div.

Shutdown through EN

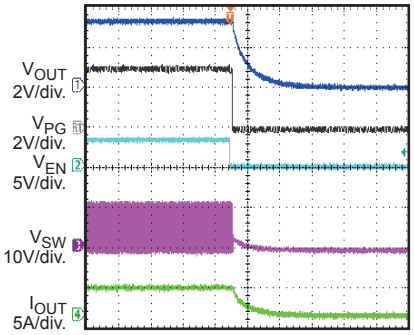
I_{OUT}=0A



200ms/div.

Shutdown through EN

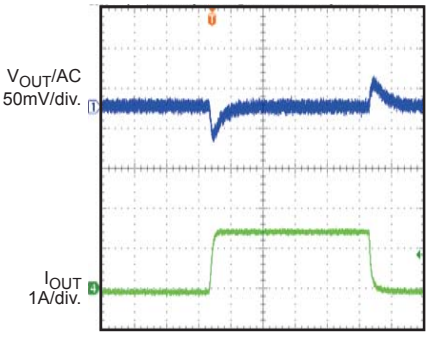
I_{OUT}=3A



40µs/div.

Response to Load Transient

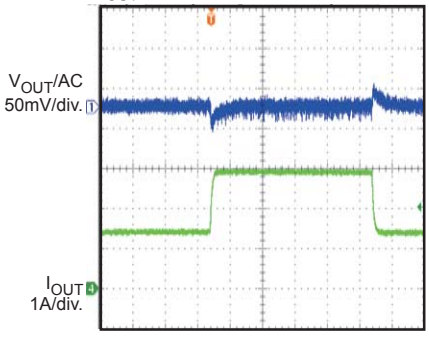
I_{OUT}=0A-1.5A, 2.5A/µs



100µs/div

Response to Load Transient

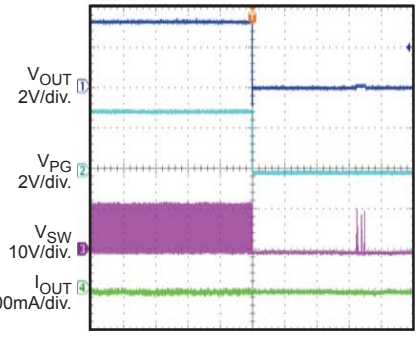
I_{OUT}=1.5A-3A, 2.5A/µs



100µs/div

V_{OUT} Short Protection

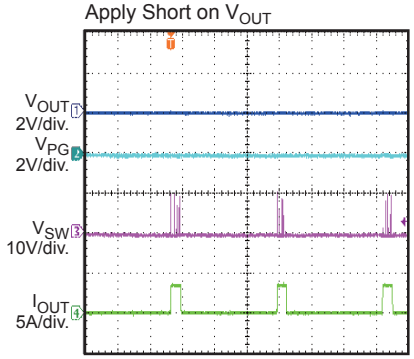
I_{OUT}=0A



4ms/div

Steady State of Short Protection

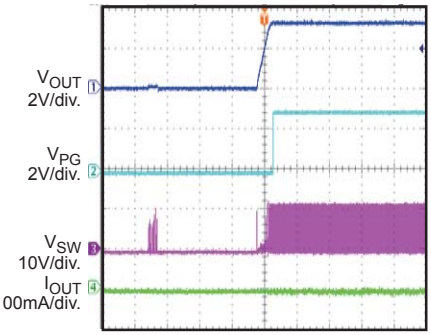
Apply Short on V_{OUT}



4ms/div

Recover from V_{OUT} Short

I_{OUT}=0A

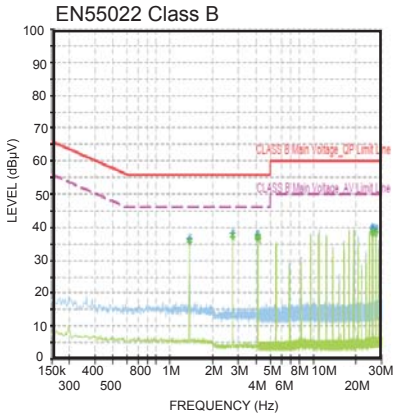


4ms/div

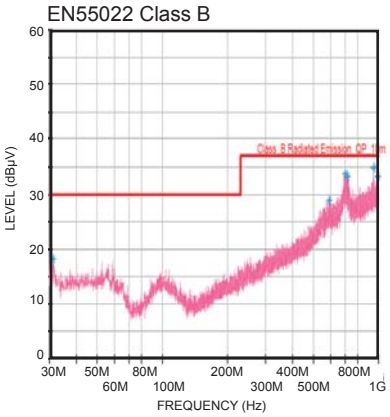
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, Fs=3MHz, with the EMI filters, unless otherwise noted.

CE Result



RE Result



PIN FUNCTIONS

Pin #	Name	Description
1, 2, 19, 20	PGND	**System ground.** PGND is the reference ground of the regulated output voltage. PGND requires special consideration during PCB layout. Connect PGND to GND with copper traces and vias.
3	BST	**Bootstrap.** A bootstrap capacitor is integrated internally. There is no need for external connections.
4 - 7	SW	**Switch output.** Connect SW using a wide PCB trace.
8, 9	OUT	**Power output.**
10	OUT_SENSE	**Output sense.** Connect OUT_SENSE to the positive terminal of the output capacitor. It is recommended to connect OUT_SENSE to OUT through a 1kΩ resistor.
11	EN	**Enable.** Drive EN high to enable the MPM3632C.
12	PG	**Power good output.** PG is the power good indication. PG is an open-drain structure. PG switches low if the output voltage is out of the regulation window.
13	FB	**Feedback.** An external resistor divider from the output to GND tapped to FB sets the output voltage.
14, 15	AGND	**Analog ground.** Connect AGND to PGND.
16	VCC	**Internal 3.3V LDO regulator output.** The MPM3632C integrates an internal decoupling capacitor. There is no need for external connections.
17, 18	VIN	**Supply voltage.** The MPM3632C operates from a 4V to 18V input rail. A ceramic capacitor is required to decouple the input rail. Connect VIN using a wide PCB trace.

BLOCK DIAGRAM

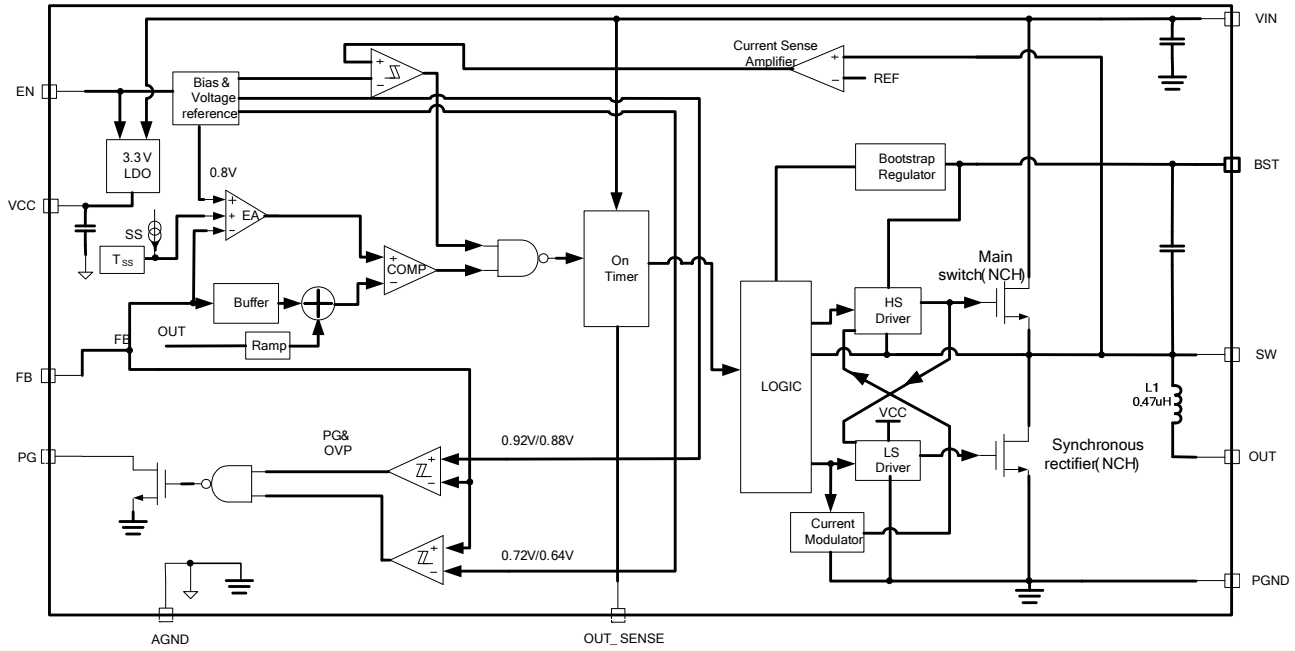


Figure 1: Functional Block Diagram

OPERATION

Pulse-Width Modulation (PWM) Operation

The MPM3632C is a fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on if the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The on period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET turns off and is turned on again when V_{FB} drops below V_{REF}. By repeating operation in this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is off to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called a shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and LS-FET on period or the LS-FET off and HS-FET on period.

Internal compensation is applied for COT control to provide a more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves jitter performance without affecting line or load regulation.

Regular-Load Operation

Continuous conduction mode (CCM) is when the output current is high and the inductor current is always above zero amps (see Figure 2). When V_{FB} is below V_{REF} - V_{DC_ERROR}, the HS-FET is turned on for a fixed interval determined by the internal one-shot on-timer. When the HS-FET is turned off, the LS-FET is turned on until the next period. In CCM, the switching frequency is fairly constant. This is called pulse-width modulation (PWM) operation.

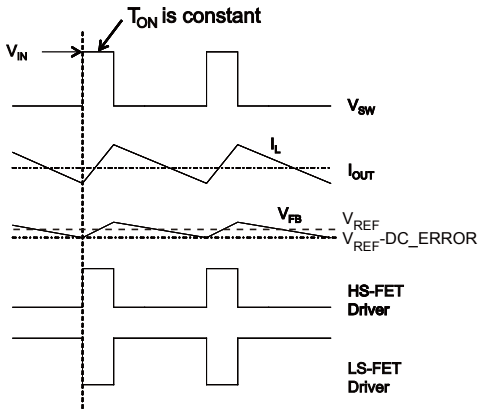


Figure 2: Heavy-Load Operation

DC Auto-Tune Loop

The MPM3632C applies a DC auto-tune loop to balance the DC error between V_{FB} and V_{REF} by adjusting the comparator input reference to make V_{FB} always follow V_{REF}. This is a slow loop and improves the load and line regulation without affecting the transient performance. The relationship between V_{FB}, V_{REF}, and REF is shown in Figure 3.

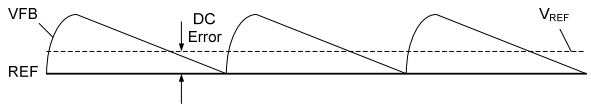


Figure 3: DC Auto-Tune Loop Operation

Internal Regulator

A 3.3V internal regulator powers most of the internal circuitries. When EN is high, this regulator takes VIN and operates in the full VIN range. When VIN is higher than 3.3V, the output of the regulator is in full regulation. When VIN is lower than 3.3V, the output voltage decreases and follows the input voltage.

Enable Control (EN)

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. EN is a high-voltage input node, so connecting EN to the input can enable the part to start-up automatically. EN can support an 18V input voltage.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MPM3632C UVLO comparator monitors VIN. The UVLO rising threshold is about 3.6V, while its falling threshold is 3.1V.

Soft Start (SS)

Soft start prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to 3.3V. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, the error amplifier uses REF as the reference.

Over-Current Protection (OCP) and Hiccup

The MPM3632C has a cycle-by-cycle over-current (OC) limiting control. The current-limit circuit employs a valley current-sensing algorithm. The MPM3623 uses the $R_{DS(ON)}$ of the LS-FET as a current-sensing element. If the magnitude of the current-sense signal is above the current-limit threshold, PWM is not allowed to initiate a new cycle.

The trip level is fixed internally. The inductor current is monitored by the voltage between GND and SW. GND is used as the positive current sensing node, so GND should be connected to the source terminal of the bottom MOSFET.

Since the comparison is done during the HS-FET off and LS-FET on state, the OC trip level sets the valley level of the inductor current. Therefore, the load current at the over-current threshold (I_{OC}) can be calculated with Equation (2):

$$I_{OC} = I\_limit + \frac{\Delta I_{inductor}}{2} \quad (2)$$

In an over-current condition, the current to the load exceeds the current to the output capacitor. Therefore, the output voltage tends to fall off. The output voltage drops until V_{FB} is below the under-voltage (UV) threshold (typically 50% below the reference). Once UV is triggered, the MPM3632C enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead-shorted to ground and reduces the average short-circuit current greatly to alleviate thermal issues and protect the regulator. The MPM3632C exits hiccup mode once the over-current condition is removed.

Over-Voltage Protection (OVP)

The MPM3632C monitors the feedback voltage to detect an over-voltage condition. When V_{FB} rises higher than 115% of V_{REF}, the controller enters a dynamic regulation period. During this period, the IC forces the LS-FET on until a -2.5A negative current limit is triggered, and then the LS-FET turns off for a fixed delay time if the over-voltage (OV) condition still remains. This discharges the output to keep it within the normal range. The MPM3632C exits dynamic regulation when V_{FB} falls below 110% of V_{REF}.

If V_{OUT}'s absolute voltage exceeds the 6V threshold, the MPM3632C enters dynamic regulation mode to discharge the output voltage.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature is below its lower threshold (typically 130°C), the chip is enabled again.

Power Good Indicator (PG)

PG is an open-drain output. When V_{FB} is above UV and below OV, EN is high, VIN is sufficient, the MPM3632C does not suffer from over-temperature, and PG is set to a high impedance. Otherwise, PG is pulled down to GND. With an external resistor pulled up to a reliable voltage, PG can be used for some digital interfaces.

Floating Driver and Bootstrap Charging

An internal bootstrap capacitor powers the floating power MOSFET driver (see Figure 5). This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.3V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by VIN through D1, M1, C4, L1, and C2. If VIN - V_{SW} exceeds 3.3V, U1 regulates M1 to maintain a 3.3V BST voltage across C4.

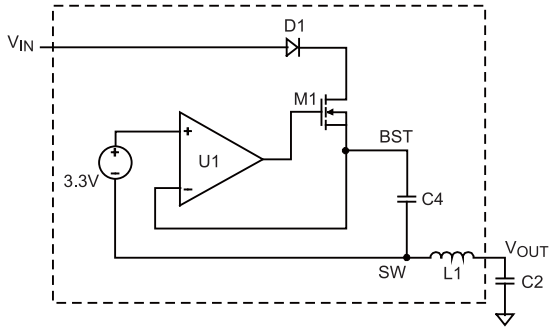


Figure 4: Internal Bootstrap Charging Circuit

Additional RC Snubber Circuit

An additional RC snubber circuit can be used to clamp the voltage spike and dampen the ringing voltage for better EMI performance.

The power dissipation of the RC snubber circuit can be estimated with Equation (3):

$$P_{LOSS}=f_s \times C_s \times VIN^2 \quad (3)$$

Where f_S is the switching frequency, Cs is the snubber capacitor, and VIN is the input voltage.

For improved efficiency, the value of C_S should not be set too high. Generally, a 5.6Ω R_S and a 330pF C_S are recommended to generate the RC snubber circuit (see Figure 5).

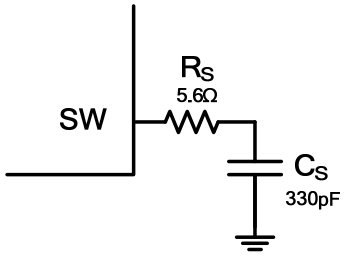


Figure 5: Additional RC Snubber Circuit

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage. Choose the R1 resistance. Then calculate R2 with Equation (4):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1} \quad (4)$$

The feedback circuit is shown in Figure 6. See Table 1 for a list of recommended feedback network parameters for common output voltages.

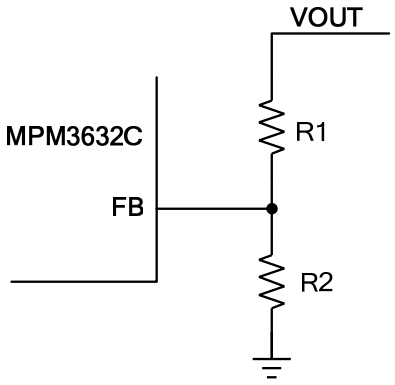


Figure 6: Feedback Network

Table 1: Recommended Parameters for Common Output Voltages

V_{IN} (V)	V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	Small Solution Size (C_{IN} = 10µF, C_{OUT} = 22µF/0805/16V)		Low V_{OUT} Ripple (C_{IN} = 10µF, C_{OUT} = 2*22µF/0805/16V)	
				V_{OUT} Ripple in PWM (mV) [8]	V_{OUT} Ripple on Load Transient (mV) [9]	V_{OUT} Ripple in PWM (mV) [8]	V_{OUT} Ripple on Load Transient (mV) [9]
18	5	47	8.87	8	80	8	76
16				7.4	74	6.4	73
14				6.8	74	4.6	73
12				6.4	73	4	72
10				5.6	70	3.4	69
8				5	70	3.2	69
6 [9]				22.4	87	3.5	80
18	3.3	47	15	6.8	49	5	49
16				6.8	49	5.2	47
14				6.8	46	5.2	45
12				5.2	45	5	44
10				5	44	4.6	43
8				4.6	42	3.8	42
5 [9]				3.6	46	3.4	46
18	2.5	47	22	7.6	39	3.8	39
16				6.2	37	4.6	36
14				6	36	4.2	35
12				5.5	35	4	34
10				5	34	4	33
8				5.2	33	4	33
5				5.2	34	3.8	32

Table 1: Recommended Parameters for Common Output Voltages *(continued)*

V_{IN} (V)	V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	Small Solution Size (C_{IN} = 10µF, C_{OUT} = 22µF/0805/16V)		Low V_{OUT} Ripple (C_{IN} = 10µF, C_{OUT} = 2*22µF/0805/16V)	
				V_{OUT} Ripple in PWM (mV) (7)	V_{OUT} Ripple on Load Transient (mV) (8)	V_{OUT} Ripple in PWM (mV) (7)	V_{OUT} Ripple on Load Transient (mV) (8)
18	1.8	47	37.4	5.4	31	4.2	30
16				5.6	30	4.2	30
14				6	27	4	26
12				5.2	26	4	25
10				5.2	25	4	25
8				4.2	24	4.2	24
5				4.2	24	3.8	23
18	1.5	47	53.6	5	27	4.4	27
16				5.2	27	3.8	26
14				5.6	24	4	24
12				4.8	23	4.2	23
10				4.8	22	3.8	22
8				4.2	21	4.2	21
5				3.8	21	3	21
18	1.2	47	93.1	4.4	22	3.6	21
16				5.2	23	3.4	20
14				5.8	21	3.2	20
12				4.6	19	3.6	18
10				3.4	18	3.4	17
8				4	17	4	17
5				3.2	16	3	14.8
14	1	47	187	4.8	19	3.4	18
12				3.6	17	3	17
10				4.6	15	4.6	15
8				3.6	15	3.6	14
5				3.6	15	3.2	14

NOTES:

7) V_{OUT} PWM ripple is tested when I_{OUT} = 3A.
8) Load transition from 1A to 3A, slew rate = 2.5A/µs.
9) A larger C_{IN} may be required in large duty cycle applications to stabilize the system.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10µF capacitor is sufficient.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case condition occurs at V_{IN} = 2*V_{OUT} shown in Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (i.e.: 0.1µF) should be placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent an excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Selecting the Output Capacitor

An output capacitor (C2) is required to maintain the DC output voltage. Low ESR ceramic capacitors can be used with the MPM3632C to keep the output ripple low. Generally, a 22µF output ceramic capacitor is sufficient for most cases.

When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

Where L_1 is a 0.47µH, integrated inductor.

The characteristics of the output capacitor also affect the stability of the regulation system.

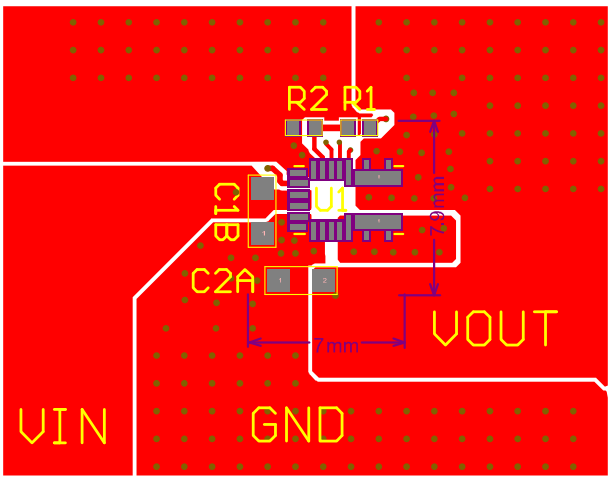
PCB Layout Guidelines (10)

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 7 and follow the guidelines below.

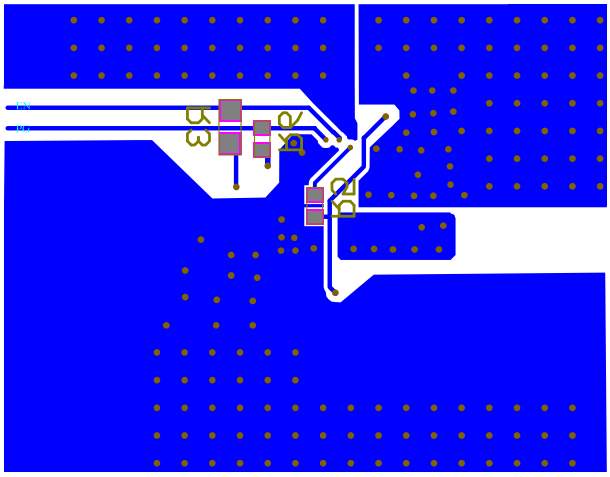
1. Keep the connection of the input ground and GND as short and wide as possible.
2. Ensure that all feedback connections are short and direct.
3. Place the feedback resistors as close as to the chip as possible.
4. Route sensitive analog areas such as FB away from SW.
5. Place enough vias around chip for better thermal performances

NOTES:

10) The recommended layout is based on Figure 8 through Figure 15.



Top Layer



Bottom Layer

Figure 7: Recommended Layout

TYPICAL APPLICATION CIRCUITS

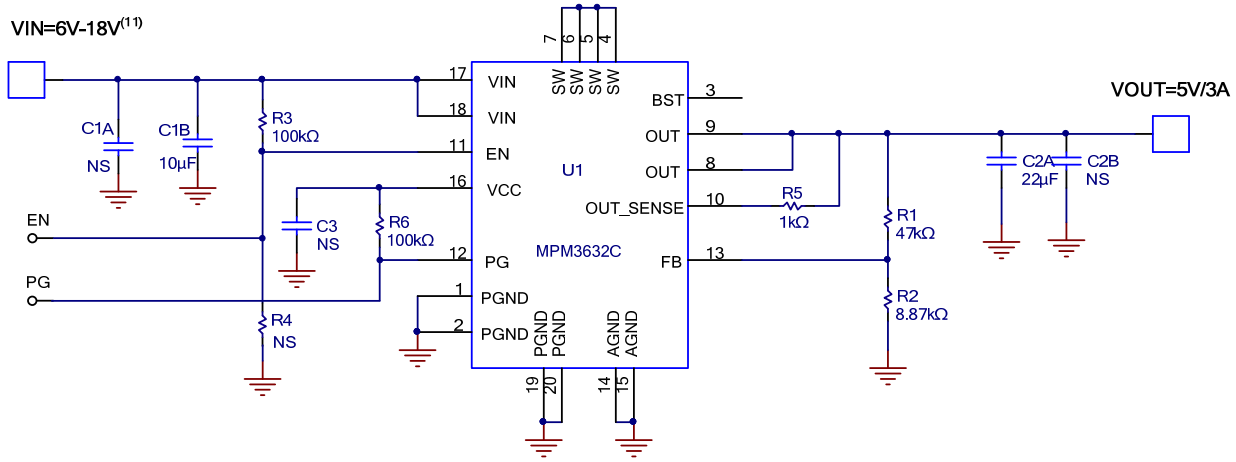


Figure 8: 5V Output

NOTES:

11) Larger C_{IN} may be required at large duty cycle applications to stabilize the system.

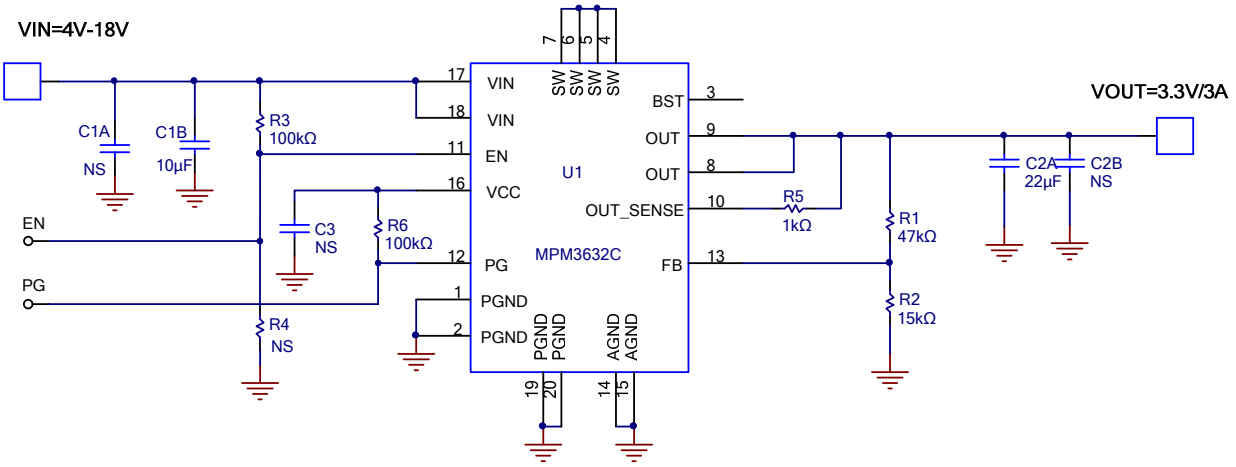


Figure 9: 3.3V Output

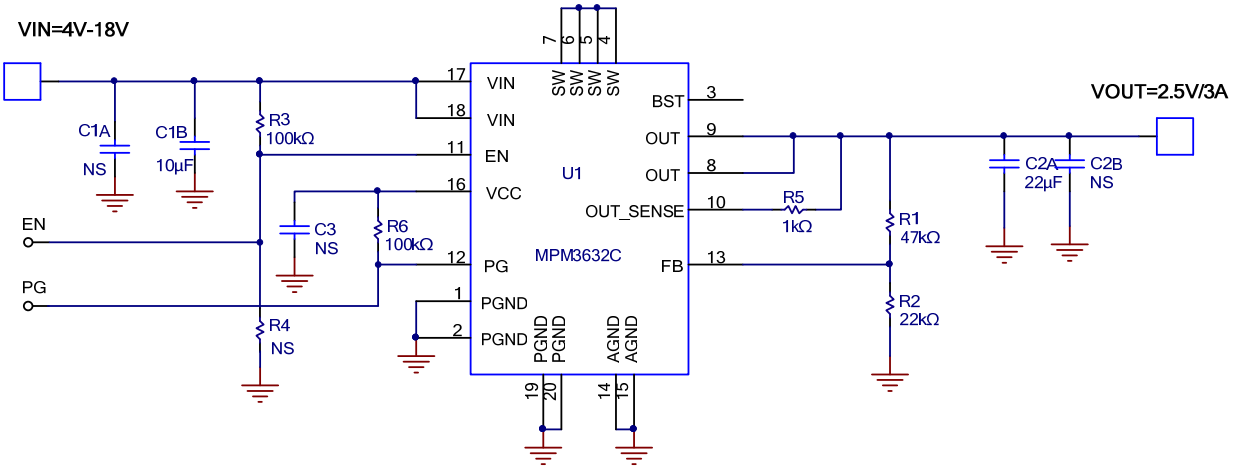


Figure 10: 2.5V Output

TYPICAL APPLICATION CIRCUITS *(continued)*

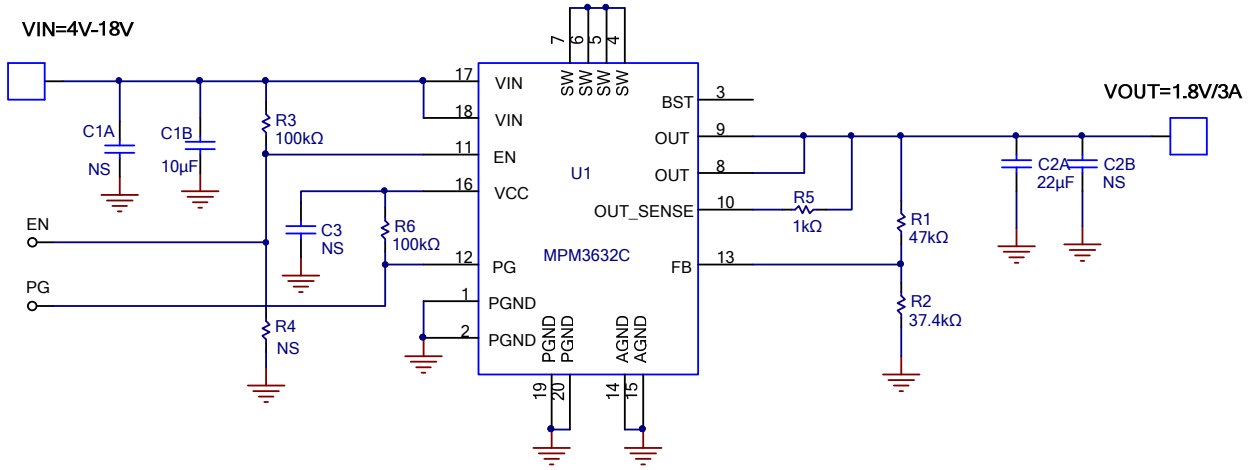


Figure 11: 1.8V Output

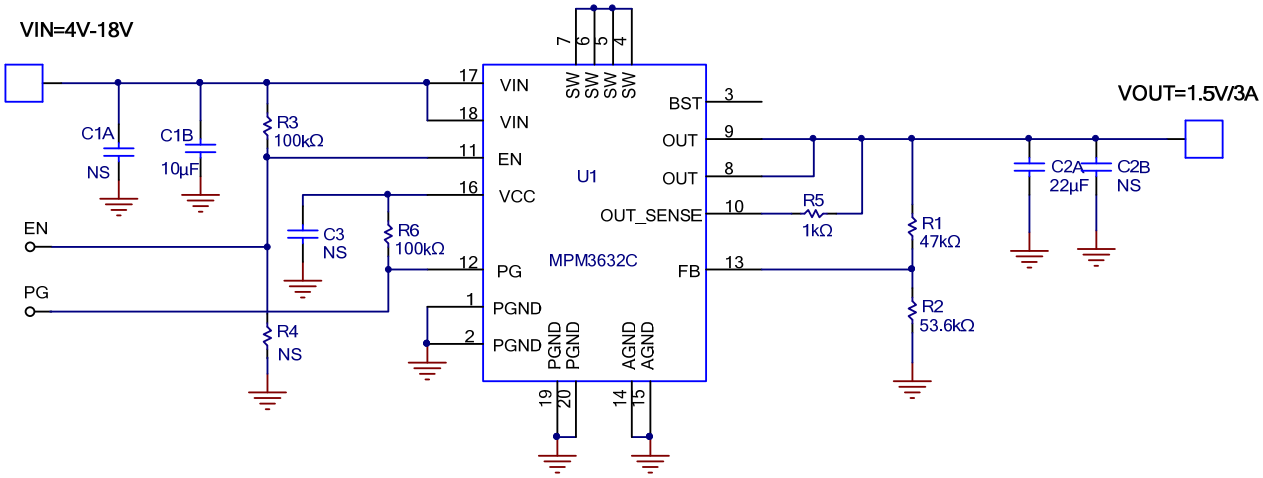


Figure 12: 1.5V Output

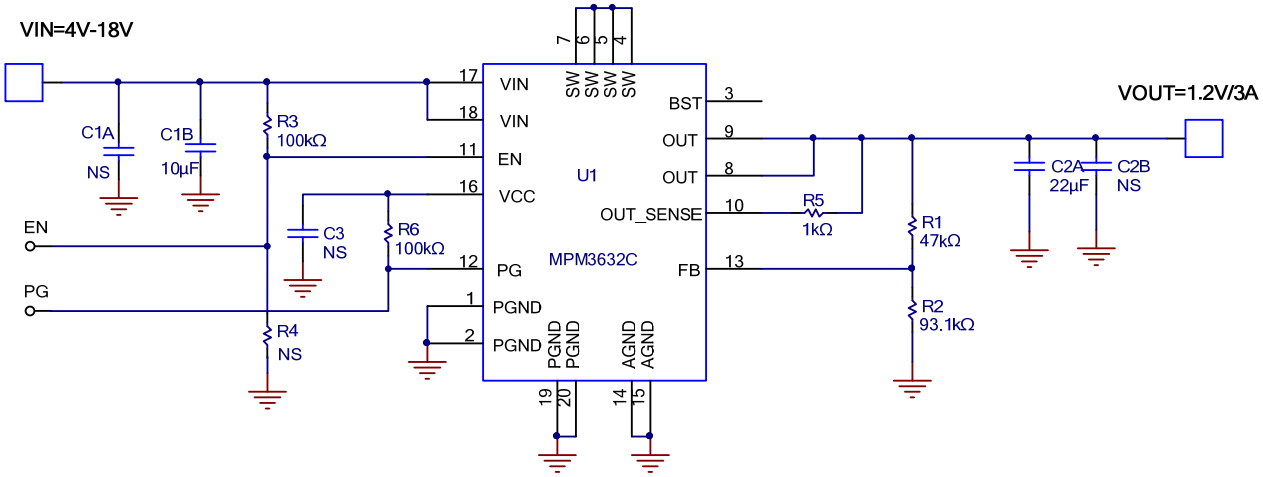


Figure 13: 1.2V Output

TYPICAL APPLICATION CIRCUITS *(continued)*

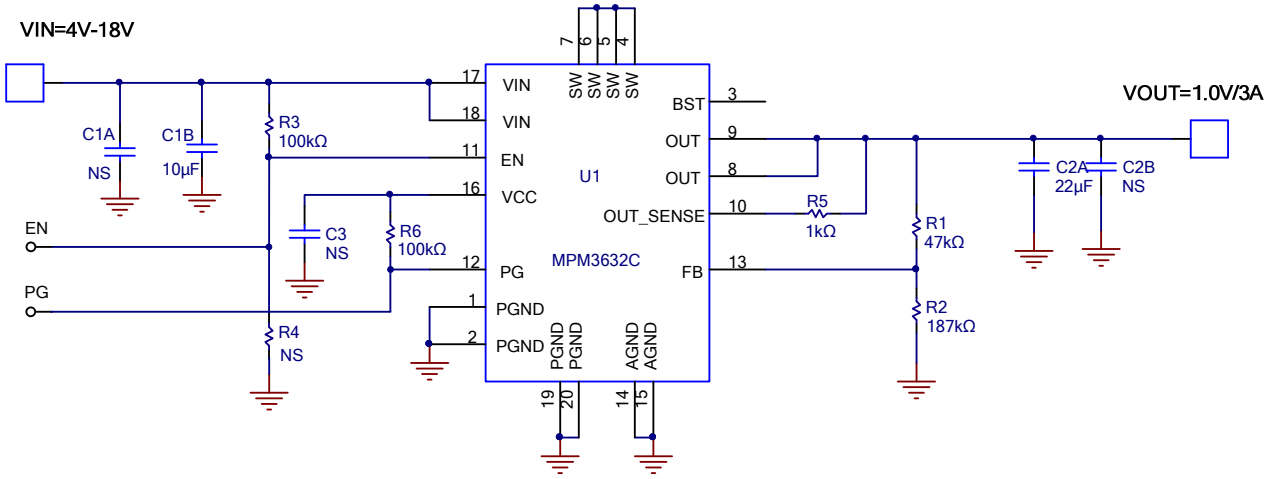


Figure 14: 1.0V Output

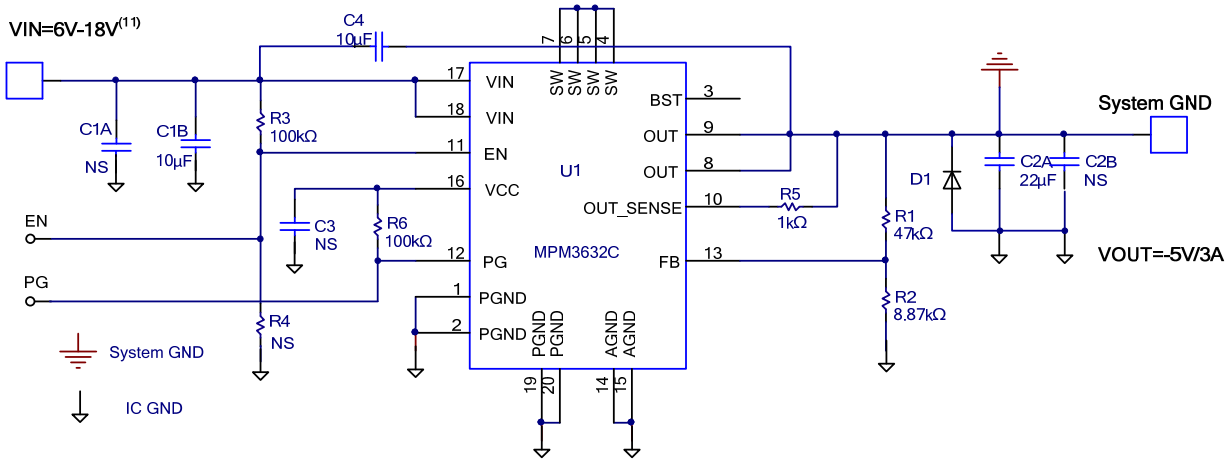


Figure 15: -5V Output

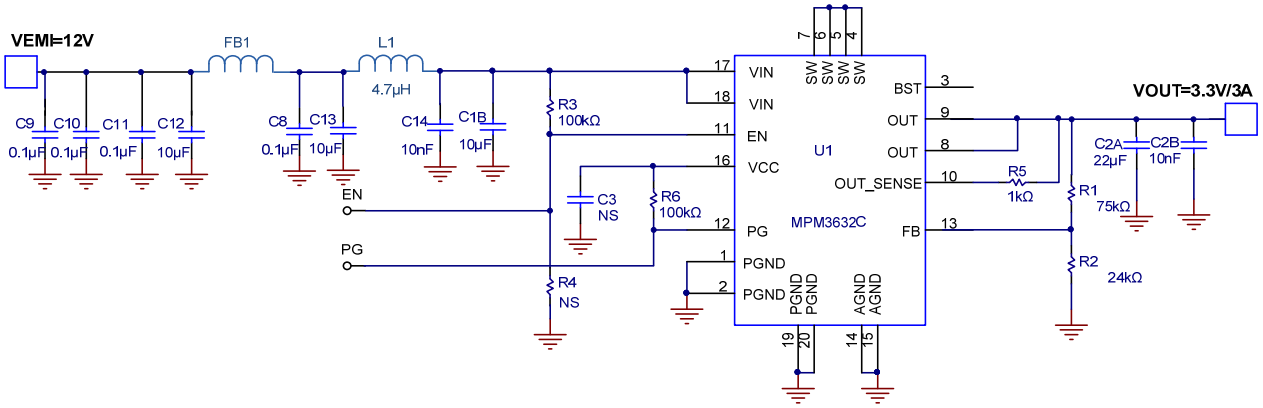
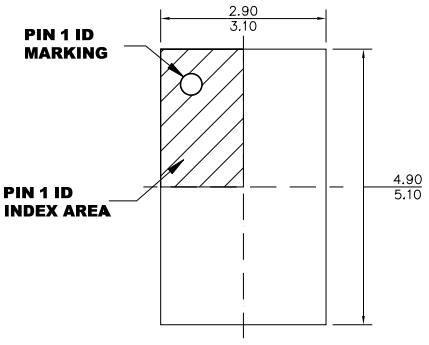


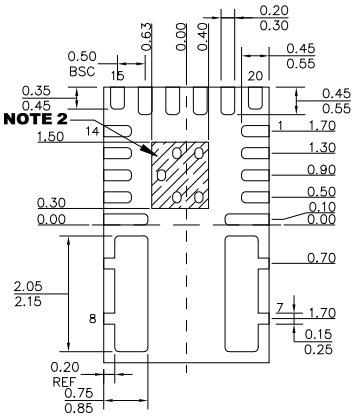
Figure 16: EMI Test Circuit

PACKAGE INFORMATION

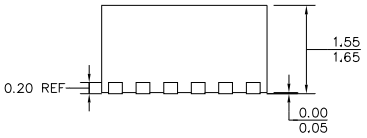
QFN-20 (3mmx5mmx1.6mm)



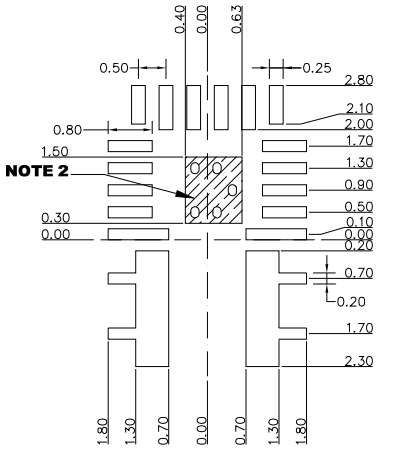
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) SHADED AREA IS THE KEEP-OUT ZONE. ANY PCB METAL TRACE AND VIA ARE NOT ALLOWED TO CONNECT TO THIS AREA ELECTRICALLY OR MECHANICALLY.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.