ESP32-S2

Hardware Design Guidelines

Version 1.1

Espressif Systems

About This Document

The guidelines outline recommended design practices when developing standalone or add-on systems based on the ESP32-S2 series of products, including ESP32-S2 SoCs, ESP32-S2 modules and ESP32-S2 development boards.

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1. Overview

ESP32-S2 is a highly-integrated, low-power, 2.4 GHz Wi-Fi System-on-Chip (SoC) solution. With its state-of-the-art power and RF performance, this SoC is an ideal choice for a wide variety of application scenarios relating to Internet of Things (IoT), wearable electronics and smart home.

At the core of this chip is an Xtensa® 32-bit LX7 CPU that operates at up to 240 MHz. The chip supports application development, without the need for a host MCU.

ESP32-S2 includes a Wi-Fi subsystem that integrates a Wi-Fi MAC, Wi-Fi radio and baseband, RF switch, RF balun, power amplifier, low noise amplifier (LNA), etc. The chip is fully compliant with the IEEE 802.11b/g/n protocol and offers a complete Wi-Fi solution.

ESP32-S2 also integrates advanced calibration circuitries that allow the solution to dynamically adjust itself to remove external circuit imperfections or adjust to changes in external conditions. As such, the mass production of ESP32-S2 solutions does not require expensive and specialized Wi-Fi test equipment.

For more information about ESP32-S2, please refer to *ESP32-S2 Datasheet*.

2. Schematic Checklist

ESP32-S2's integrated circuitry requires only 20 resistors, capacitors and inductors, one crystal and one SPI flash memory chip. ESP32-S2 integrates a Wi-Fi MAC, Wi-Fi radio and baseband, RF switch, RF balun, power amplifier, low noise amplifier (LNA), and advanced calibration circuitries.

ESP32-S2's high integration allows for simple peripheral circuit design. This chapter details ESP32-S2 schematics. ESP32-S2 schematic is shown in Figure 1.

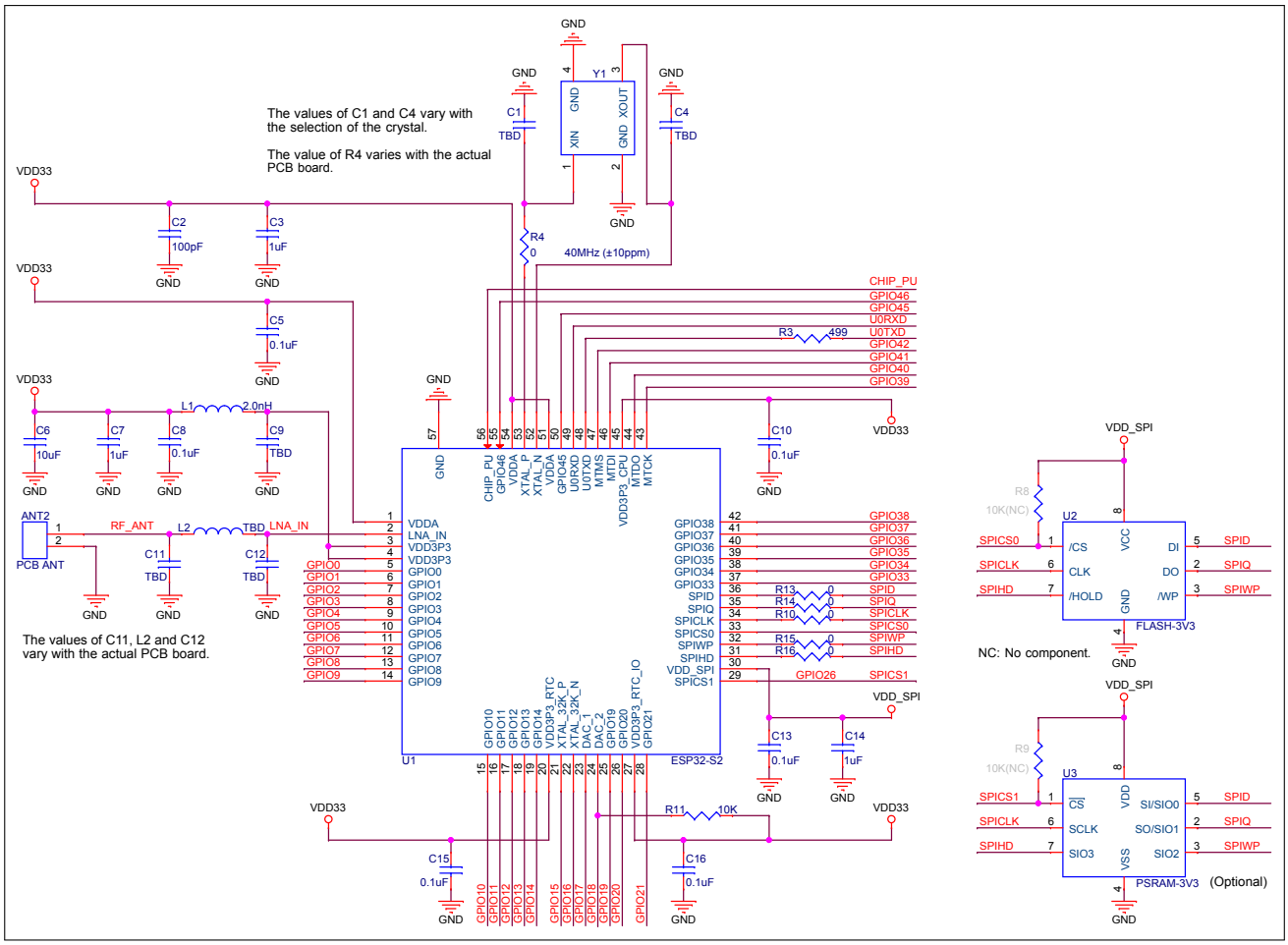

Figure 1: ESP32-S2 Schematic

Any basic ESP32-S2 circuit design may be broken down into nine major sections:

- Power supply
- Power-on sequence and system reset
- Flash and SRAM (optional)
- Crystal oscillator
- RF
- UART
- USB
- ADC

- Touch Sensor

2.1 Power Supply

For further details of using the power supply pins, please refer to Section *Power Scheme* in *ESP32-S2 Datasheet*.

2.1.1 Digital Power Supply

Pin27 and pin45 are the power supply pins for RTC IO and CPU IO, in a voltage range of 3.0 V ~ 3.6 V and 2.8 V ~ 3.6 V, respectively. We recommend adding extra 0.1 μF capacitors close to each digital power supply pin.

VDD_SPI can work as the power supply for the external device at either 1.8 V (when GPIO45 is 1 during boot), or 3.3 V (when GPIO45 is 0 and at default state during boot). We recommend adding extra 0.1 μF and 1 μF capacitors close to VDD_SPI.

- When VDD_SPI operates at 1.8 V, it can be generated from ESP32-S2's internal LDO. The maximum current this LDO can offer is 40 mA, and the output voltage range is 1.8 V ~ 3.6 V.
- When VDD_SPI operates at 3.3 V, it is driven directly by VDD3P3_RTC_IO through a 5 Ω resistor, therefore, there will be some voltage drop from VDD3P3_RTC_IO.

VDD_SPI can also be driven by an external power supply.

The schematic for ESP32-S2 digital power supply pins is shown in Figure 2.

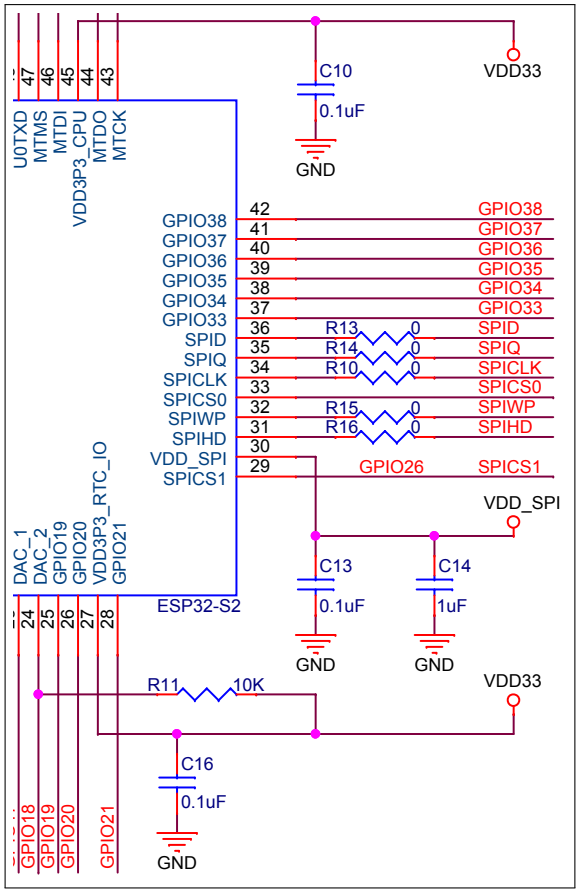

Figure 2: ESP32-S2 Digital Power Supply Pins

Notice: When using VDD_SPI as the power supply pin for the external 3.3 V flash/PSRAM, the supply voltage should be 3.0 V or above, so as to meet the requirements of flash/PSRAM's working voltage.

2.1.2 Analog Power Supply

Pin1, pin3, pin4, pin20, pin51, and pin54 are the analog power supply pins, working at 2.8 V ~ 3.6 V. It should be noted that the sudden increase in current draw, when ESP32-S2 is in transmission mode, may cause a power rail collapse. Therefore, it is highly recommended to add another 10 μF capacitor to the power trace, which can work in conjunction with the 0.1 μF capacitor. In addition, a CLC filter circuit needs to be added near the power pins (pin3 and pin4) so as to suppress high-frequency harmonics. The inductor's rated current is preferably 500 mA or above. Refer to Figure 3 and place the appropriate decoupling capacitor near each analog power pin.

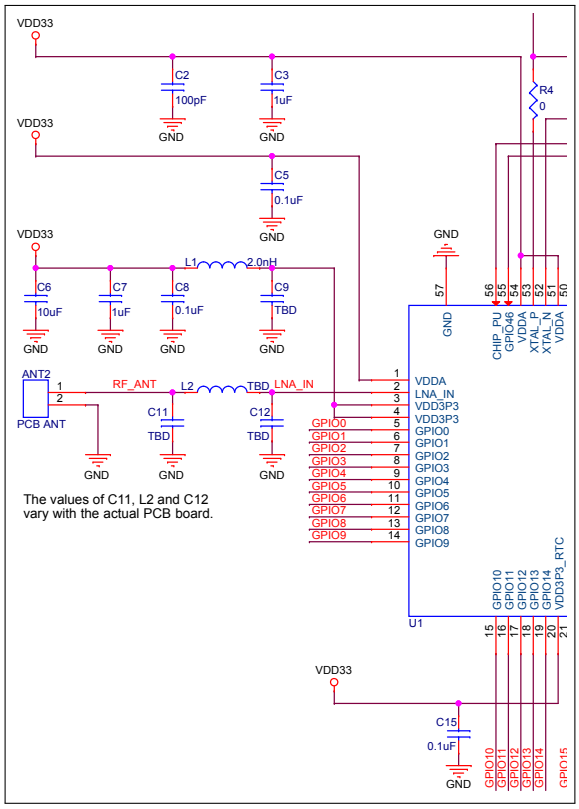

Figure 3: ESP32-S2 Analog Power Supply Pins

Notice:

- The recommended voltage of the power supply for ESP32-S2 is 3.3 V, and its recommended output current is 500 mA or more.
- It is suggested that users add an ESD protection diode at the power entrance.

2.2 Power-on Sequence and System Reset

2.2.1 Power-on Sequence

ESP32-S2 uses a 3.3 V system power supply. The chip should be activated after the power rails have stabilized. This is achieved by delaying the activation of CHIP_PU after the 3.3 V rails have been brought up. More details can be found in Section *Power Scheme* in *ESP32-S2 Datasheet*.

Notice:

To ensure the power supply to the ESP32-S2 chip during power-up, it is advised to add an RC delay circuit at the CHIP_PU pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the power-up timing of the power supply and the power-up and reset sequence timing of the chip.

2.2.2 Reset

CHIP_PU serves as the reset pin of ESP32-S2. The reset voltage (V_{IL_nRST}) should meet the requirements specified in Section *DC Characteristics* in *ESP32-S2 Datasheet*. To avoid reboots caused by external interferences, route the CHIP_PU trace as short as possible, and add a pull-up resistor as well as a capacitor to the ground whenever possible.

Notice:

CHIP_PU pin must not be left floating.

2.3 Flash (compulsory) and SRAM (optional)

ESP32-S2 can support up to 1 GB external flash and 1 GB external SRAM. The ESP32-S2-WROVER module uses a 4 MB SPI flash and 2 MB PSRAM, powered by VDD_SPI. Make sure to select the appropriate flash and PSRAM according to the power voltage on VDD_SPI. We recommend reserving a serial resistor (a 0 Ω resistor can be used initially) on the SPI communication line, to lower the driving current, reduce interference to RF, adjust timing, and improve anti-interference ability.

The schematic for ESP32-S2 flash and SRAM is shown in Figure 4.

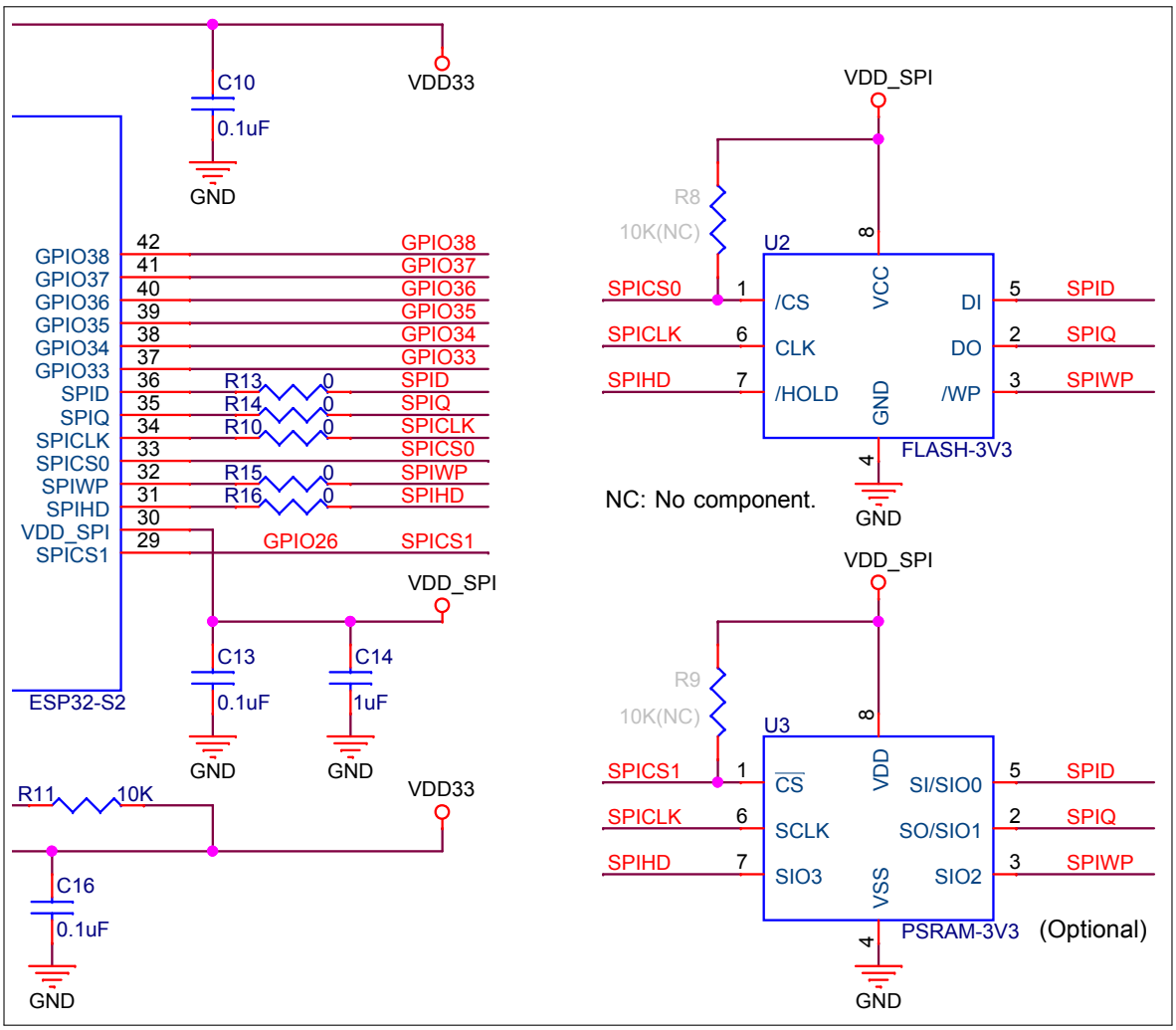

Figure 4: ESP32-S2 Flash and SRAM

2.4 Crystal Oscillator

There are two clock sources for the ESP32-S2, that is, an external crystal oscillator clock source and an RTC clock source.

2.4.1 External Clock Source (compulsory)

Currently, the ESP32-S2 firmware only supports 40 MHz crystal oscillator. The specific capacitive values of C1 and C4 depend on further testing of, and adjustment to, the overall performance of the whole circuit. It is recommended that users reserve a series resistor (a 0 Ω resistor can be used initially) on the XTAL_P clock trace to reduce the drive strength of the crystal, as well as to minimize the impact of crystal harmonics on RF performance. Note that the accuracy of the selected crystal is ±10 ppm.

Figure 5 and Figure 6 show the schematics for crystal and crystal oscillator in ESP32-S2.

Notice:

- If an oscillator is used, its output should be connected to XTAL_P on the chip through a DC blocking capacitor (about 50 pF). XTAL_N can be floating. Please make sure that the oscillator output is stable and its accuracy is within ±10 ppm. It is also recommended that the circuit design for the oscillator is compatible with the use of crystal, in case that if there is a defect in the circuit design, users can still use the crystal.
- Defects in the craftsmanship of the crystal oscillators (for example, large frequency deviation of more than ±10 ppm, unstable performance within operating temperature range, etc) may lead to the malfunction of ESP32-S2, resulting in a decrease of the RF performance.

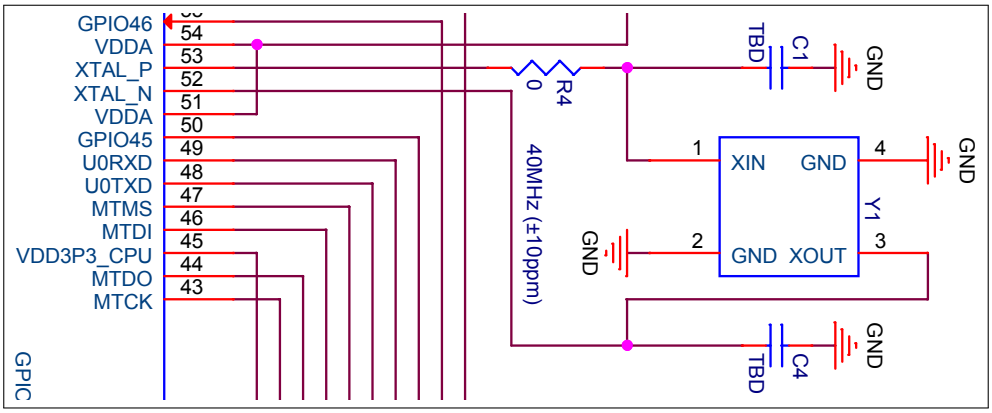

Figure 5: Schematic for ESP32-S2's Crystal

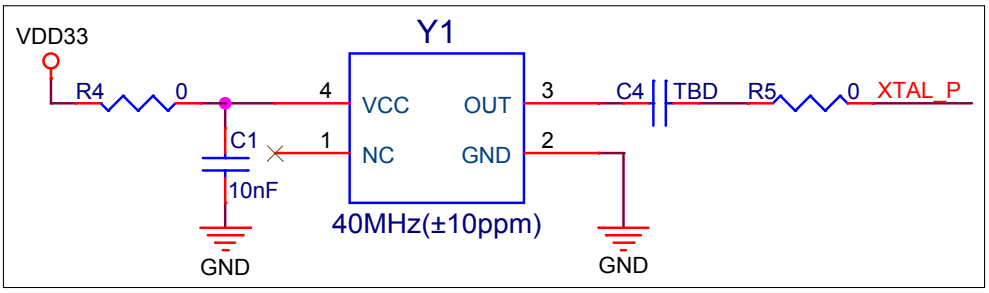

Figure 6: Schematic for ESP32-S2's Crystal Oscillator

2.4.2 RTC (optional)

ESP32-S2 supports an external 32.768 kHz crystal or an external signal (e.g., an oscillator) to act as the RTC sleep clock.

Figure 7 shows the schematic for the external 32.768 kHz crystal.

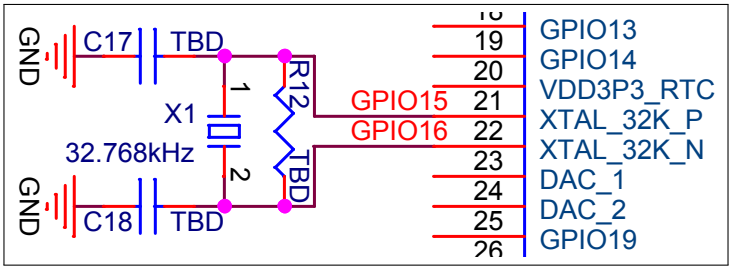

Figure 7: Schematic for ESP32-S2's External Crystal (RTC)

Notice:

- Please note the requirements for the 32.768 kHz crystal.
  - Equivalent series resistance (ESR) $\leqslant 70\ k\Omega$.
  - Load capacitance at both ends should be configured according to the crystal's specification.
- The parallel resistor R12 is used for biasing the crystal circuit (5 MΩ < R12 $\leqslant$ 10 MΩ). In general, users do not need to populate R12.
- If the RTC source is not required, then pin21 (XTAL_32K_P) and pin22 (XTAL_32K_N) can be used as general GPIOs.

Figure 8 shows the schematic of the external signal.

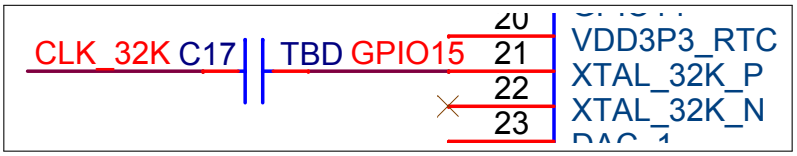

Figure 8: Schematic of External Oscillator

The external signal can be input to XTAL_32K_P through a DC blocking capacitor (about 20 pF). XTAL_32K_N can be floating. The signal should meet the following requirements:

XTAL_32K_P input	Amplitude (Vpp, unit: V)
Sine wave or square wave	0.6 < Vpp < VDD

2.5 RF

The impedance matching point for the RF pin (pin2) of ESP32-S2 is (34+j5) Ω. A π-type matching network is essential for antenna matching in the circuit design. CLC structure is recommended for the matching network. Figure 9 shows the RF matching schematic.

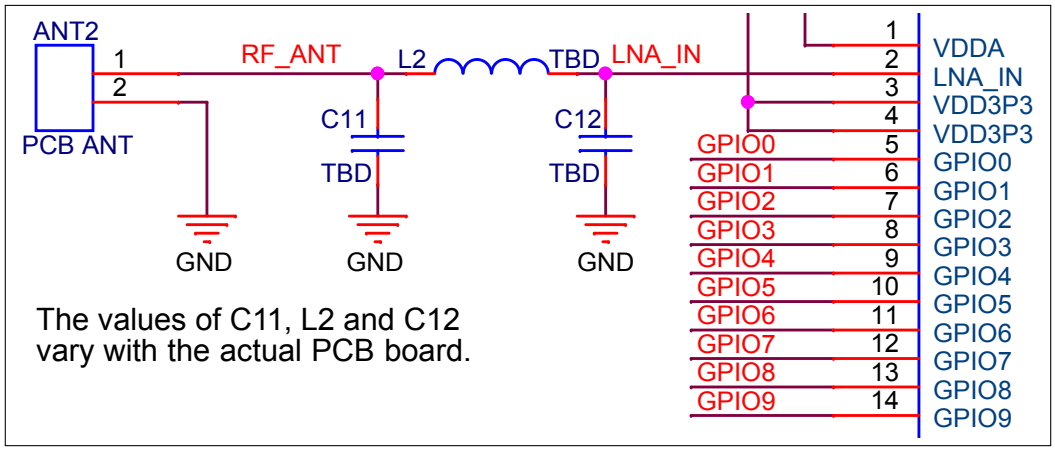

Figure 9: ESP32-S2 RF Matching Schematic

Note:
The parameters of the components in the matching network are subject to the actual antenna and PCB layout.

2.6 UART

Users need to connect a 499 Ω resistor to the U0TXD line in order to suppress the 80 MHz harmonics. GPIO18 works as U1RXD and is in an uncertain state when the chip is powered on, which may affect the chip's entry into download boot mode. To solve this issue, add an external pull-up resistor.

2.7 USB

The ESP32-S2 has a full-speed USB OTG peripheral with integrated transceivers and is compliant with the USB 1.1 specification. GPIO19 and GPIO20 can be used as D- and D + of USB respectively. It is recommended to reserve series resistor and capacitor to the ground on each line, and place them close to the chip side.

2.8 ADC

It is recommended that users add a 0.1 μF filter capacitor to a pad when using the ADC function.

2.9 Touch Sensor

When using the touch function, it is recommended to reserve a series resistor at the chip side to reduce the coupling noise and interference on the line, and to strengthen the ESD protection. The recommended resistance is from 470 Ω to 2 kΩ, preferably 510 Ω. The specific value also depends on the actual test results of the product.

The ESP32-S2 touch sensor adopts a waterproof design. Note that only GPIO14 (TOUCH14) can drive the shield electrode.

3. PCB Layout Design

This chapter introduces the key points of designing ESP32-S2 PCB layout with the example of ESP32-S2 module.

While the high level of integration makes the PCB design and layout process simple, the performance of the system strongly depends on system design aspects. To achieve the best overall system performance, please follow the guidelines specified in this document for circuit design and PCB layout. All the common rules associated with good PCB design still apply and this document is not an exhaustive list of good design practices.

The ESP32-S2 PCB layout design is shown in Figure 10.

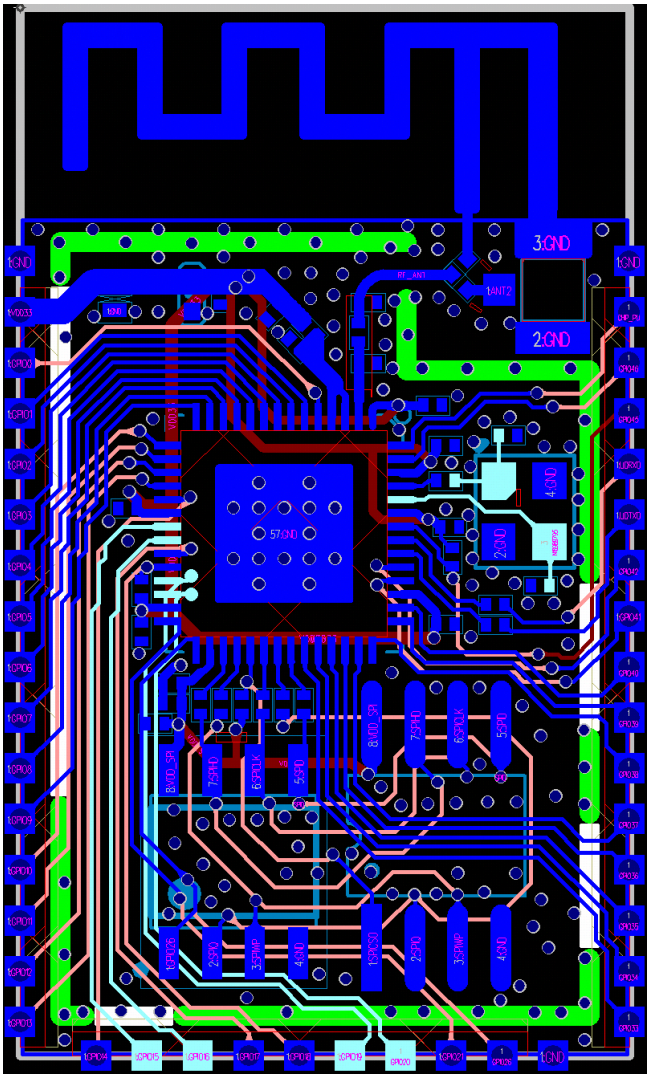

Figure 10: ESP32-S2 PCB Layout

3.1 General Principles of PCB Layout

We recommend a four-layer PCB design.

- The first layer is the TOP layer for signal traces and components.
- The second layer is the GND layer without signal traces being routed so as to ensure a complete GND plane.
- The third layer is the POWER layer where a GND plane should be applied to better isolate the RF and crystal

oscillator part. It is acceptable to route signal traces on this layer, provided that there is a complete GND plane under the RF and crystal oscillator.

- The fourth layer is the BOTTOM layer, where power traces are routed. Placing any components on this layer is not recommended.

Below are the suggestions for a two-layer PCB design.

- The first layer is the TOP layer for traces and components.
- The second layer is the BOTTOM layer. Please do not place any components on this layer and keep traces to a minimum. Ideally, it should be a complete GND plane.

3.2 Positioning an ESP32-S2 Module on a Base Board

If users adopt module-on-board design, they should pay attention to the layout of the module on the base board. The interference of the base board on the module's antenna performance should be minimized.

The module should be placed as close to the edge of the base board as possible. The PCB antenna area should be placed outside the base board whenever possible. In addition, the feed point of the antenna should be closest to the board, as Figure 11 shows.

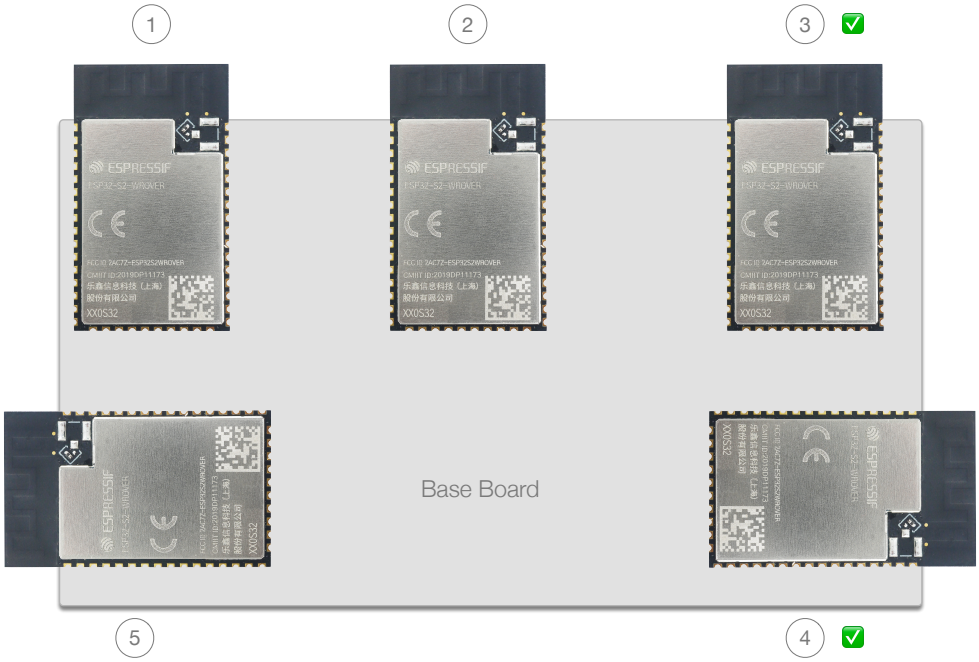

Figure 11: ESP32-S2 Module Antenna Position on Base Board

Note:

As is shown in Figure 11, the recommended position of ESP32-S2 module on the base board should be:

- Position 3, 4: Highly recommended;
- Position 1, 2, 5: Not recommended.

If the positions recommended are not feasible, please make sure that the module is not covered by any metal shell. Besides, the antenna area of the module and the area 15 mm outside the antenna should be kept clean, (namely no copper, routing, components on it) as shown in Figure 12.

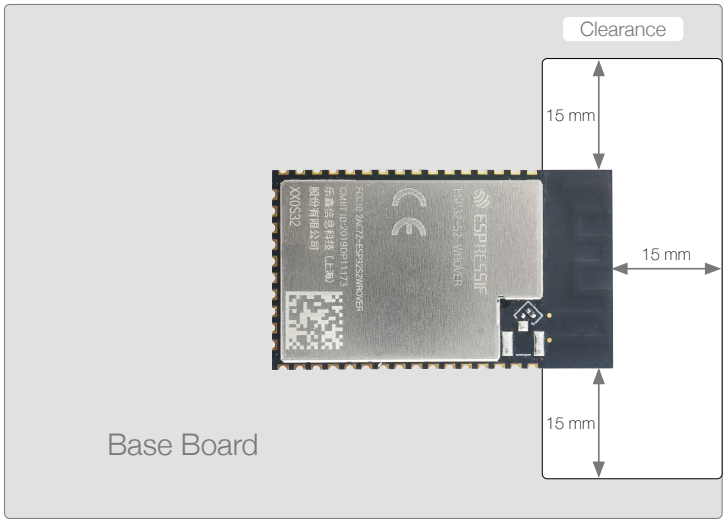

Figure 12: Keepout Zone for ESP32-S2 Module's Antenna on the Base Board

If there is base board under the antenna area, it is recommended to cut it off to minimize its impact on the antenna. When designing an end product, pay attention to the impact of enclosure on the antenna.

3.3 Power Supply

- Four-layer PCB design is recommended over two-layer design. Route the power traces on the fourth (bottom) layer whenever possible. Vias are required for the power traces to go through the layers and get connected to the pins on the top layer. There should be at least two vias if the main power traces need to cross layers. The drill diameter on other power traces should be no smaller than the width of the power traces.
- The 3.3 V power traces, highlighted in yellow, are routed as shown in Figure 13. The width of the main power traces should be at least 25 mil. The width of the power traces for pin3 and pin4 should be at least 20 mil. The width of other power traces is preferably 10 mil.
- As shown in Figure 13, an ESD protection diode is placed close to the power port (marked in red circle). A 10 µF capacitor is required before the power trace connects the ESP32-S2 chip, to be used in conjunction with a 0.1 µF capacitor. Then the power traces are divided into two ways from here and form a star-shape topology, thus reducing the coupling between different power pins. Note that all decoupling capacitors should be placed close to the power pin, and ground vias should be added adjacent to the ground pin for the decoupling capacitors to ensure a short return path.
- The power supply for the PA is provided by pin3 and pin4. It is required to add GND isolation between this power trace and the GPIO traces on the left, and place ground vias as much as possible.
- The ground pad at the bottom of the chip should be connected to the ground plane through at least nine ground vias.

Note:
If you need to add a thermal pad EPAD under the chip on the bottom of the module, it is recommended to employ a nine-grid on the EPAD, cover the gaps with ink, and place ground vias in the gaps, as shown in Figure 13. This can avoid tin leakage when soldering the module EPAD to the substrate.

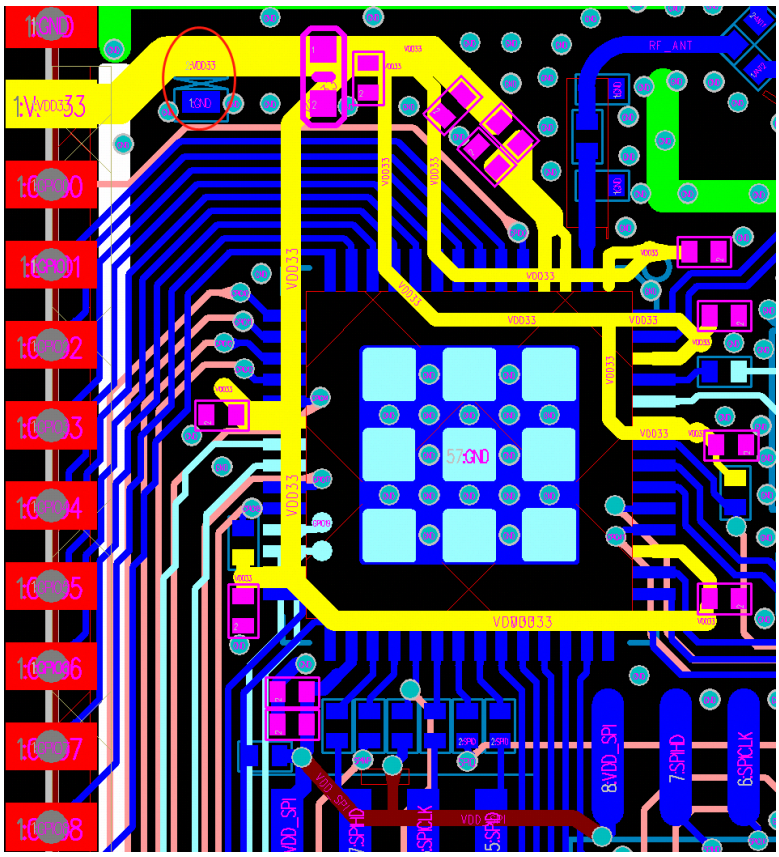

Figure 13: ESP32-S2 Power Traces in a Four-layer PCB Design

3.4 Crystal Oscillator

Figure 14 shows the reference design of the crystal oscillator. In addition, the following should be noted:

- The crystal oscillator should be placed far from the clock pin to avoid the interference on the chip. **The gap should be at least 2.0 mm**. It is good practice to add high-density ground via stitching around the clock trace for better isolation.
- There should be no vias for the clock input and output traces, which means the traces cannot cross layers.
- The external regulating capacitor should be placed on the near left or right side of the crystal oscillator, and at the end of the clock trace whenever possible, to make sure the ground pad of the capacitor is close to that of the crystal oscillator.
- Do not route high-frequency digital signal traces under the crystal oscillator. It is best not to route any signal trace under the crystal oscillator. The vias on the power traces on both sides of the crystal clock trace should be placed as far away from the clock trace as possible, and the two sides of the clock trace should be surrounded by grounding copper.
- As the crystal oscillator is a sensitive component, do not place any magnetic components nearby that may cause interference, for example large inductance component, and ensure that there is a clean large-area ground plane around the crystal oscillator.

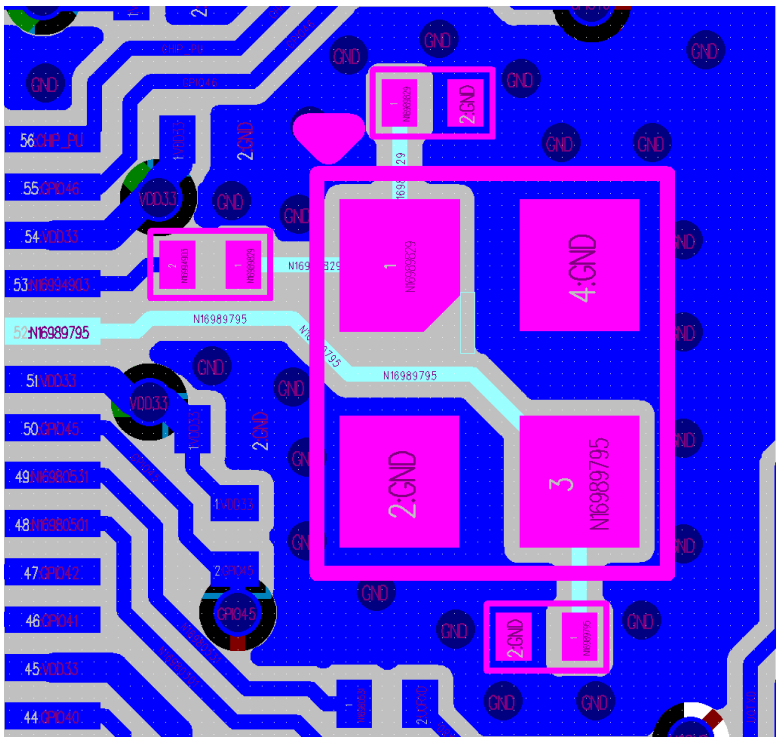

Figure 14: ESP32-S2 Crystal Oscillator Layout

3.5 RF

In a four-layer PCB design, the RF trace is routed as shown highlighted in pink in Figure 15.

- The RF trace should have 50 Ω single-ended characteristic impedance. The reference plane is the second layer. A π-type matching circuitry should be reserved on the RF trace and placed close to the chip.
- Make sure to keep the width of the RF trace consistent, and do not branch the trace. The RF trace should be as short as possible with dense ground via stitching around it for isolation.
- The RF trace should be routed on the outer layer without vias, i.e., should not cross layers. The RF trace should be routed at a 135° angle, or with circular arcs if trace bends are required.
- The ground plane on the adjacent layer needs to be complete. Do not route any traces under the RF trace whenever possible.
- There should be no high-frequency signal traces routed close to the RF trace. The RF antenna should be placed away from high-frequency transmitting devices, such as crystal oscillators, DDR, and clocks, etc. In addition, the USB port, USB-to-UART chip, UART signal lines (including traces, vias, test points, header pins, etc.) must be as far away from the antenna as possible. It is good practice to add ground vias around the UART signal line.
- When doing 50 Ω single-ended impedance control for the RF trace, please refer to the PCB stack-up design shown in Figure 16.

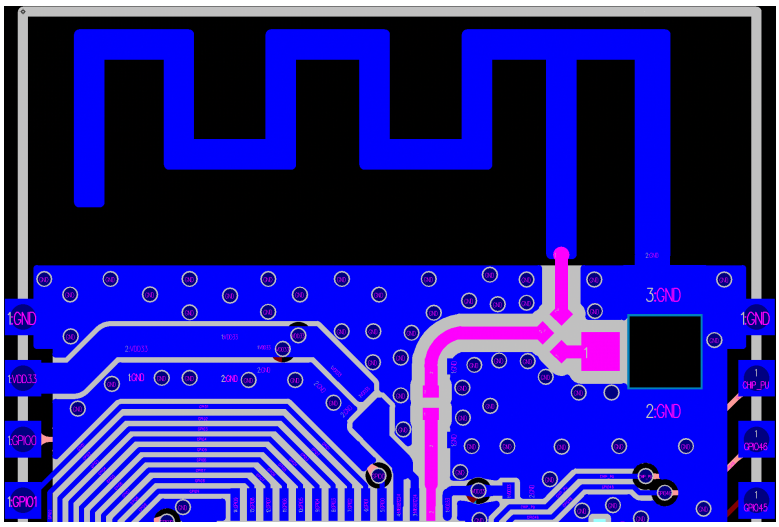

Figure 15: ESP32-S2 RF Layout in a Four-layer PCB Design

Thickness (mm)	Impedance (Ohm)	Gap (mil)	Width (mil)	Gap (mil)
-	50	12.2	12.6	12.2

Stack up	Material	Base copper (oz)	Thickness (mil)	DK
SM			0.4	4
L1_Top	Finished copper 1 oz	0.33	0.8	
PP	7628 TG150 RC50%		8	4.39
L2_Gnd		1	1.2	
Core	Core		Adjustable	4.43
L3_Power		1	1.2	
PP	7628 TG150 RC50%		8	4.39
L4_Bottom	Finished copper 1 oz	0.33	0.8	
SM			0.4	4

Figure 16: ESP32-S2 PCB Stack-up Design

3.6 Flash and PSRAM

Place the reserved serial resistor on the SPI communication line close to the chip side. Route the SPI traces on the inner layer (e.g., the third layer) whenever possible. Add ground vias around the clock and data traces of SPI separately. The layout of the flash and PSRAM on ESP32-S2 is shown in Figure 17.

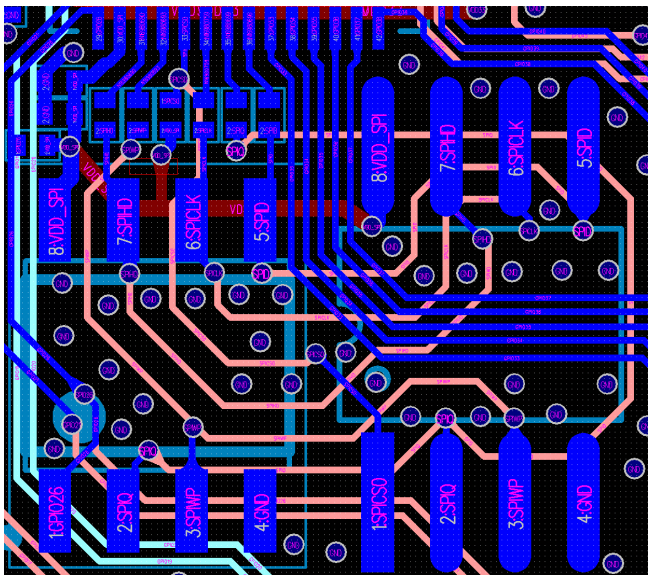

Figure 17: ESP32-S2 Flash and PSRAM Layout

3.7 UART

The series resistor on the U0TXD line needs to be placed as close to the chip and far from the crystal oscillator as possible. The U0TXD and U0RXD traces on the top layer should be as short as possible. Employ vias around the traces for isolation.

3.8 USB

Place the RC circuit reserved on the USB lines close to the chip. Route the USB traces on the inner layer (third layer) whenever possible. Please use differential routing and make each trace the same length. Make sure there is a complete reference ground plane. Note to surround the USB traces with ground copper.

3.9 Touch Sensor

ESP32-S2 offers up to 14 capacitive IOs that detect changes in capacitance on touch sensors due to finger contact or proximity. The chip's internal capacitance detection circuit features low noise and high sensitivity. It allows users to use touch pads with smaller area to implement the touch detection function. Users can also use the touch panel array to detect a larger area or more test points. Figure 18 depicts a typical touch sensor application.

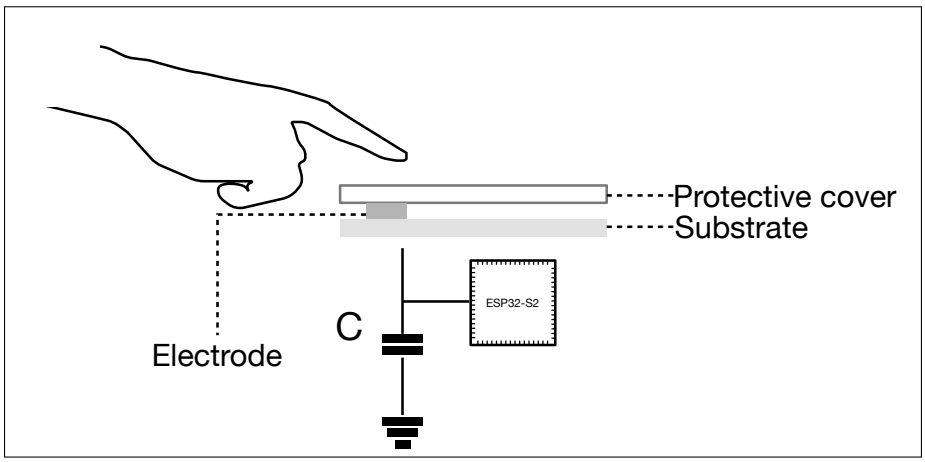

Figure 18: A Typical Touch Sensor Application

In order to prevent capacitive coupling and other electrical interference to the sensitivity of the touch sensor system, the following factors should be taken into account.

Electrode Pattern

The proper size and shape of an electrode improves system sensitivity. Round, oval, or shapes similar to a human fingertip is commonly applied. Large size or irregular shape might lead to incorrect responses from nearby electrodes.

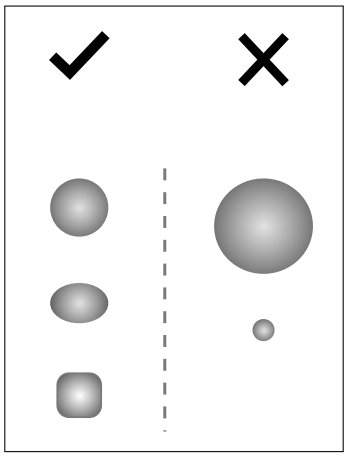

Figure 19: Electrode Pattern Requirements

Note:
The examples illustrated in Figure 19 are not of actual scale. It is suggested that users use a human fingertip as reference.

PCB Layout

The following are general guidelines to routing traces, as shown in Figure 20:

- The trace should be as short as possible and not exceed 300 mm.
- The trace width (W) can not be larger than 0.18 mm (7 mil).
- The alignment angle (R) should not be less than 90°.
- The trace-to-ground gap (S) should be in the range of 0.5 mm to 1 mm.

- The electrode diameter (D) should be in the range of 8 mm to 15 mm.
- Hatched ground should be added around the electrodes and traces.
- The traces should be isolated well and routed away from that of the antenna.

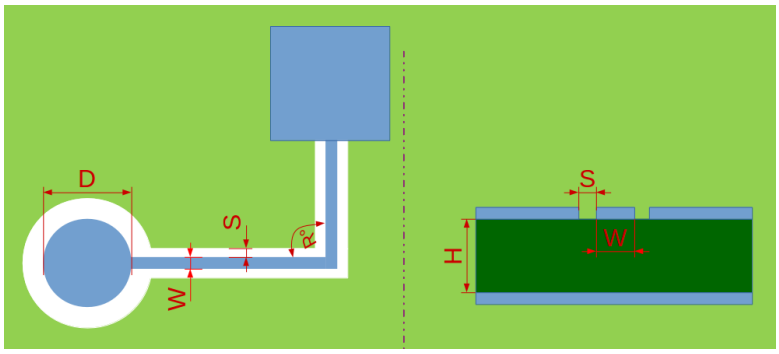

Figure 20: Sensor Track Routing Requirements

In addition, ESP32-S2 touch sensor adopts a waterproof design and features proximity sensor function. Figure 21 shows an example layout of a waterproof and proximity sensing design.

Note the following guidelines to better implement the above functions:

- It is recommended that the width of the shield electrode width is 2 cm.
- Employ a grid on the top layer with a trace width of 7 mil and a grid width of 45 mil (25% fill). The filled grid is connected to the driver shield signal.
- Employ a grid on the bottom layer with a trace width of 7 mil and a grid width of 70 mil (17% fill). The filled grid is connected to the driver shield signal.
- The protective sensor should be in a rectangle shape with curved edges and surround all other sensors.
- It is recommended that the width of the protective sensor is 2 mm.
- It is recommended that the gap between the protective sensor and shield sensor is 1 mm.
- The sensing distance of the proximity sensor is directly proportional to the area of the proximity sensor. However, increasing the sensing area will introduce larger noise. Actual testing is needed for optimized performance.
- It is recommended that the shape of the proximity sensor is a closed loop. The recommended width is 1.5 mm.

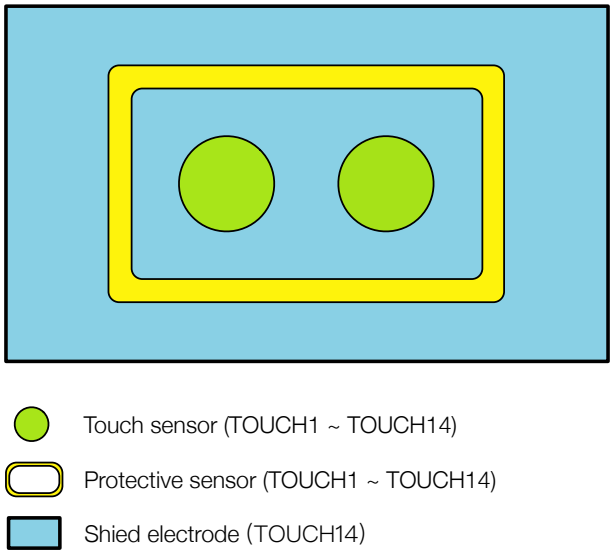

Figure 21: Shied Electrode and Protective Sensor

Note:
For more details on the hardware design of ESP32-S2 touch sensor, please refer to *Touch Sensor Application Note*.

3.10 Typical Layout Problems and Solutions

3.10.1 Q: The current ripple is not large, but the TX performance of RF is rather poor.

Analysis:

The current ripple has a strong impact on the RF TX performance. It should be noted that the ripple must be tested when ESP32-S2 is in the normal working mode. The ripple increases when the power gets high in a different mode.

Generally, the peak-to-peak value of the ripple should be <80 mV when ESP32-S2 sends MCS7@11n packets, and <120 mV when ESP32-S2 sends 11m@11b packets.

Solution:

Add a 10 μF filter capacitor to the branch of the power trace (the branch powering the ESP32-S2 analog power pin). The 10 μF capacitor should be as close to the analog power pin as possible for small and stable current ripples.

3.10.2 Q: The power ripple is small, but RF TX performance is poor.

Analysis:

The RF TX performance can be affected not only by power ripples, but also by the crystal oscillator itself. Poor quality and big frequency offsets of the crystal oscillator decrease the RF TX performance. The crystal oscillator clock may be corrupted by other interfering signals, such as high-speed output or input signals. In addition, high-frequency signal traces, such as the UART trace under the crystal oscillator, could also result in the malfunction of the crystal oscillator. Besides, sensitive components or radiation components, such as inductors and antennas, may also decrease the RF performance.

Solution:

This problem is caused by improper layout and can be solved by re-layout. Please see Section 3 for details.

3.10.3 Q: When ESP32-S2 sends data packages, the power value is much higher or lower than the target power value, and the EVM is relatively poor.

Analysis:

The disparity between the tested value and the target value may be due to signal reflection caused by the impedance mismatch on the transmission line connecting the RF pin and the antenna. Besides, the impedance mismatch will affect the working state of the internal PA, making the PA prematurely access the saturated region in an abnormal way. The EVM becomes poor as the signal distortion happens.

Solution:

Match the antenna's impedance with the reserved π-type circuit on the RF trace, so that impedance of the antenna as seen from the RF pin matches closely with that of the chip. This reduces reflections to the minimum.

3.10.4 Q: TX performance is not bad, but the RX sensitivity is low.

Analysis:

Good TX performance indicates proper RF impedance matching. External coupling to the antenna can affect the RX performance. For instance, the crystal oscillator signal harmonics could couple to the antenna. If the TX and RX traces of UART cross over with RF trace, then, they will affect the RX performance, as well. If there are many high-frequency interference sources on the board, signal integrity should be considered.

Solution:

Keep the antenna away from crystal oscillators. Do not route high-frequency signal traces close to the RF trace. Please see Section 3 for details.

4. Hardware Development

Espressif designs and manufactures a large variety of modules and boards to help users evaluate functionality of the ESP32-S2 chip.

4.1 ESP32-S2 Modules

For a list of ESP32-S2 modules please check Modules section of Espressif website.

To review module reference designs please check Documentation section of Espressif website.

Notes on Using Modules

- The module uses one single pin as the power supply pin. Users can connect the module to a 3.3 V power supply that can drive at least 500 mA output current. The 3.3 V power supply works both for the analog circuit and the digital circuit.
- The EN pin is used for enabling the module. Set the EN pin high for normal working mode. There is no RC delay circuit on the module. It is recommended that users add an external RC delay circuit to the module. For details please refer to Section 2.2.
- Lead the GND, RXD, TXD pins out and connect them to a USB-to-UART tool for firmware download, log-printing and communication.

By default, the initial firmware has already been downloaded in the flash. If users need to re-download the firmware, they should follow the steps below:

1. Set the module to UART Download mode by pulling IO0 (pulled up by default) and IO46 (pulled down by default) low.
2. Power on the module and check through the serial terminal if the UART Download mode is enabled.
3. Download the firmware to flash, using the Flash Download Tool.
4. After downloading, pull IO0 high and enable the SPI Boot mode.
5. Power on the module again. The chip will read and execute the firmware during initialization.

Notice:

- During the whole process, users can check the status of the chip with the log printed through UART. If the firmware cannot be downloaded or executed, users can check if the working mode is normal during the chip initialization by looking at the log.
- The serial tool cannot be used for both the log-print and flash-download tools simultaneously.

4.2 ESP32-S2 Development Boards

For a list of the latest designs of ESP32-S2 boards please check Development Boards section of Espressif website.

Revision History

Date	Version	Release notes
2020-11-18	V1.1	Updated the capacitance of RC circuit to 1 μF in 2.2.1.
2020-05-07	V1.0	First release.