APPENDIX SUMMARY

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Appendix I: SSD1320 Command Descriptions

1 COMMAND DESCRIPTIONS

1.1 Fundamental Command

1.1.1 Set Memory Addressing Mode (20h)

There are 2 different memory addressing mode in SSD1320: horizontal addressing mode and vertical addressing mode. This command sets the way of memory addressing into one of the above two modes.

1.1.2 Set Column Address (21h)

This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

1.1.3 Set Row Address (22h)

This triple byte command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. If vertical address increment mode is enabled, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address.

1.1.4 Set Portrait Addressing Mode (25h)

This double byte command sets the way of memory addressing into portrait addressing mode or the normal (original) addressing mode. Horizontal or vertical addressing mode can be set on top of it by command 20h.

1.1.5 Set Contrast Control (81h)

This double byte command sets the Contrast Setting of the display, with a valid range from 01h to FFh. The segment output current increases as the contrast step value increases, which results in brighter display.

1.1.6 Set Segment Re-map (A0h/A1h)

This command changes the mapping between the display data column address and the segment driver. It allows flexibility in OLED module design.

This command only affects subsequent data input. Data already stored in GDDRAM will have no change.

1.1.7 Set Display Start Line (A2h)

This double byte command sets the Display Start Line register to determine starting address of display RAM, by selecting a value from 0 to 159. With value equal to 0, RAM row 0 is mapped to COM0. With value equal to 1, RAM row 1 is mapped to COM0 and so on.

1.1.8 Set Display Mode (A4h/A5h/A6h/A7h)

These are single byte commands and are used to set display status to Normal Display, Entire Display ON, Entire Display OFF or Inverse Display, respectively.

- Normal Display (A4h)
  Reset the "Entire Display ON" effect and turn the data to ON at the corresponding gray level. Figure 1-1 shows an example of Normal Display.

Figure 1-1: Example of Normal Display

Memory Display

- Set Entire Display ON (A5h)
  Force the entire display to be at gray scale level GS15, regardless of the contents of the display data RAM, as shown on Figure 1-2.

Figure 1-2: Example of Entire Display ON

Memory Display

- Normal Display (A6h)
  Reset the "Inverse Display" effect and turn the data to ON at the corresponding gray level. Figure 1-3 shows an example of Normal Display.

Figure 1-3: Example of Normal Display

Memory Display

- Inverse Display (A7h)
  The gray scale level of display data are swapped such that "GS0" ↔ "GS15", "GS1" ↔ "GS14", etc. Figure 1-4 shows an example of inverse display.

Figure 1-4: Example of Inverse Display

Memory Display

1.1.9 Set Multiplex Ratio (A8h)

This command switches the default 160 multiplex mode to any multiplex ratio, ranging from 16 to 160. The output pads COM0~COM159 will be switched to the corresponding COM signal.

1.1.10 External or internal IREF Selection (ADh)

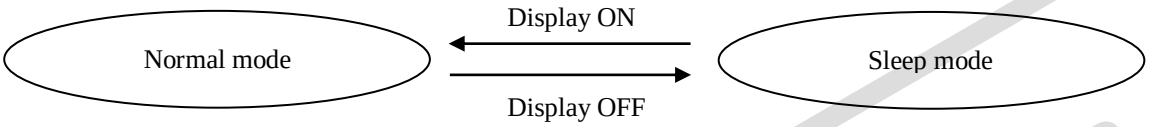
This double byte command supports External or Internal I_{REF} Selection.

1.1.11 Set Display ON/OFF (AEh/AFh)

These single byte commands are used to turn the OLED panel display ON or OFF.
When the display is ON, the selected circuits by Set Master Configuration command will be turned ON.
When the display is OFF, those circuits will be turned OFF and the segment and common output are in V_{SS} state and high impedance state, respectively. These commands set the display to one of the two states:

- Display OFF
- Display ON

Figure 1-5 : Transition between different modes



1.1.12 Set Pre-charge voltage (BCh)

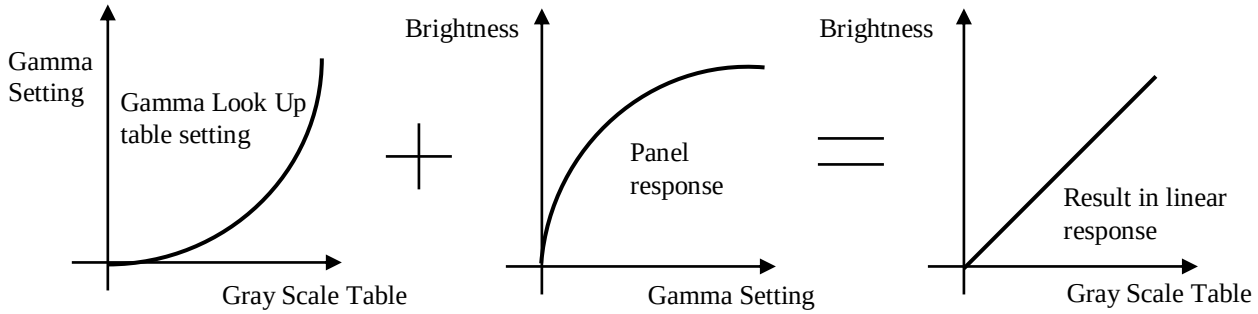
This double byte command sets the first pre-charge voltage (phase 2) level of segment pins. The level of pre-charge voltage is programmed with reference to V_{CC}.

1.1.13 Set Gray Scale Table (BEh)

This command is used to set each individual gray scale level for the display. Except gray scale levels GS0 that has no pre-charge and current drive, each gray scale level is programmed in the length of current drive stage pulse width with unit of DCLK. The longer the length of the pulse width, the brighter the OLED pixel when it's turned ON. Following the command BEh, the user has to set the gray scale setting for GS1, GS2, …, GS14, GS15 one by one in sequence.

The setting of gray scale table entry can perform gamma correction on OLED panel display. Since the perception of the brightness scale shall match the image data value in display data RAM, appropriate gray scale table setting like the example shown below (Figure 1-6) can compensate this effect.

Figure 1-6 : Example of Gamma correction by Gamma Look Up table setting



1.1.14 Select Default Linear Gray Scale Table (BFh)

This single byte command reloads the preset linear Gray Scale table as GS0 =Gamma Setting 0, GS1 = Gamma Setting 4, GS2 = Gamma Setting 8, ..., GS14 = Gamma Setting 56, GS15 = Gamma Setting 60.

1.1.15 Set COM Output Scan Direction (C0h/C8h)

This command sets the scan direction of the COM output, allowing layout flexibility in the OLED module design. Additionally, the display will show once this command is issued. For example, if this command is sent during normal display then the graphic display will be vertically flipped immediately.

1.1.16 Set Display Offset (D3h)

This double byte command specifies the mapping of display start line to one of COM0~COM159 (assuming that COM0 is the display start line, display start line register equals to 0).

1.1.17 Set Display Clock Divide Ratio / Oscillator Frequency (D5h)

This command consists of two functions:

- Display Clock Divide Ratio (D) (A[3:0])
  Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 256, with reset value = 0001b.

- Oscillator Frequency (A[7:4])
  Program the oscillator frequency Fosc that is the source of CLK if CLS pin is pulled high. The 4-bit value results in 16 different frequency settings being available.

1.1.18 Set Phase Length (D9h)

This double byte command sets the length of phase 1 and 2 of segment waveform of the driver.

- Phase 1 (A[3:0]): Set the period for Phase 1 in the unit of DCLK. A larger capacitance of the OLED pixel may require longer period to discharge the previous data charge completely.

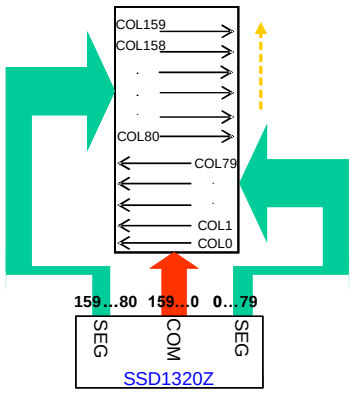
- Phase 2 (A[7:4]): Set the period for Phase 2 in the unit of DCLKs. A longer period is needed to charge up a larger capacitance of the OLED pixel to the target voltage V_P.

1.1.19 Set SEG Pins Hardware Configuration (DAh)

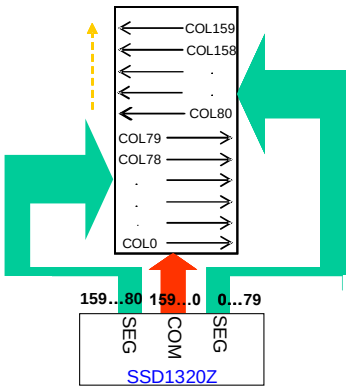
This command sets the SEG signals pin configuration to match the OLED panel hardware layout. SEG Odd / Even (Left / Right) and Top / Bottom connections are software selectable, thus there are total of 8 cases and they are shown on the followings:

Table 1-1: SEG Pins Hardware Configuration

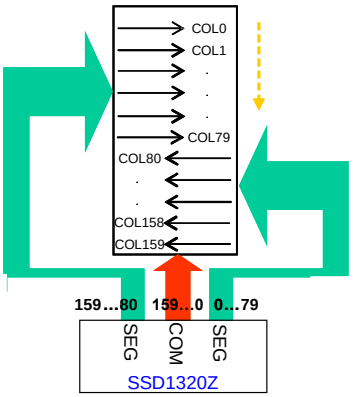
Case no.	Oddeven (1) / Sequential (0)	SEG Remap (0 disable, 1 enable)	Left / Right Swap	Remark
1	0	0	0	
2	0	0	1	
3	0	1	0	
4	0	1	1	
5	1	0	0	Default
6	1	0	1	
7	1	1	0	
8	1	1	1	



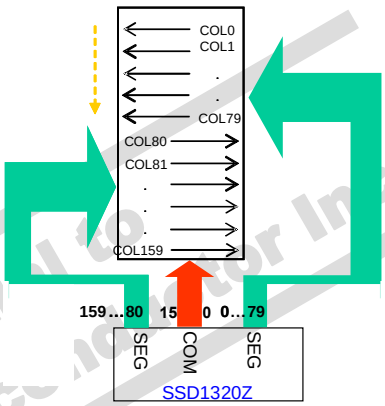
(1) Sequential SEG



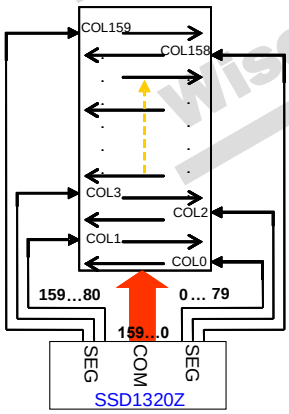
(2) Sequential SEG & left / right swap



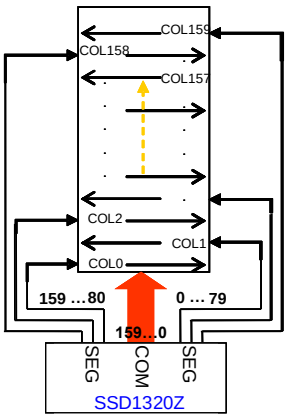
(3) Sequential SEG & SEG remap (with nibble remap)



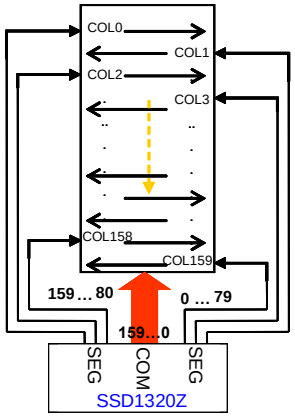
(4) Sequential SEG & SEG remap (with nibble remap) & left / right swap



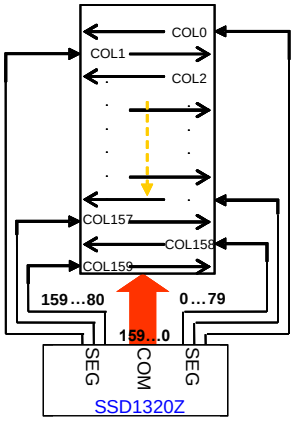
(5) Odd / even SEG



(6) Odd / even SEG & left / right swap



(7) Odd / even SEG & SEG remap (with nibble remap)



(8) Odd / even SEG & SEG remap (with nibble remap) & left / right swap

Note:

(1) The above eight figures are all with bump pads being faced up.

1.1.20 Set VCOMH Deselect Level (DBh)

This double byte command adjusts the VCOMH regulator output.

1.1.21 Set Command Lock (FDh)

This double byte command is used to lock the OLED driver IC from accepting any command except itself. After entering the "Lock" state, the OLED driver IC will not respond to any newly-entered command (except the register for unlocking it) and there will be no memory access. That means the OLED driver IC ignore all the commands (except the register for unlocking it) during the "Lock" state.

In the "Unlock" state, the driver IC resumes from the "Lock" state, and the driver IC will then respond to the command and memory access.

Appendix II: SSD1320 Command Table

1 COMMAND TABLE

Table 1-1: SSD1320 Command Table

(D/C#=0, R/W#(WR#) = 0, E(RD#=1) unless specific setting is stated)

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0	20 A[0]	0 *	0 *	1 *	0 *	0 *	0 *	0 0	0 A_0	Set Memory Addressing Mode	A[0] = 0b, Horizontal Addressing Mode A[0] = 1b, Vertical Addressing Mode
0 0 0	21 A[7:0] B[7:0]	0 A_7 B_7	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Setup column start and end address A[7:0] : Column start address, range : 0-79d, (RESET=0d) B[7:0]: Column end address, range : 0-79d, (RESET =79d)
0 0 0	22 A[7:0] B[7:0]	0 A_7 B_7	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	1 A_1 B_1	0 A_0 B_0	Set Row Address	Setup page start and end address A[7:0] : Row start address, range : 0-159d, (RESET=0d) B[7:0]: Row end address, range : 0-159d, (RESET =159d)
0 0	25 A[0]	0 *	0 *	1 *	0 *	0 *	1 *	0 0	1 A_0	Set Portrait Addressing Mode	A[0] = 0b, Normal Addressing Mode A[0] = 1b, Portrait Addressing Mode
0	A0/A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET) A1h, X[0]=1b: column address 79 is mapped to SEG0
0 0	A2 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Start Line	Set display RAM display start line register from 0-159 by A[7:0] (RESET=00h) **Note** (1) In command A2h, A[6:0] from 00h to 3Fh has the same effect as command 40h-7Fh.
0	A4/A5	1	0	1	0	0	1	0	X_0	Entire Display ON	A4h, X_0=0b: Resume to RAM content display (RESET) Output follows RAM content A5h, X_0=1b: Entire display ON Output ignores RAM content

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	A6/A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	A6h, X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel A7h, X[0]=1b: Inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0 0	A8 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[7:0] : from 16MUX to 160MUX. RESET = 1001 1111b (i.e. 159d, 160MUX) A[7:0] from 0 to 14 are invalid entry
0 0	AD A[4]	1 0	0 0	1 0	0 A_4	1 0	1 0	0 0	1 0	External or internal I_{REF} Selection	Select external or internal I_{REF}: A[4] = '0' Select external I_{REF} (RESET) A[4] = '1' Enable internal I_{REF} during display ON
0	AE/AF	1	0	1	0	1	1	1	X_0	Set Display ON/OFF	AEh, X[0]=0b: Display OFF (sleep mode) (RESET) AFh X[0]=1b: Display ON in normal mode
0	BC A[4:0]	1 *	0 *	1 *	1 A_4	1 A_3	1 A_2	0 A_1	0 A_0	Set Pre-charge voltage	Set pre-charge voltage level.[reset = 11110b] A[4:0] | Hex code | pre-charge voltage 00000 | 00h | 0.10 x V_{CC} : | : | : 11110 | 1Eh | 0.50 x V_{CC} [reset] 11111 | 1Fh | 0.5133 x V_{CC} **Note** (1)Pre-charge voltage level must be smaller than COM deselect voltage level
0 0 0 … … … 0 0	BE A1[6:0] A2[6:0] … … … A14[6:0] A15[6:0]	1 * * … … … * *	0 $A1_6$ $A2_6$ … … … $A14_6$ $A15_6$	1 $A1_5$ $A2_5$ … … … $A14_5$ $A15_5$	1 $A1_4$ $A2_4$ … … … $A14_4$ $A15_4$	1 $A1_3$ $A2_3$ … … … $A14_3$ $A15_3$	1 $A1_2$ $A2_2$ … … … $A14_2$ $A15_2$	1 $A1_1$ $A2_1$ … … … $A14_1$ $A15_1$	0 $A1_0$ $A2_0$ … … … $A14_0$ $A15_0$	Set Gray Scale Table	The next 15 data bytes set the gray scale pulse width in unit of DCLK's. A1[6:0], value for GS1 level Pulse width A2[6:0], value for GS2 level Pulse width … A14[6:0], value for GS14 level Pulse width A15[6:0], value for GS15 level Pulse width **Note** (1) The pulse width value of GS1, GS2, ... , GS15 should not be equal. i.e. 0<GS1<GS2 … <GS15 (2) GS15 level pulse width must be set larger than the period of phase 1 + phase 2

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	BF	1	0	1	1	1	1	1	1	Linear LUT	The default Linear Gray Scale table is set in unit of DCLK's as follow GS0 level pulse width = 0; GS1 level pulse width = 4 GS2 level pulse width = 8; GS3 level pulse width = 12; : : GS14 level pulse width = 56; GS15 level pulse width = 60
0	C0/C8	1	1	0	0	X_3	0	0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N –1] C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0 Where N is the Multiplex ratio.
0 0	D3 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Display Offset	Set vertical shift by COM from 0d~159d (RESET=0d)
0 0	D5 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	0 A_3	1 A_2	0 A_1	1 A_0	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0]: Define divide ratio (D) of display clock (DCLK) (i.e. 1, 2, 4, 8…256) (RESET is 0001b, i.e. divide ratio = 2) A[7:4] : Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. (RESET is 0100b) Range: 0000b~1111b.
0 0	D9 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	1 A_3	0 A_2	0 A_1	1 A_0	Set Phase Length	A[3:0] : Phase 1 period of up to 15 DCLK Clock 0 is invalid entry (RESET=2h) A[7:4] : Phase 2 period of up to 15 DCLK Clock 0 is invalid entry (RESET=7h)
0 0	DA A[5:4]	1 0	1 0	0 A_5	1 A_4	1 0	0 0	1 1	0 0	Set SEG Pins Hardware Configuration	A[4]=0b, Sequential SEG pin configuration A[4]=1b (RESET), Alternative (odd/even) SEG pin configuration A[5]=0b (RESET), Disable SEG Left/Right remap A[5]=1b, Enable SEG Left/Right remap
0 0	DB A[2:0]	1 0	0 0	1 0	1 0	1 0	0 A_2	1 A_1	1 A_0	Set V_{COMH}	Set COM deselect voltage level. **A[5:3] / Hex code / V_{COMH} deselect level** 000b / 00h / ~ 0.72 x V_{CC} 010b / 10h / ~ 0.76 x V_{CC} 100b / 20h / ~ 0.80 x V_{CC} (RESET) 110b / 30h / ~ 0.84 x V_{CC}

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	FD	1	1	1	1	1	1	0	1	Set Command Lock	A[2]: MCU protection status. A[2] = 0b, Unlock OLED driver IC MCU interface from entering command (RESET) A[2] = 1b, Lock OLED driver IC MCU interface from entering command **Note** (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command
0	A[2]	0	0	0	1	0	A_2	1	0		

Appendix IV: SSD1320 Display Enhancement

1 COMMAND DESCRIPTIONS

1.1 Display Enhancement (D8h)

The low Greyscale display quality would be improved by this command.

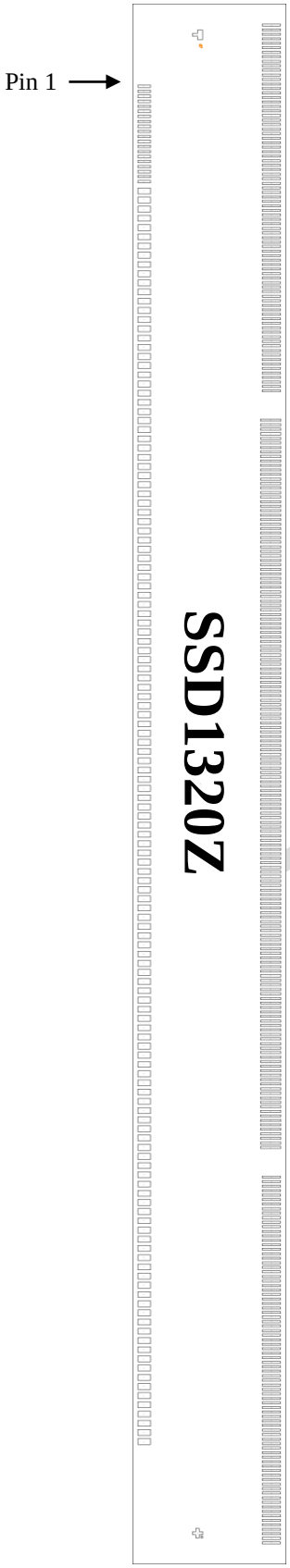
2 COMMAND TABLE

Table 2-1 : Command Table for Display Enhancement

Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	D8	1	1	0	1	1	0	0	0	Display Enhancement	A[5] = 0b: Enhanced low GS display quality
0	A[5]	1	1	A_5	1	0	1	0	1		A[5] = 1b: Normal [reset]

Appendix V: SSD1320Z Die Pad Floor Plan

Figure 1: – SSD1320Z Die drawing

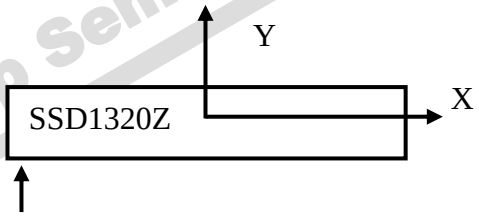


Die size	9.33mm +/- 0.05mm x 0.80mm+/- 0.05mm
Die thickness	250 +/- 15um
Min I/O pad pitch	30um
Min SEG pad pitch	27um
Min COM pad pitch	27um
Bump height	Nominal 9 um

Bump size		
Pad#	X[um]	Y[um]
1-20	15	67
20-157	35	67
158-239, 402-483	12	100
240-401	12	110

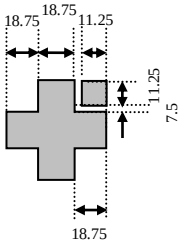
Alignment mark	Size
+ shape	56.25um x 56.25um
T shape	56.25um x 56.25um

(For details dimension please see Figure 2)

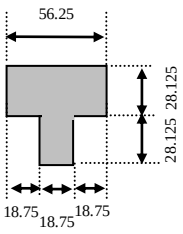


Pad 1,2,3,…->483
Gold Bumps face up

Figure 2: SSD1320Z alignment mark dimension



Size: 56.25 x 56.25 μm²



Size: 56.25 x 56.25 μm²

Appendix VI: SSD1320 Bump Die Pad Coordinates

Table 1 : SSD1320Z Pin Assignment

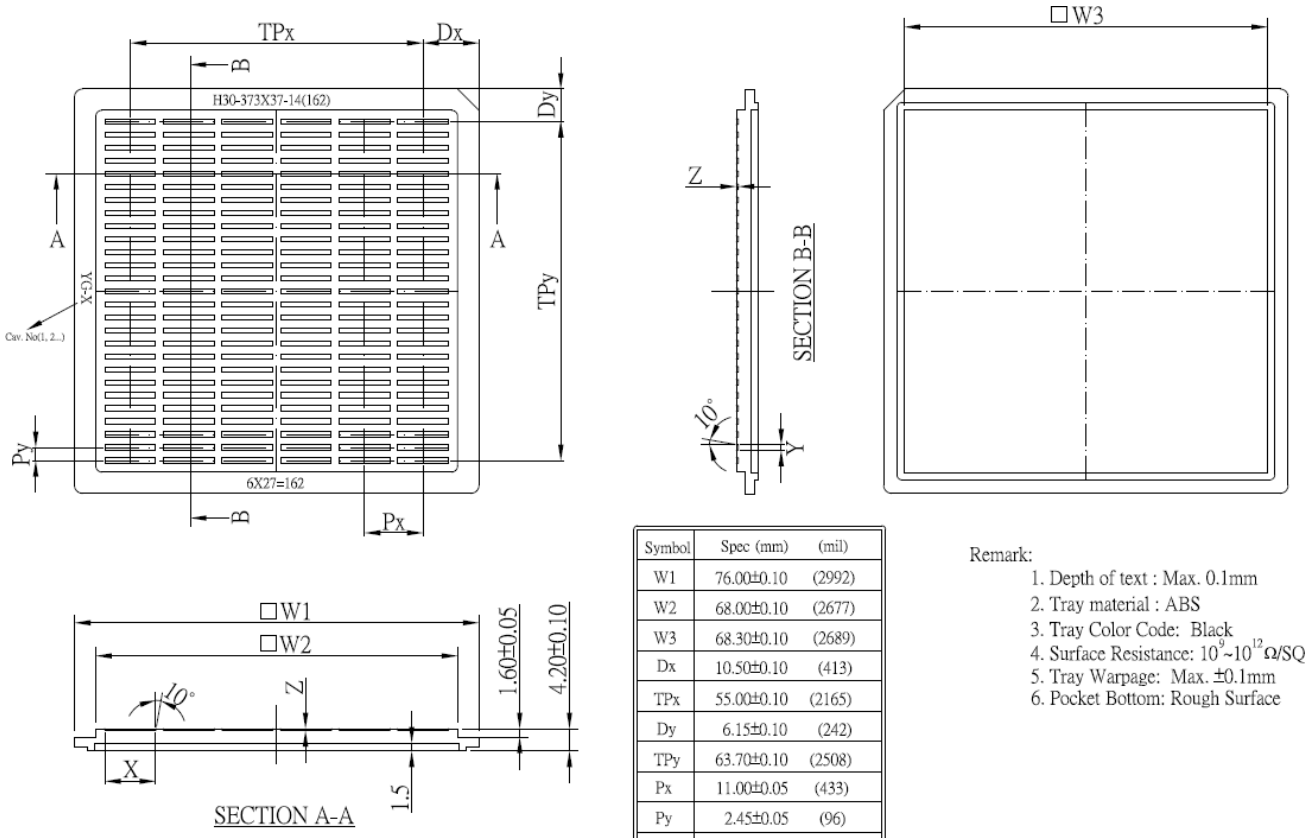
Pin number	Pin name	X	Y
1	VSS	-4172.5	-338.5
2	TP0	-4142.5	-338.5
3	TP1	-4112.5	-338.5
4	TP2	-4082.5	-338.5
5	TP3	-4052.5	-338.5
6	TP4	-4022.5	-338.5
7	TP5	-3992.5	-338.5
8	VSS	-3962.5	-338.5
9	TP6	-3932.5	-338.5
10	TP7	-3902.5	-338.5
11	TP8	-3872.5	-338.5
12	TP9	-3842.5	-338.5
13	TP10	-3812.5	-338.5
14	TP11	-3782.5	-338.5
15	VSS	-3752.5	-338.5
16	TP12	-3722.5	-338.5
17	TP13	-3692.5	-338.5
18	TP14	-3662.5	-338.5
19	TP15	-3632.5	-338.5
20	VSS	-3602.5	-338.5
21	NC	-3547.5	-338.5
22	NC	-3492.5	-338.5
23	NC	-3437.5	-338.5
24	NC	-3382.5	-338.5
25	VCC	-3327.5	-338.5
26	VCC	-3272.5	-338.5
27	VCC	-3217.5	-338.5
28	VCC	-3162.5	-338.5
29	VCC	-3107.5	-338.5
30	VCC	-3052.5	-338.5
31	VCC	-2997.5	-338.5
32	VCC	-2942.5	-338.5
33	VCOMH	-2887.5	-338.5
34	VCOMH	-2832.5	-338.5
35	VCOMH	-2777.5	-338.5
36	VCOMH	-2722.5	-338.5
37	VCOMH	-2667.5	-338.5
38	VCOMH	-2612.5	-338.5
39	VCOMH	-2557.5	-338.5
40	VCOMH	-2502.5	-338.5
41	NC	-2447.5	-338.5
42	VDD	-2392.5	-338.5
43	VDD	-2337.5	-338.5
44	VDD	-2282.5	-338.5
45	VID0	-2227.5	-338.5
46	VID0	-2172.5	-338.5
47	VID0	-2117.5	-338.5
48	VID0	-2062.5	-338.5
49	VSS	-2007.5	-338.5
50	VSS	-1952.5	-338.5
51	VSS	-1897.5	-338.5
52	VSS	-1842.5	-338.5
53	VID1	-1787.5	-338.5
54	VID1	-1732.5	-338.5
55	VID1	-1677.5	-338.5
56	VID1	-1622.5	-338.5
57	VDD	-1567.5	-338.5
58	VDD	-1512.5	-338.5
59	VDD	-1457.5	-338.5
60	VDD	-1402.5	-338.5
61	VDD	-1347.5	-338.5
62	VDD	-1292.5	-338.5
63	VDD	-1237.5	-338.5
64	NC	-1182.5	-338.5
65	VSL	-1127.5	-338.5
66	VSL	-1072.5	-338.5
67	VSL	-1017.5	-338.5
68	VLSS	-962.5	-338.5
69	VLSS	-907.5	-338.5
70	VLSS	-852.5	-338.5
71	VLSS	-797.5	-338.5
72	VLSS	-742.5	-338.5
73	VLSS	-687.5	-338.5
74	VLSS	-632.5	-338.5
75	VLSS	-577.5	-338.5
76	NC	-522.5	-338.5
77	VP	-467.5	-338.5
78	VP	-412.5	-338.5
79	VP	-357.5	-338.5
80	VP	-302.5	-338.5
81	VP	-247.5	-338.5
82	VP	-192.5	-338.5
83	NC	-137.5	-338.5
84	VDD	-82.5	-338.5
85	VDD	-27.5	-338.5
86	VDD	27.5	-338.5
87	VDD	82.5	-338.5
88	FR	137.5	-338.5
89	VSS	192.5	-338.5
90	CS#	247.5	-338.5
91	RES#	302.5	-338.5
92	NC	357.5	-338.5
93	D/C	412.5	-338.5
94	R/W#(WR#)	467.5	-338.5
95	VSS	522.5	-338.5
96	E(RD#)	577.5	-338.5
97	NC	632.5	-338.5
98	D0	687.5	-338.5
99	NC	742.5	-338.5
100	D1	797.5	-338.5
101	D2	852.5	-338.5
102	NC	907.5	-338.5
103	D3	962.5	-338.5
104	VSS	1017.5	-338.5
105	VSS	1072.5	-338.5
106	D4	1127.5	-338.5
107	NC	1182.5	-338.5
108	D5	1237.5	-338.5
109	D6	1292.5	-338.5
110	NC	1347.5	-338.5
111	D7	1402.5	-338.5
112	CL	1457.5	-338.5
113	VSS	1512.5	-338.5
114	CLS	1567.5	-338.5
115	VDD	1622.5	-338.5
116	VDD	1677.5	-338.5
117	BS0	1732.5	-338.5
118	VSS	1787.5	-338.5
119	BS1	1842.5	-338.5
120	VDD	1897.5	-338.5
121	BS2	1952.5	-338.5
122	VSS	2007.5	-338.5
123	VSS	2062.5	-338.5
124	VSS	2117.5	-338.5
125	BGGND	2172.5	-338.5
126	VBREF	2227.5	-338.5
127	VLSS	2282.5	-338.5
128	VLSS	2337.5	-338.5
129	VLSS	2392.5	-338.5
130	VLSS	2447.5	-338.5
131	VLSS	2502.5	-338.5
132	VLSS	2557.5	-338.5
133	VLSS	2612.5	-338.5
134	VLSS	2667.5	-338.5
135	VSL	2722.5	-338.5
136	VSL	2777.5	-338.5
137	VSL	2832.5	-338.5
138	IREF	2887.5	-338.5
139	VCOMH	2942.5	-338.5
140	VCOMH	2997.5	-338.5
141	VCOMH	3052.5	-338.5
142	VCOMH	3107.5	-338.5
143	VCOMH	3162.5	-338.5
144	VCOMH	3217.5	-338.5
145	VCOMH	3272.5	-338.5
146	VCOMH	3327.5	-338.5
147	VCC	3382.5	-338.5
148	VCC	3437.5	-338.5
149	VCC	3492.5	-338.5
150	VCC	3547.5	-338.5
151	VCC	3602.5	-338.5
152	VCC	3657.5	-338.5
153	VCC	3712.5	-338.5
154	VCC	3767.5	-338.5
155	T1	3822.5	-338.5
156	T0	3877.5	-338.5
157	NC	3932.5	-338.5
158	NC	4537.5	322
159	SEG79	4510.5	322
160	SEG78	4483.5	322
161	SEG77	4456.5	322
162	SEG76	4429.5	322
163	SEG75	4402.5	322
164	SEG74	4375.5	322
165	SEG73	4348.5	322
166	SEG72	4321.5	322
167	SEG71	4294.5	322
168	SEG70	4267.5	322
169	SEG69	4240.5	322
170	SEG68	4213.5	322
171	SEG67	4186.5	322
172	SEG66	4159.5	322
173	SEG65	4132.5	322
174	SEG64	4105.5	322
175	SEG63	4078.5	322
176	SEG62	4051.5	322
177	SEG61	4024.5	322
178	SEG60	3997.5	322
179	SEG59	3970.5	322
180	SEG58	3943.5	322
181	SEG57	3916.5	322
182	SEG56	3889.5	322
183	SEG55	3862.5	322
184	SEG54	3835.5	322
185	SEG53	3808.5	322
186	SEG52	3781.5	322
187	SEG51	3754.5	322
188	SEG50	3727.5	322
189	SEG49	3700.5	322
190	SEG48	3673.5	322
191	SEG47	3646.5	322
192	SEG46	3619.5	322
193	SEG45	3592.5	322
194	SEG44	3565.5	322
195	SEG43	3538.5	322
196	SEG42	3511.5	322
197	SEG41	3484.5	322
198	SEG40	3457.5	322
199	SEG39	3430.5	322
200	SEG38	3403.5	322
201	SEG37	3376.5	322
202	SEG36	3349.5	322
203	SEG35	3322.5	322
204	SEG34	3295.5	322
205	SEG33	3268.5	322
206	SEG32	3241.5	322
207	SEG31	3214.5	322
208	SEG30	3187.5	322
209	SEG29	3160.5	322
210	SEG28	3133.5	322
211	SEG27	3106.5	322
212	SEG26	3079.5	322
213	SEG25	3052.5	322
214	SEG24	3025.5	322
215	SEG23	2998.5	322
216	SEG22	2971.5	322
217	SEG21	2944.5	322
218	SEG20	2917.5	322
219	SEG19	2890.5	322
220	SEG18	2863.5	322
221	SEG17	2836.5	322
222	SEG16	2809.5	322
223	SEG15	2782.5	322
224	SEG14	2755.5	322
225	SEG13	2728.5	322
226	SEG12	2701.5	322
227	SEG11	2674.5	322
228	SEG10	2647.5	322
229	SEG9	2620.5	322
230	SEG8	2593.5	322
231	SEG7	2566.5	322
232	SEG6	2539.5	322
233	SEG5	2512.5	322
234	SEG4	2485.5	322
235	SEG3	2458.5	322
236	SEG2	2431.5	322
237	SEG1	2404.5	322
238	SEG0	2377.5	322
239	VCC	2350.5	322
240	NC	2173.5	317
241	COM0	2146.5	317
242	COM1	2119.5	317
243	COM2	2092.5	317
244	COM3	2065.5	317
245	COM4	2038.5	317
246	COM5	2011.5	317
247	COM6	1984.5	317
248	COM7	1957.5	317
249	COM8	1930.5	317
250	COM9	1903.5	317
251	COM10	1876.5	317
252	COM11	1849.5	317
253	COM12	1822.5	317
254	COM13	1795.5	317
255	COM14	1768.5	317
256	COM15	1741.5	317
257	COM16	1714.5	317
258	COM17	1687.5	317
259	COM18	1660.5	317
260	COM19	1633.5	317
261	COM20	1606.5	317
262	COM21	1579.5	317
263	COM22	1552.5	317
264	COM23	1525.5	317
265	COM24	1498.5	317
266	COM25	1471.5	317
267	COM26	1444.5	317
268	COM27	1417.5	317
269	COM28	1390.5	317
270	COM29	1363.5	317
271	COM30	1336.5	317
272	COM31	1309.5	317
273	COM32	1282.5	317
274	COM33	1255.5	317
275	COM34	1228.5	317
276	COM35	1201.5	317
277	COM36	1174.5	317
278	COM37	1147.5	317
279	COM38	1120.5	317
280	COM39	1093.5	317
281	COM40	1066.5	317
282	COM41	1039.5	317
283	COM42	1012.5	317
284	COM43	985.5	317
285	COM44	958.5	317
286	COM45	931.5	317
287	COM46	904.5	317
288	COM47	877.5	317
289	COM48	850.5	317
290	COM49	823.5	317
291	COM50	796.5	317
292	COM51	769.5	317
293	COM52	742.5	317
294	COM53	715.5	317
295	COM54	688.5	317
296	COM55	661.5	317
297	COM56	634.5	317
298	COM57	607.5	317
299	COM58	580.5	317
300	COM59	553.5	317
301	COM60	526.5	317
302	COM61	499.5	317
303	COM62	472.5	317
304	COM63	445.5	317
305	COM64	418.5	317
306	COM65	391.5	317
307	COM66	364.5	317
308	COM67	337.5	317
309	COM68	310.5	317
310	COM69	283.5	317
311	COM70	256.5	317
312	COM71	229.5	317
313	COM72	202.5	317
314	COM73	175.5	317
315	COM74	148.5	317
316	COM75	121.5	317
317	COM76	94.5	317
318	COM77	67.5	317
319	COM78	40.5	317
320	COM79	13.5	317
321	COM80	-13.5	317
322	COM81	-40.5	317
323	COM82	-67.5	317
324	COM83	-94.5	317
325	COM84	-121.5	317
326	COM85	-148.5	317
327	COM86	-175.5	317
328	COM87	-202.5	317
329	COM88	-229.5	317
330	COM89	-256.5	317
331	COM90	-283.5	317
332	COM91	-310.5	317
333	COM92	-337.5	317
334	COM93	-364.5	317
335	COM94	-391.5	317
336	COM95	-418.5	317
337	COM96	-445.5	317
338	COM97	-472.5	317
339	COM98	-499.5	317
340	COM99	-526.5	317
341	COM100	-553.5	317
342	COM101	-580.5	317
343	COM102	-607.5	317
344	COM103	-634.5	317
345	COM104	-661.5	317
346	COM105	-688.5	317
347	COM106	-715.5	317
348	COM107	-742.5	317
349	COM108	-769.5	317
350	COM109	-796.5	317
351	COM110	-823.5	317
352	COM111	-850.5	317
353	COM112	-877.5	317
354	COM113	-904.5	317
355	COM114	-931.5	317
356	COM115	-958.5	317
357	COM116	-985.5	317
358	COM117	-1012.5	317
359	COM118	-1039.5	317
360	COM119	-1066.5	317
361	COM120	-1093.5	317
362	COM121	-1120.5	317
363	COM122	-1147.5	317
364	COM123	-1174.5	317
365	COM124	-1201.5	317
366	COM125	-1228.5	317
367	COM126	-1255.5	317
368	COM127	-1282.5	317
369	COM128	-1309.5	317
370	COM129	-1336.5	317
371	COM130	-1363.5	317
372	COM131	-1390.5	317
373	COM132	-1417.5	317
374	COM133	-1444.5	317
375	COM134	-1471.5	317
376	COM135	-1498.5	317
377	COM136	-1525.5	317
378	COM137	-1552.5	317
379	COM138	-1579.5	317
380	COM139	-1606.5	317
381	COM140	-1633.5	317
382	COM141	-1660.5	317
383	COM142	-1687.5	317
384	COM143	-1714.5	317
385	COM144	-1741.5	317
386	COM145	-1768.5	317
387	COM146	-1795.5	317
388	COM147	-1822.5	317
389	COM148	-1849.5	317
390	COM149	-1876.5	317
391	COM150	-1903.5	317
392	COM151	-1930.5	317
393	COM152	-1957.5	317
394	COM153	-1984.5	317
395	COM154	-2011.5	317
396	COM155	-2038.5	317
397	COM156	-2065.5	317
398	COM157	-2092.5	317
399	COM158	-2119.5	317
400	COM159	-2146.5	317
401	NC	-2173.5	317
402	VCC	-2350.5	322
403	SEG80	-2377.5	322
404	SEG81	-2404.5	322
405	SEG82	-2431.5	322
406	SEG83	-2458.5	322
407	SEG84	-2485.5	322
408	SEG85	-2512.5	322
409	SEG86	-2539.5	322
410	SEG87	-2566.5	322
411	SEG88	-2593.5	322
412	SEG89	-2620.5	322
413	SEG90	-2647.5	322
414	SEG91	-2674.5	322
415	SEG92	-2701.5	322
416	SEG93	-2728.5	322
417	SEG94	-2755.5	322
418	SEG95	-2782.5	322
419	SEG96	-2809.5	322
420	SEG97	-2836.5	322
421	SEG98	-2863.5	322
422	SEG99	-2890.5	322
423	SEG100	-2917.5	322
424	SEG101	-2944.5	322
425	SEG102	-2971.5	322
426	SEG103	-2998.5	322
427	SEG104	-3025.5	322
428	SEG105	-3052.5	322
429	SEG106	-3079.5	322
430	SEG107	-3106.5	322
431	SEG108	-3133.5	322
432	SEG109	-3160.5	322
433	SEG110	-3187.5	322
434	SEG111	-3214.5	322
435	SEG112	-3241.5	322
436	SEG113	-3268.5	322
437	SEG114	-3295.5	322
438	SEG115	-3322.5	322
439	SEG116	-3349.5	322
440	SEG117	-3376.5	322
441	SEG118	-3403.5	322
442	SEG119	-3430.5	322
443	SEG120	-3457.5	322
444	SEG121	-3484.5	322
445	SEG122	-3511.5	322
446	SEG123	-3538.5	322
447	SEG124	-3565.5	322
448	SEG125	-3592.5	322
449	SEG126	-3619.5	322
450	SEG127	-3646.5	322
451	SEG128	-3673.5	322
452	SEG129	-3700.5	322
453	SEG130	-3727.5	322
454	SEG131	-3754.5	322
455	SEG132	-3781.5	322
456	SEG133	-3808.5	322
457	SEG134	-3835.5	322
458	SEG135	-3862.5	322
459	SEG136	-3889.5	322
460	SEG137	-3916.5	322
461	SEG138	-3943.5	322
462	SEG139	-3970.5	322
463	SEG140	-3997.5	322
464	SEG141	-4024.5	322
465	SEG142	-4051.5	322
466	SEG143	-4078.5	322
467	SEG144	-4105.5	322
468	SEG145	-4132.5	322
469	SEG146	-4159.5	322
470	SEG147	-4186.5	322
471	SEG148	-4213.5	322
472	SEG149	-4240.5	322
473	SEG150	-4267.5	322
474	SEG151	-4294.5	322
475	SEG152	-4321.5	322
476	SEG153	-4348.5	322
477	SEG154	-4375.5	322
478	SEG155	-4402.5	322
479	SEG156	-4429.5	322
480	SEG157	-4456.5	322
481	SEG158	-4483.5	322
482	SEG159	-4510.5	322
483	NC	-4537.5	322

Note

(1) Input Side: pin 1 to 157; Output Side: pin 158 to 483.

Appendix VII: SSD1320Z Die Tray Information

Figure 1: SSD1320Z Die Tray drawing



Symbol	Spec (mm)	(mil)
W1	76.00±0.10	(2992)
W2	68.00±0.10	(2677)
W3	68.30±0.10	(2689)
Dx	10.50±0.10	(413)
TPx	55.00±0.10	(2165)
Dy	6.15±0.10	(242)
TPy	63.70±0.10	(2508)
Px	11.00±0.05	(433)
Py	2.45±0.05	(96)
X	9.48±0.05	(373)
Y	0.95±0.05	(37)
Z	0.35±0.05	(14)
N	162(pocket number)	

Remark:

1. Depth of text : Max. 0.1mm
2. Tray material : ABS
3. Tray Color Code: Black
4. Surface Resistance: 10^{9}~10^{12}Ω/SQ
5. Tray Warpage: Max. ±0.1mm
6. Pocket Bottom: Rough Surface