FDC2112-Q1, FDC2114-Q1, FDC2212-Q1, FDC2214-Q1 Multi-Channel 12-Bit or 28-Bit Capacitance-to-Digital Converter (FDC) for Capacitive Sensing

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1:−40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C5
- EMI-Resistant Architecture
- Maximum Output Rates (One Active Channel):
  - 13.3 kspS (FDC2112-Q1, FDC2114-Q1)
  - 4.08 kspS (FDC2212-Q1, FDC2214-Q1)
- Maximum Input Capacitance: 250 nF (at 10 kHz with 1-mH inductor)
- Sensor Excitation Frequency: 10 kHz to 10 MHz
- Number of Channels: 2, 4
- Resolution: Up to 28 bits
- RMS noise: 0.3 fF at 100 sps and fSENSOR = 5MHz
- Supply Voltage: 2.7 V to 3.6 V
- Power Consumption: Active: 2.1 mA
- Low-Power Sleep Mode: 35 µA
- Shutdown: 200 nA
- Interface: I2C
- Temperature Range: −40°C to +125°C

2 Applications

- EMI-Resistant Proximity Sensor
- EMI-Resistant Gesture Recognition
- EMI-Resistant Foreign Object Detection
- EMI-Resistant Rain / Fog / Ice / Snow Sensor
- Automotive Door / Kick Sensors

3 Description

Capacitive sensing is a low-power, low-cost, high-resolution contactless sensing technique that can be applied to a variety of applications ranging from proximity detection to gesture recognition. The sensor in a capacitive sensing system is any metal or conductor, allowing for low cost and highly flexible system design.

The main challenge limiting sensitivity in capacitive sensing applications is noise susceptibility of the sensors. With the FDC2x1x-Q1 innovative EMI resistant architecture, performance can be maintained even in presence of high-noise environments.

The FDC2x1x-Q1 is a multi-channel family of noise- and EMI-resistant, high-resolution, high-speed capacitance-to-digital converters for implementing capacitive sensing solutions. The devices employ an innovative narrow-band based architecture to offer high rejection of noise and interferers while providing high resolution at high speed. The devices support a wide excitation frequency range, offering flexibility in system design.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FDC2112-Q1</td>
<td>WSON (12)</td>
<td>4.00 mm × 4.00 mm</td>
</tr>
<tr>
<td>FDC2114-Q1</td>
<td>WQFN (16)</td>
<td>4.00 mm × 4.00 mm</td>
</tr>
<tr>
<td>FDC2212-Q1</td>
<td>WSON (12)</td>
<td>4.00 mm × 4.00 mm</td>
</tr>
<tr>
<td>FDC2214-Q1</td>
<td>WQFN (16)</td>
<td>4.00 mm × 4.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

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An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History

<table>
<thead>
<tr>
<th>DATE</th>
<th>REVISION</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>May 2016</td>
<td>*</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>
# Pin Configuration and Functions

## 5 Pin Configuration and Functions

### Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE(1)</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NO.</td>
<td>NAME</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>SCL</td>
<td>I</td>
</tr>
<tr>
<td>2</td>
<td>SDA</td>
<td>I/O</td>
</tr>
<tr>
<td>3</td>
<td>CLKN</td>
<td>I</td>
</tr>
<tr>
<td>4</td>
<td>ADDR</td>
<td>I</td>
</tr>
<tr>
<td>5</td>
<td>INTB</td>
<td>O</td>
</tr>
<tr>
<td>6</td>
<td>SD</td>
<td>I</td>
</tr>
<tr>
<td>7</td>
<td>VDD</td>
<td>P</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>G</td>
</tr>
<tr>
<td>9</td>
<td>IN0A</td>
<td>A</td>
</tr>
<tr>
<td>10</td>
<td>IN0B</td>
<td>A</td>
</tr>
<tr>
<td>11</td>
<td>IN1A</td>
<td>A</td>
</tr>
<tr>
<td>12</td>
<td>IN1B</td>
<td>A</td>
</tr>
<tr>
<td>13</td>
<td>IN2A</td>
<td>A</td>
</tr>
<tr>
<td>14</td>
<td>IN2B</td>
<td>A</td>
</tr>
<tr>
<td>15</td>
<td>IN3A</td>
<td>A</td>
</tr>
<tr>
<td>16</td>
<td>IN3B</td>
<td>A</td>
</tr>
<tr>
<td>DAP</td>
<td>DAP(2)</td>
<td>N/A</td>
</tr>
</tbody>
</table>

---

(1) I = Input, O = Output, P=Power, G=Ground, A=Analog  
(2) There is an internal electrical connection between the exposed Die Attach Pad (DAP) and the GND pin of the device. Although the DAP can be left floating, for best performance the DAP should be connected to the same potential as the device's GND pin. Do not use the DAP as the primary ground for the device. The device GND pin must always be connected to ground.
6 Specifications

6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td></td>
<td>5</td>
<td>V</td>
</tr>
<tr>
<td>V(i)</td>
<td>–0.3</td>
<td>VDD + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>I(A)</td>
<td>–8</td>
<td>8</td>
<td>mA</td>
</tr>
<tr>
<td>I(D)</td>
<td>–5</td>
<td>5</td>
<td>mA</td>
</tr>
<tr>
<td>(T_J)</td>
<td>–55</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>(T_{stg})</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>Description</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(\text{ESD})</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Charge-device model (CDM), per AEC Q100-011</td>
<td>±750</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions
Unless otherwise specified, all limits ensured for \(T_A = 25°C, VDD = 3.3\) V

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>2.7</td>
<td>3.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(T_A)</td>
<td>–40</td>
<td></td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>Thermal Metric(^{(1)})</th>
<th>FDC2112 / FDC2212</th>
<th>FDC2214 / FDC2214</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{JA}) Junction-to-ambient thermal resistance</td>
<td>36.7</td>
<td>35.6</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{JC\text{(top)}}) Junction-to-case (top) thermal resistance</td>
<td>36.2</td>
<td>36.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{JB}) Junction-to-board thermal resistance</td>
<td>14</td>
<td>13.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi_{JT}) Junction-to-top characterization parameter</td>
<td>0.4</td>
<td>0.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi_{JB}) Junction-to-board characterization parameter</td>
<td>14.2</td>
<td>13.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{JC\text{(bot)}}) Junction-to-case (bottom) thermal resistance</td>
<td>3.5</td>
<td>3.5</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
### 6.5 Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_A = 25°C$, $VDD = 3.3\, V$\(^{(1)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS (^{(2)})</th>
<th>MIN (^{(3)})</th>
<th>TYP (^{(4)})</th>
<th>MAX (^{(3)})</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>Supply voltage $T_A = –40°C$ to 125°C</td>
<td>2.7</td>
<td>3.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{DD}$</td>
<td>Supply current (not including sensor current) (^{(5)}) $CLKIN = 10MHz$ (^{(6)})</td>
<td>2.1</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{DDSL}$</td>
<td>Sleep mode supply current (^{(5)})</td>
<td>35</td>
<td>60</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$I_{SD}$</td>
<td>Shutdown mode supply current (^{(5)})</td>
<td>0.2</td>
<td>1</td>
<td>µA</td>
<td></td>
</tr>
</tbody>
</table>

### CAPACITIVE SENSOR

| $C_{SENSOR MAX}$ | Maximum sensor capacitance | 1-mH inductor, 10-kHz oscillation | 250 | nF |
| $C_{IN}$ | Sensor pin parasitic capacitance | 4 | pF |
| $N_{BITS}$ | Number of bits | FDC2112, FDC2114 $RCOUNT \geq 0x0400$ | 12 | bits |
| | | FDC2212, FDC2214 $RCOUNT = 0xFFFF$ | 28 | bits |
| $f_{CS}$ | Maximum channel sample rate | FDC2112, FDC2114 single active channel continuous conversion, $SCL = 400\, kHz$ | 13.3 | kSPS |
| | | FDC2212, FDC2214 single active channel continuous conversion, $SCL = 400\, kHz$ | 4.08 | kSPS |

### EXCITATION

| $f_{SENSOR}$ | Sensor excitation frequency $T_A = –40°C$ to 125°C | 0.01 | 10 | MHz |
| $V_{SENSOR MIN}$ | Minimum sensor oscillation amplitude (pk) \(^{(7)}\) | 1.2 | V |
| $V_{SENSOR MAX}$ | Maximum sensor oscillation amplitude (pk) | 1.8 | V |
| $I_{SENSOR MAX}$ | Sensor maximum current drive $HIGH_{CURRENT}_{DRV} = b0$ $DRIVE_{CURRENT}_{CH0} = 0xF800$ | 1.5 | mA |
| | | $HIGH_{CURRENT}_{DRV} = b1$ $DRIVE_{CURRENT}_{CH0} = 0xF800$ Channel 0 only | 6 | mA |

---

(1) Electrical Characteristics values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

(2) Register values are represented as either binary (b is the prefix to the digits), or hexadecimal (0x is the prefix to the digits). Decimal values have no prefix.

(3) Limits are ensured by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

(5) I2C read/write communication and pullup resistors current through SCL, SDA not included.

(6) Sensor capacitor: 1 layer, 20.9 × 13.9 mm, Bourns CMH322522-180KL sensor inductor with L=18 µH and 33 pF 1% COG/NP0 Target: Grounded aluminum plate (176 × 123 mm), Channel = Channel 0 (continuous mode) $CLKIN = 40\, MHz$, $CHx_{FIN\_SEL} = b10$, $CHx_{FREQ\_DIVIDER} = b00\, 0000\, 0001\, CH0_{RCOUNT} = 0xFFFF$, $SETTLECOUNT_{CH0} = 0x0100$, $DRIVE_{CURRENT}_{CH0} = 0x7800$.

(7) Lower $V_{SENSOR MIN}$ oscillation amplitudes can be used, but will result in lower SNR.
## Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for $T_A = 25^\circ C$, $VDD = 3.3\, V^{(1)}$

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN(3)</th>
<th>TYP(4)</th>
<th>MAX(5)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>MASTER CLOCK</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f_{\text{CLKIN}}$</td>
<td>External master clock input frequency (CLKIN)</td>
<td>$T_A = –40^\circ C$ to $125^\circ C$</td>
<td>2</td>
<td>40</td>
<td>MHz</td>
</tr>
<tr>
<td>$CLKIN_{\text{DUTY_MIN}}$</td>
<td>External master clock minimum acceptable duty cycle (CLKIN)</td>
<td></td>
<td></td>
<td>40%</td>
<td></td>
</tr>
<tr>
<td>$CLKIN_{\text{DUTY_MAX}}$</td>
<td>External master clock maximum acceptable duty cycle (CLKIN)</td>
<td></td>
<td></td>
<td>60%</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{CLKIN LO}}$</td>
<td>CLKN low voltage threshold</td>
<td></td>
<td></td>
<td>0.3 $V_{\text{DD}}$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{CLKIN HI}}$</td>
<td>CLKN high voltage threshold</td>
<td></td>
<td></td>
<td>$0.7 \times V_{\text{DD}}$</td>
<td>V</td>
</tr>
<tr>
<td>$f_{\text{INTCLK}}$</td>
<td>Internal master clock frequency range</td>
<td></td>
<td>35</td>
<td>43.4</td>
<td>55 MHz</td>
</tr>
<tr>
<td>$T_{\text{CF,int}_p}$</td>
<td>Internal master clock temperature coefficient mean</td>
<td></td>
<td></td>
<td>–13</td>
<td>ppm/°C</td>
</tr>
</tbody>
</table>

### 6.6 Timing Requirements

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{\text{SDWAKEUP}}$</td>
<td>2</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>$t_{\text{SLEEPWAKEUP}}$</td>
<td>0.05</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>$t_{\text{WD-TIMEOUT}}$</td>
<td>5.2</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
</tbody>
</table>

#### I2C TIMING CHARACTERISTICS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{SCL}$</td>
<td>10</td>
<td></td>
<td>400</td>
<td>kHz</td>
</tr>
<tr>
<td>$t_{\text{LOW}}$</td>
<td>1.3</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>$t_{\text{HIGH}}$</td>
<td>0.6</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>$t_{\text{HD;STA}}$</td>
<td>0.6</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>$t_{\text{SU;STA}}$</td>
<td>0.6</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>$t_{\text{HD;DAT}}$</td>
<td>0</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>$t_{\text{SU;DAT}}$</td>
<td>0</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>$t_{\text{SU;STO}}$</td>
<td>0</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>$t_{\text{BUF}}$</td>
<td>0.6</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>$t_{\text{VD;DAT}}$</td>
<td>0.9</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>$t_{\text{VD;ACK}}$</td>
<td>0.9</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>$t_{\text{SP}}$</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) This parameter is specified by design and/or characterization and is not tested in production.
6.7 Switching Characteristics - I2C

Unless otherwise specified, all limits ensured for $T_A = 25^\circ C$, $VDD = 3.3 \, V$

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Input high voltage</td>
<td>$0.7 \times V_{DD}$</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input low voltage</td>
<td>$0.3 \times V_{DD}$</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output low voltage (3 mA sink current)</td>
<td>$0.4$</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>HYS</td>
<td>Hysteresis</td>
<td>$0.1 \times V_{DD}$</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

![I2C Timing Diagram](image-url)

**Figure 1. I2C Timing**
6.8 Typical Characteristics

Common test conditions (unless specified otherwise): Sensor capacitor: 1 layer, 20.9 × 13.9 mm, Bourns CMH322522-180KL sensor inductor with L = 18 µH and 33 pF 1% COG/NP0 Target: Grounded aluminum plate (176 × 123 mm), Channel = Channel 0 (continuous mode) CLKin = 40 MHz, CHx_FIN_SEL = b01, CHx_FREF_DIVIDER = b00 0000 0001 CH0_RCOUNT = 0xFFFF, SETTLECOUNT_CH0 = 0x0100, DRIVE_CURRENT_CH0 = 0x7800.

-40°C to +125°C

![Figure 2. Active Mode \(I_{DD}\) vs. Temperature](image)

![Figure 3. Active Mode \(I_{DD}\) vs \(V_{DD}\)](image)

-40°C to +125°C

![Figure 4. Sleep Mode \(I_{DD}\) vs Temperature](image)

![Figure 5. Sleep Mode \(I_{DD}\) vs \(V_{DD}\)](image)

-40°C to +125°C

![Figure 6. Shutdown Mode \(I_{DD}\) vs Temperature](image)

![Figure 7. Shutdown Mode \(I_{DD}\) vs \(V_{DD}\)](image)

-40°C to +125°C
Typical Characteristics (continued)

Common test conditions (unless specified otherwise): Sensor capacitor: 1 layer, 20.9 × 13.9 mm, Bourns CMH322522-180KL sensor inductor with L = 18 µH and 33 pF 1% COG/NP0 Target: Grounded aluminum plate (176 × 123 mm), Channel = Channel 0 (continuous mode) CLkin = 40 MHz, CHx_FLN_SEL = b01, CHx_FREF_DIVIDER = b00 0000 0001 CH0_RCOUNT = 0xFFFF, SETTLE_COUNT_CH0 = 0x0100, DRIVE_CURRENT_CH0 = 0x7800.

<table>
<thead>
<tr>
<th>Temperature (° C)</th>
<th>Internal Oscillator (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-40</td>
<td>43.32</td>
</tr>
<tr>
<td>-20</td>
<td>43.33</td>
</tr>
<tr>
<td>0</td>
<td>43.34</td>
</tr>
<tr>
<td>25</td>
<td>43.35</td>
</tr>
<tr>
<td>50</td>
<td>43.36</td>
</tr>
<tr>
<td>85</td>
<td>43.37</td>
</tr>
<tr>
<td>100</td>
<td>43.38</td>
</tr>
<tr>
<td>125</td>
<td>43.39</td>
</tr>
</tbody>
</table>

-40°C to +125°C

Data based on 1 unit

Figure 8. Internal Oscillator Frequency vs Temperature

Figure 9. Internal Oscillator Frequency vs VDD
7 Detailed Description

7.1 Overview

The FDC2112, FDC2114, FDC2212, and FDC2214 are high-resolution, multichannel capacitance-to-digital converters for implementing capacitive sensing solutions. In contrast to traditional switched-capacitance architectures, the FDC2112, FDC2114, FDC2212, and FDC2214 employ an L-C resonator, also known as L-C tank, as a sensor. The narrow-band architecture allows unprecedented EMI immunity and greatly reduced noise floor when compared to other capacitive sensing solutions.

Using this approach, a change in capacitance of the L-C tank can be observed as a shift in the resonant frequency. Using this principle, the FDC is a capacitance-to-digital converter (FDC) that measures the oscillation frequency of an LC resonator. The device outputs a digital value that is proportional to frequency. This frequency measurement can be converted to an equivalent capacitance.

7.2 Functional Block Diagrams

Figure 10. Block Diagram for the FDC2112 and FDC2212

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The FDC is composed of front-end resonant circuit drivers, followed by a multiplexer that sequences through the active channels, connecting them to the core that measures and digitizes the sensor frequency ($f_{\text{SENSOR}}$). The core uses a reference frequency ($f_{\text{REF}}$) to measure the sensor frequency. $f_{\text{REF}}$ is derived from either an internal reference clock (oscillator), or an externally supplied clock. The digitized output for each channel is proportional to the ratio of $f_{\text{SENSOR}}$/$f_{\text{REF}}$. The I2C interface is used to support device configuration and to transmit the digitized frequency values to a host processor. The FDC can be placed in shutdown mode, saving current, using the SD pin. The INTB pin may be configured to notify the host of changes in system status.

### 7.3 Feature Description

#### 7.3.1 Clocking Architecture

Figure 12 shows the clock dividers and multiplexers of the FDC.
Feature Description (continued)

In Figure 12, the key clocks are $f_{IN}$, $f_{REF}$, and $f_{CLK}$. $f_{CLK}$ is selected from either the internal clock source or external clock source (CLKIN). The frequency measurement reference clock, $f_{REF}$, is derived from the $f_{CLK}$ source. TI recommends that precision applications use an external master clock that offers the stability and accuracy requirements needed for the application. The internal oscillator may be used in applications that require low cost and do not require high precision. The $f_{IN}$ clock is derived from sensor frequency for a channel $x$, $f_{SENSOR_x}$. $f_{REF_x}$ and $f_{IN_x}$ must meet the requirements listed in Table 1, depending on whether $f_{CLK}$ (master clock) is the internal or external clock.

![Clocking Diagram](image-url)

(1) FDC2114 / FDC2214 only

Figure 12. Clocking Diagram
Feature Description (continued)

Table 1. Clock Configuration Requirements

<table>
<thead>
<tr>
<th>MODE(1)</th>
<th>CLKin SOURCE</th>
<th>VALID fREFx RANGE (MHz)</th>
<th>VALID fINx RANGE</th>
<th>SET CHx FIN_SEL to (2)</th>
<th>SET CHx_SETTLECOUNT to</th>
<th>SET CHx_RCOUNT to</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-channel</td>
<td>Internal</td>
<td>fREFx ≤ 55</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>External</td>
<td>fREFx ≤ 40</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Single-channel</td>
<td>Either external or internal</td>
<td>fREFx ≤ 35</td>
<td>&lt; fREFx /4</td>
<td>Differential sensor configuration: b0: 0.01MHz to 8.75MHz (divide by 1) b1: 5MHz to 10MHz (divide by 2)</td>
<td>&gt; 3</td>
<td>&gt; 8</td>
</tr>
</tbody>
</table>

(1) Channels 2 and 3 are only available for FDC2114 and FDC2214.

(2) Refer to Sensor Configuration for information on differential and single-ended sensor configurations.

Table 2 shows the clock configuration registers for all channels.

Table 2. Clock Configuration Registers

<table>
<thead>
<tr>
<th>CHANNEL(1)</th>
<th>CLOCK</th>
<th>REGISTER</th>
<th>FIELD [BIT(S)]</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>All</td>
<td>fCLK = Master Clock Source</td>
<td>CONFIG, addr 0x1A</td>
<td>REF_CLK_SRC [9]</td>
<td>b0 = internal oscillator is used as the master clock b1 = external clock source is used as the master clock</td>
</tr>
<tr>
<td>0</td>
<td>fREF0</td>
<td>CLOCK_DIVIDER S_CH0, addr 0x14</td>
<td>CH0_FREF_DIVIDER [9:0]</td>
<td>fREF0 = fCLK / CH0_FREF_DIVIDER</td>
</tr>
<tr>
<td>1</td>
<td>fREF1</td>
<td>CLOCK_DIVIDER S_CH1, addr 0x15</td>
<td>CH1_FREF_DIVIDER [9:0]</td>
<td>fREF1 = fCLK / CH1_FREF_DIVIDER</td>
</tr>
<tr>
<td>2</td>
<td>fREF2</td>
<td>CLOCK_DIVIDER S_CH2, addr 0x16</td>
<td>CH2_FREF_DIVIDER [9:0]</td>
<td>fREF2 = fCLK / CH2_FREF_DIVIDER</td>
</tr>
<tr>
<td>3</td>
<td>fREF3</td>
<td>CLOCK_DIVIDER S_CH3, addr 0x17</td>
<td>CH3_FREF_DIVIDER [9:0]</td>
<td>fREF3 = fCLK / CH3_FREF_DIVIDER</td>
</tr>
<tr>
<td>0</td>
<td>fIN0</td>
<td>CLOCK_DIVIDER S_CH0, addr 0x14</td>
<td>CH0_FIN_SEL [13:12]</td>
<td>fIN0 = fSENSOR0 / CH0_FIN_SEL</td>
</tr>
<tr>
<td>1</td>
<td>fIN1</td>
<td>CLOCK_DIVIDER S_CH1, addr 0x15</td>
<td>CH1_FIN_SEL [13:12]</td>
<td>fIN1 = fSENSOR1 / CH1_FIN_SEL</td>
</tr>
<tr>
<td>2</td>
<td>fIN2</td>
<td>CLOCK_DIVIDER S_CH2, addr 0x16</td>
<td>CH2_FIN_SEL [13:12]</td>
<td>fIN2 = fSENSOR2 / CH2_FIN_SEL</td>
</tr>
<tr>
<td>3</td>
<td>fIN3</td>
<td>CLOCK_DIVIDER S_CH3, addr 0x17</td>
<td>CH3_FIN_SEL [13:12]</td>
<td>fIN3 = fSENSOR3 / CH3_FIN_SEL</td>
</tr>
</tbody>
</table>

(1) Channels 2 and 3 are only available for FDC2114 and FDC2214

7.3.2 Multi-Channel and Single-Channel Operation

The multi-channel package of the FDC enables the user to save board space and support flexible system design. For example, temperature drift can often cause a shift in component values, resulting in a shift in resonant frequency of the sensor. Using a second sensor as a reference provides the capability to cancel out a temperature shift. When operated in multi-channel mode, the FDC sequentially samples the active channels. In single-channel mode, the FDC samples a single channel, which is selectable. Table 3 shows the registers and values that are used to configure either multi-channel or single-channel modes.
Table 3. Single- and Multi-Channel Configuration Registers

<table>
<thead>
<tr>
<th>MODE</th>
<th>REGISTER</th>
<th>FIELD [ BIT(S) ]</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single channel</td>
<td>CONFIG, addr 0x1A</td>
<td>ACTIVE_CHAN[15:14]</td>
<td>00 = chan 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01 = chan 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10 = chan 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11 = chan 3</td>
</tr>
<tr>
<td></td>
<td>MUX_CONFIG addr 0x1B</td>
<td>AUTOSCAN_EN[15]</td>
<td>0 = continuous conversion on a single channel (default)</td>
</tr>
<tr>
<td>Multi-channel</td>
<td>MUX_CONFIG addr 0x1B</td>
<td>AUTOSCAN_EN[15]</td>
<td>1 = continuous conversion on multiple channels</td>
</tr>
<tr>
<td></td>
<td>MUX_CONFIG addr 0x1B</td>
<td>RR_SEQUENCE[14:13]</td>
<td>00 = Ch0, Ch1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01 = Ch0, Ch1, Ch2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10 = Ch0, Ch1, Ch2, Ch3</td>
</tr>
</tbody>
</table>

The digitized sensor measurement for each channel (DATAx) represents the ratio of the sensor frequency to the reference frequency.

The data output (DATAx) of the FDC2112 and FDC2114 is expressed as the 12 MSBs of a 16-bit result:

\[
DATA_x = \frac{f_{SENSORx} \times 2^{12}}{f_{REFx}}
\]  

The data output (DATAx) of the FDC2212 and FDC2214 is expressed as:

\[
DATA_x = \frac{f_{SENSORx} \times 2^{28}}{f_{REFx}}
\]  

Table 4. Sample Data Registers

<table>
<thead>
<tr>
<th>CHANNEL (1)</th>
<th>REGISTER (2)</th>
<th>FIELD NAME [ BITS(S) ] AND VALUE (FDC2112, FDC2114)</th>
<th>FIELD NAME [ BITS(S) ] AND VALUE (FDC2212, FDC2214) (3)(4)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>DATA_CH0, addr 0x00</td>
<td>DATA0 [11:0]: 12 bits of the 16 bit conversion result. 0x000 = under range 0xffff = over range</td>
<td>DATA0 [27:16]: 12 MSBs of the 28 bit conversion result</td>
</tr>
<tr>
<td></td>
<td>DATA_LSB_CH0, addr 0x01</td>
<td>Not applicable</td>
<td>DATA0 [15:0]: 16 LSBs of the 28 bit conversion result</td>
</tr>
<tr>
<td>1</td>
<td>DATA_CH1, addr 0x02</td>
<td>DATA1 [11:0]: 12 bits of the 16 bit conversion result. 0x000 = under range 0xffff = over range</td>
<td>DATA1 [27:16]: 12 MSBs of the 28 bit conversion result</td>
</tr>
<tr>
<td></td>
<td>DATA_LSB_CH1, addr 0x03</td>
<td>Not applicable</td>
<td>DATA1 [15:0]: 16 LSBs of the 28 bit conversion result</td>
</tr>
<tr>
<td>2</td>
<td>DATA_CH2, addr 0x04</td>
<td>DATA2 [11:0]: 12 bits of the 16 bit conversion result. 0x000 = under range 0xffff = over range</td>
<td>DATA2 [27:16]: 12 MSBs of the 28 bit conversion result</td>
</tr>
<tr>
<td></td>
<td>DATA_LSB_CH2, addr 0x05</td>
<td>Not applicable</td>
<td>DATA2 [15:0]: 16 LSBs of the 28 bit conversion result</td>
</tr>
</tbody>
</table>

(1) Channels 2 and 3 are only available for FDC2114 and FDC2214.
(2) The DATA_CHx.DATAx register must always be read first, followed by the DATA_LSB_CHx.DATAx register of the same channel to ensure data coherency.
(3) A DATA value of 0x00000000 = under range for FDC2212/FDC2214.
(4) A DATA value of 0xFFFFFFF = over range for FDC2212/FDC2214.
Table 4. Sample Data Registers (continued)

<table>
<thead>
<tr>
<th>CHANNEL(1)</th>
<th>REGISTER(2)</th>
<th>FIELD NAME [ BITS(S) ] AND VALUE (FDC2112, FDC2114)</th>
<th>FIELD NAME [ BITS(S) ] AND VALUE (FDC2212, FDC2214) (3)(4)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>DATA_CH3, addr 0x06</td>
<td>DATA3 [11:0]: 12 bits of the 16 bit conversion result. 0x000 = under range 0xfff = over range</td>
<td>DATA3 [27:16]: 12 MSBs of the 28 bit conversion result</td>
</tr>
<tr>
<td></td>
<td>DATA_LSB_CH3, addr 0x07</td>
<td>Not applicable</td>
<td>DATA3 [15:0]: 16 LSBs of the 28 bit conversion result</td>
</tr>
</tbody>
</table>

When the FDC sequences through the channels in multi-channel mode, the dwell time interval for each channel is the sum of three parts:
1. sensor activation time
2. conversion time
3. channel switch delay

The sensor activation time is the amount of settling time required for the sensor oscillation to stabilize, as shown in Figure 13. The settling wait time is programmable and should be set to a value that is long enough to allow stable oscillation. The settling wait time for channel \( x \) is given by:

\[
t_{Sx} = \frac{(\text{CHX\_SETTLECOUNT}^x)}{f_{\text{REFx}}} \tag{3}
\]

Table 5 illustrates the registers and values for configuring the settling time for each channel.

![Figure 13. Multi-channel Mode Sequencing](image1)

![Figure 14. Single-channel Mode Sequencing](image2)
Table 5. Settling Time Register Configuration

<table>
<thead>
<tr>
<th>CHANNEL(1)</th>
<th>REGISTER</th>
<th>FIELD [ BIT(S) ]</th>
<th>CONVERSION TIME(2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>SETTLECOUNT_CH0, addr 0x10</td>
<td>CH0_SETTLECOUNT [15:0]</td>
<td>(CH0_SETTLECOUNT*16)/fREF0</td>
</tr>
<tr>
<td>1</td>
<td>SETTLECOUNT_CH1, addr 0x11</td>
<td>CH1_SETTLECOUNT [15:0]</td>
<td>(CH1_SETTLECOUNT*16)/fREF1</td>
</tr>
<tr>
<td>2</td>
<td>SETTLECOUNT_CH2, addr 0x12</td>
<td>CH2_SETTLECOUNT [15:0]</td>
<td>(CH2_SETTLECOUNT*16)/fREF2</td>
</tr>
<tr>
<td>3</td>
<td>SETTLECOUNT_CH3, addr 0x13</td>
<td>CH3_SETTLECOUNT [15:0]</td>
<td>(CH3_SETTLECOUNT*16)/fREF3</td>
</tr>
</tbody>
</table>

(1) Channels 2 and 3 are available only in the FDC2114 and FDC2214.
(2) fREFx is the reference frequency configured for the channel.

The SETTLECOUNT for any channel x must satisfy:

\[ CHx_SETTLECOUNT > V_{p_k} \times f_{REFx} \times C \times \pi^2 / (32 \times IDRIVE_x) \]  

where
- \( V_{p_k} \) = Peak oscillation amplitude at the programmed IDrive setting
- \( f_{REFx} \) = Reference frequency for Channel x
- \( C \) = sensor capacitance including parasitic PCB capacitance
- \( IDRIVE_x \) = setting programmed into the IDRIVE register in amps

Round the result to the next highest integer (for example, if Equation 4 recommends a minimum value of 6.08, program the register to 7 or higher).

The conversion time represents the number of reference clock cycles used to measure the sensor frequency. It is set by the CHx_RCOUNT register for the channel. The conversion time for any channel x is:

\[ t_{Cx} = (CHx_RCOUNT \times 16 + 4) / f_{REFx} \]  

The reference count value must be chosen to support the required number of effective bits (ENOB). For example, if an ENOB of 13 bits is required, then a minimum conversion time of \( 2^{13} = 8192 \) clock cycles is required. 8192 clock cycles correspond to a CHx_RCOUNT value of 0x0200.

Table 6. Conversion Time Configuration Registers, Channels 0 - 3(1)

<table>
<thead>
<tr>
<th>CHANNEL</th>
<th>REGISTER</th>
<th>FIELD [ BIT(S) ]</th>
<th>CONVERSION TIME</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>RCOUNT_CH0, addr 0x08</td>
<td>CH0_RCOUNT [15:0]</td>
<td>(CH0_RCOUNT \times 16)/fREF0</td>
</tr>
<tr>
<td>1</td>
<td>RCOUNT_CH1, addr 0x09</td>
<td>CH1_RCOUNT [15:0]</td>
<td>(CH1_RCOUNT \times 16)/fREF1</td>
</tr>
<tr>
<td>2</td>
<td>RCOUNT_CH2, addr 0x0A</td>
<td>CH2_RCOUNT [15:0]</td>
<td>(CH2_RCOUNT \times 16)/fREF2</td>
</tr>
<tr>
<td>3</td>
<td>RCOUNT_CH3, addr 0x0B</td>
<td>CH3_RCOUNT [15:0]</td>
<td>(CH3_RCOUNT \times 16)/fREF3</td>
</tr>
</tbody>
</table>

(1) Channels 2 and 3 are available only for FDC2114 and FDC2214.

The typical channel switch delay time between the end of conversion and the beginning of sensor activation of the subsequent channel is:

\[ \text{Channel Switch Delay} = 692 \text{ ns} + 5 / \text{fref} \]  

The deterministic conversion time of the FDC allows data polling at a fixed interval. For example, if the programmed SETTLECOUNT is 128 FREF cycles (SETTLECOUNT = 0x0008) and RCOUNT is 512 FREF cycles (RCOUNT=0x0020), then one conversion takes 3.2 ms (sensor-activation time) + 12.8 ms (conversion time) + 0.8 µs (channel-switch delay) = 16.0 ms per channel. If the FDC is configured for dual-channel operation by setting AUTOSCAN_EN = 1 and RR_SEQUENCE = 00, then one full set of conversion results will be available from the data registers every 32 ms.

A data ready flag (DRDY) is also available for interrupt driven system designs (see the STATUS register description in Register Maps).

7.3.2.1 Gain and Offset (FDC2112, FDC2114 only)

The FDC2112 and FDC2114 have internal 16-bit data converters, but the standard conversion output word width is only 12 bits; therefore only 12 of the 16 bits are available from the data registers. By default, the gain feature is disabled and the DATA registers contain the 12 MSBs of the 16-bit word. However, it is possible to shift the data output by up to 4 bits. Figure 15 shows the segment of the 16-bit sample that is reported for each possible gain setting.
Figure 15. Conversion Data Output Gain

For systems in which the sensor signal variation is less than 25% of the full-scale range, the FDC can report conversion results with higher resolution by setting the output gain. The output gain is applied to all device channels. An output gain can be used to apply a 2-bit, 3-bit, or 4-bit shift to the output code for all channels, allowing access to the 4 LSBs of the original 16-bit result. The MSBs of the sample are shifted out when a gain is applied. Do not use the output gain if the MSBs of any active channel are toggling, as the MSBs for that channel will be lost when gain is applied.

Example: If the conversion result for a channel is 0x07A3, with OUTPUT_GAIN = 0x0, the reported output code is 0x07A. If OUTPUT_GAIN is set to 0x3 in the same condition, then the reported output code is 0x7A3. The original 4 MSBs (0x0) are no longer accessible.

Table 7. Output Gain Register (FDC2112 and FDC2114 only)

<table>
<thead>
<tr>
<th>CHANNEL(1)</th>
<th>REGISTER</th>
<th>FIELD [ BIT(S) ]</th>
<th>VALUES</th>
<th>EFFECTIVE RESOLUTION (BITS)</th>
<th>OUTPUT RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>All</td>
<td>RESET_DEV, addr 0x1C</td>
<td>OUTPUT_GAIN [ 10:9 ]</td>
<td>00 (default): Gain =1 (0 bits shift)</td>
<td>12</td>
<td>100% full scale</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: Gain = 4 (2 bits left shift)</td>
<td>14</td>
<td>25% full scale</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10: Gain = 8 (3 bits left shift)</td>
<td>15</td>
<td>12.5% full scale</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Gain = 16 (4 bits left shift)</td>
<td>16</td>
<td>6.25% full scale</td>
</tr>
</tbody>
</table>

(1) Channels 2 and 3 are available for FDC2114 only.

An offset value may be subtracted from each DATA value to compensate for a frequency offset or maximize the dynamic range of the sample data. The offset values should be \( < \frac{f_{\text{SENSORx_MIN}}}{f_{\text{REFx}}} \). Otherwise, the offset might be so large that it masks the LSBs which are changing.
The sensor capacitance $C_{\text{SENSE}}$ of a differential sensor configuration can be determined by:

$$C_{\text{SENSE}} = \left( \frac{1}{L} \right) \times \left( \frac{f_{\text{SENSORx}}}{2\pi} \right)^2 - C$$

where

- $C$ = parallel sensor capacitance (see Figure 55) \hspace{1cm} (7)

The FDC2112 and FDC2114 sensor frequency $f_{\text{SENSORx}}$ can be determined by:

$$f_{\text{SENSORx}} = \left( \frac{\text{CHx_FIN_SEL} \times f_{\text{REFx}} \times \text{DATAx}}{2^{(12 - \text{OUTPUT_GAIN})}} + \frac{\text{CHx_OFFSET}}{2^{16}} \right)$$

where

- $\text{DATAx}$ = Conversion result from the DATA_CHx register
- $\text{CHx OFFSET}$ = Offset value set in the OFFSET_CHx register
- OUTPUT_GAIN = output multiplication factor set in the RESET_DEVICE.OUTPUT_GAIN register \hspace{1cm} (8)

The FDC2212 and FDC2214 sensor frequency $f_{\text{SENSORx}}$ can be determined by:

$$f_{\text{SENSORx}} = \left( \frac{\text{CHx_FIN_SEL} \times f_{\text{REFx}} \times \text{DATAx}}{2^{28}} \right)$$

where

- $\text{DATAx}$ = Conversion result from the DATA_CHx register \hspace{1cm} (9)
7.3.3 Current Drive Control Registers

The registers listed in Table 9 are used to control the sensor drive current. The recommendations listed in the last column of the table should be followed.

<table>
<thead>
<tr>
<th>CHANNEL(^{(1)})</th>
<th>REGISTER</th>
<th>FIELD [ BIT(S) ]</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>All</td>
<td>CONFIG, addr 0x1A</td>
<td>SENSOR_Activate_SEL [11]</td>
<td>Sets current drive for sensor activation. Recommended value is b0 (full current mode).</td>
</tr>
<tr>
<td>0</td>
<td>CONFIG, addr 0x1A</td>
<td>HIGH_CURRENT_DRV [6]</td>
<td>b0 = normal current drive (1.5 mA) b1 = increased current drive (&gt; 1.5 mA) for Ch 0 in single channel mode only. Cannot be used in multi-channel mode.</td>
</tr>
<tr>
<td>0</td>
<td>DRIVE_CURRENT_CH0, addr 0x1E</td>
<td>CH0_IDRIVE [15:11]</td>
<td>Drive current used during the settling and conversion time for Ch. 0. Set such that 1.2 V ≤ sensor oscillation amplitude (pk) ≤ 1.8 V</td>
</tr>
<tr>
<td>1</td>
<td>DRIVE_CURRENT_CH1, addr 0x1F</td>
<td>CH1_IDRIVE [15:11]</td>
<td>Drive current used during the settling and conversion time for Ch. 1. Set such that 1.2 V ≤ sensor oscillation amplitude (pk) ≤ 1.8 V</td>
</tr>
<tr>
<td>2</td>
<td>DRIVE_CURRENT_CH2, addr 0x20</td>
<td>CH2_IDRIVE [15:11]</td>
<td>Drive current used during the settling and conversion time for Ch. 2. Set such that 1.2 V ≤ sensor oscillation amplitude (pk) ≤ 1.8 V</td>
</tr>
<tr>
<td>3</td>
<td>DRIVE_CURRENT_CH3, addr 0x21</td>
<td>CH3_IDRIVE [15:11]</td>
<td>Drive current used during the settling and conversion time for Ch. 3. Set such that 1.2 V ≤ sensor oscillation amplitude (pk) ≤ 1.8 V</td>
</tr>
</tbody>
</table>

(1) Channels 2 and 3 are available for FDC2114 and FDC2214 only.

The CHx_IDRIVE field should be programmed such that the sensor oscillates at an amplitude between 1.2 Vpk (VSENSORMIN) and 1.8 Vpk (VSENSORMAX). An IDRIVE value of 00000 corresponds to 16 µA, and IDRIVE = b11111 corresponds to 1563 µA.

A high sensor current drive mode can be enabled to drive sensor coils with > 1.5 mA on channel 0, only in single channel mode. This feature can be used when the sensor minimum recommended oscillation amplitude of 1.2 V cannot be achieved with the highest IDRIVE setting. Set the HIGH_CURRENT_DRV register bit to b1 to enable this mode.

7.3.4 Device Status Registers

The registers listed in Table 10 may be used to read device status.

<table>
<thead>
<tr>
<th>CHANNEL(^{(1)})</th>
<th>REGISTER</th>
<th>FIELDS [ BIT(S) ]</th>
<th>VALUES</th>
</tr>
</thead>
<tbody>
<tr>
<td>All</td>
<td>STATUS, addr 0x18</td>
<td>12 fields are available that contain various status bits [15:0]</td>
<td>Refer to Register Maps for a description of the individual status bits.</td>
</tr>
<tr>
<td>All</td>
<td>STATUS_CONFIG, addr 0x19</td>
<td>12 fields are available that are used to configure status reporting [15:0]</td>
<td>Refer to Register Maps for a description of the individual error configuration bits.</td>
</tr>
</tbody>
</table>

(1) Channels 2 and 3 are available for FDC2114 and FDC2214 only.

See the STATUS and STATUS_CONFIG register description in Register Maps. These registers can be configured to trigger an interrupt on the INTB pin for certain events. The following conditions must be met:

1. The error or status register must be unmasked by enabling the appropriate register bit in the STATUS_CONFIG register
2. The INTB function must be enabled by setting CONFIG.INTB_DIS to 0
When a bit field in the STATUS register is set, the entire STATUS register content is held until read or until the DATA_CHx register is read. Reading also de-asserts INTB.

Interrupts are cleared by one of the following events:
1. Entering sleep mode
2. Power-on reset (POR)
3. Device enters shutdown mode (SD is asserted)
4. S/W reset
5. I2C read of the STATUS register: Reading the STATUS register clears any error status bit set in STATUS along with the ERR_CHAN field and de-assert INTB

Setting register CONFIG.INTB_DIS to b1 disables the INTB function and holds the INTB pin high.

### 7.3.5 Input Deglitch Filter

The input deglitch filter suppresses EMI and ringing above the sensor frequency. It does not impact the conversion result as long as its bandwidth is configured to be above the maximum sensor frequency. The input deglitch filter can be configured in MUX_CONFIG.DEGLITCH register field as shown in Table 11. For optimal performance, TI recommends selection of the lowest setting that exceeds the sensor oscillation frequency. For example, if the maximum sensor frequency is 2 MHz, choose MUX_CONFIG.DEGLITCH = b100 (3.3 MHz).

<table>
<thead>
<tr>
<th>CHANNEL (1)</th>
<th>MUX_CONFIG.DEGLITCH (addr 0x1B) REGISTER VALUE</th>
<th>DEGLITCH FREQUENCY</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALL</td>
<td>001</td>
<td>1 MHz</td>
</tr>
<tr>
<td>ALL</td>
<td>100</td>
<td>3.3 MHz</td>
</tr>
<tr>
<td>ALL</td>
<td>101</td>
<td>10 MHz</td>
</tr>
<tr>
<td>ALL</td>
<td>011</td>
<td>33 MHz</td>
</tr>
</tbody>
</table>

(1) Channels 2 and 3 are available for FDC2114 / FDC2214 only.

### 7.4 Device Functional Modes

#### 7.4.1 Start-Up Mode

When the FDC powers up, it enters into sleep mode and waits for configuration. Once the device is configured, exit sleep mode by setting CONFIG.SLEEP_MODE_EN to b0.

TI recommends configuring the FDC while in sleep mode. If a setting on the FDC needs to be changed, return the device to sleep mode, change the appropriate register, and then exit sleep mode.

#### 7.4.2 Normal (Conversion) Mode

When operating in the normal (conversion) mode, the FDC is periodically sampling the frequency of the sensor(s) and generating sample outputs for the active channel(s).

#### 7.4.3 Sleep Mode

Sleep mode is entered by setting the CONFIG.SLEEP_MODE_EN register field to 1. While in this mode, the device configuration is maintained. To exit sleep mode, set the CONFIG.SLEEP_MODE_EN register field to 0. After setting CONFIG.SLEEP_MODE_EN to b0, sensor activation for the first conversion begins after 16,384 f_{INT} clock cycles. While in sleep mode the I2C interface is functional so that register reads and writes can be performed. While in sleep mode, no conversions are performed. In addition, entering sleep mode will clear conversion results, any error condition, and de-assert the INTB pin.

#### 7.4.4 Shutdown Mode

When the SD pin is set to high, the FDC enters shutdown mode. Shutdown mode is the lowest power state. To exit shutdown mode, set the SD pin to low. Entering shutdown mode returns all registers to their default state.
Device Functional Modes (continued)

While in shutdown mode, no conversions are performed. In addition, entering shutdown mode clears any error condition and de-assert the INTB pin. While the device is in shutdown mode, it is not possible to read to or write from the device via the I2C interface.

7.4.4.1 Reset

The FDC can be reset by writing to RESET_DEV. Any active conversion stops, and all register values return to their default value. This register bit always returns 0 when read.

7.5 Programming

The FDC device uses an I2C interface to access control and data registers.

7.5.1 I2C Interface Specifications

The FDC uses an extended start sequence with I2C for register access. The maximum speed of the I2C interface is 400 kbit/s. This sequence follows the standard I2C 7-bit slave address followed by an 8-bit pointer register byte to set the register address. When the ADDR pin is set low, the FDC I2C address is 0x2A; when the ADDR pin is set high, the FDC I2C address is 0x2B. The ADDR pin must not change state after the FDC exits Shutdown Mode.

![I2C Write Register Sequence](image1)

**Figure 16. I2C Write Register Sequence**

![I2C Read Register Sequence](image2)

**Figure 17. I2C Read Register Sequence**
### 7.6 Register Maps

#### 7.6.1 Register List

Fields indicated with Reserved must be written only with indicated values, otherwise improper device operation may occur. The R/W column indicates the Read-Write status of the corresponding field. A ‘R/W’ entry indicates read and write capability, a ‘R’ indicates read-only, and a ‘W’ indicates write-only.

**Figure 18. Register List**

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>NAME</th>
<th>DEFAULT VALUE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>DATA_CH0</td>
<td>0x0000</td>
<td>Channel 0 Conversion Result and status (FDC2112 / FDC2114 only)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0x0000</td>
<td>Channel 0 MSB Conversion Result and status (FDC2212 / FDC2214 only)</td>
</tr>
<tr>
<td>0x01</td>
<td>DATA_LSB_CH0</td>
<td>0x0000</td>
<td>Channel 0 LSB Conversion Result. Must be read after Register address 0x00</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(FDC2212 / FDC2214 only)</td>
</tr>
<tr>
<td>0x02</td>
<td>DATA_CH1</td>
<td>0x0000</td>
<td>Channel 1 Conversion Result and status (FDC2112 / FDC2114 only)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0x0000</td>
<td>Channel 1 MSB Conversion Result and status (FDC2212 / FDC2214 only)</td>
</tr>
<tr>
<td>0x03</td>
<td>DATA_LSB_CH1</td>
<td>0x0000</td>
<td>Channel 1 LSB Conversion Result. Must be read after Register address 0x02</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(FDC2212 / FDC2214 only)</td>
</tr>
<tr>
<td>0x04</td>
<td>DATA_CH2</td>
<td>0x0000</td>
<td>Channel 2 Conversion Result and status (FDC2114 only)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0x0000</td>
<td>Channel 2 MSB Conversion Result and status (FDC2214 only)</td>
</tr>
<tr>
<td>0x05</td>
<td>DATA_LSB_CH2</td>
<td>0x0000</td>
<td>Channel 2 LSB Conversion Result. Must be read after Register address 0x04</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(FDC2214 only)</td>
</tr>
<tr>
<td>0x06</td>
<td>DATA_CH3</td>
<td>0x0000</td>
<td>Channel 3 Conversion Result and status (FDC2114 only)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0x0000</td>
<td>Channel 3 MSB Conversion Result and status (FDC2214 only)</td>
</tr>
<tr>
<td>0x07</td>
<td>DATA_LSB_CH3</td>
<td>0x0000</td>
<td>Channel 3 LSB Conversion Result. Must be read after Register address 0x06</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(FDC2214 only)</td>
</tr>
<tr>
<td>0x08</td>
<td>RCOUNT_CH0</td>
<td>0x0080</td>
<td>Reference Count setting for Channel 0</td>
</tr>
<tr>
<td>0x09</td>
<td>RCOUNT_CH1</td>
<td>0x0080</td>
<td>Reference Count setting for Channel 1</td>
</tr>
<tr>
<td>0x0A</td>
<td>RCOUNT_CH2</td>
<td>0x0080</td>
<td>Reference Count setting for Channel 2 (FDC2114 / FDC2214 only)</td>
</tr>
<tr>
<td>0x0B</td>
<td>RCOUNT_CH3</td>
<td>0x0080</td>
<td>Reference Count setting for Channel 3 (FDC2114 / FDC2214 only)</td>
</tr>
<tr>
<td>0x0C</td>
<td>OFFSET_CH0</td>
<td>0x0000</td>
<td>Offset value for Channel 0 (FDC2112 / FDC2114 only)</td>
</tr>
<tr>
<td>0x0D</td>
<td>OFFSET_CH1</td>
<td>0x0000</td>
<td>Offset value for Channel 1 (FDC2112 / FDC2114 only)</td>
</tr>
<tr>
<td>0x0E</td>
<td>OFFSET_CH2</td>
<td>0x0000</td>
<td>Offset value for Channel 2 (FDC2114 only)</td>
</tr>
<tr>
<td>0x0F</td>
<td>OFFSET_CH3</td>
<td>0x0000</td>
<td>Offset value for Channel 3 (FDC2114 only)</td>
</tr>
<tr>
<td>0x10</td>
<td>SETTLECOUNT_CH0</td>
<td>0x0000</td>
<td>Channel 0 Settling Reference Count</td>
</tr>
<tr>
<td>0x11</td>
<td>SETTLECOUNT_CH1</td>
<td>0x0000</td>
<td>Channel 1 Settling Reference Count</td>
</tr>
<tr>
<td>0x12</td>
<td>SETTLECOUNT_CH2</td>
<td>0x0000</td>
<td>Channel 2 Settling Reference Count</td>
</tr>
<tr>
<td>0x13</td>
<td>SETTLECOUNT_CH3</td>
<td>0x0000</td>
<td>Channel 3 Settling Reference Count</td>
</tr>
<tr>
<td>0x14</td>
<td>CLOCK_DIVIDERS_CH0</td>
<td>0x0000</td>
<td>Reference divider settings for Channel 0</td>
</tr>
<tr>
<td>0x15</td>
<td>CLOCK_DIVIDERS_CH1</td>
<td>0x0000</td>
<td>Reference divider settings for Channel 1</td>
</tr>
<tr>
<td>0x16</td>
<td>CLOCK_DIVIDERS_CH2</td>
<td>0x0000</td>
<td>Reference divider settings for Channel 2 (FDC2114 / FDC2214 only)</td>
</tr>
<tr>
<td>0x17</td>
<td>CLOCK_DIVIDERS_CH3</td>
<td>0x0000</td>
<td>Reference divider settings for Channel 3 (FDC2114 / FDC2214 only)</td>
</tr>
<tr>
<td>0x18</td>
<td>STATUS</td>
<td>0x0000</td>
<td>Device Status Reporting</td>
</tr>
<tr>
<td>0x19</td>
<td>STATUS_CONFIG</td>
<td>0x0000</td>
<td>Device Status Reporting Configuration</td>
</tr>
<tr>
<td>0x1A</td>
<td>CONFIG</td>
<td>0x2801</td>
<td>Conversion Configuration</td>
</tr>
<tr>
<td>0x1B</td>
<td>MUX_CONFIG</td>
<td>0x020F</td>
<td>Channel Multiplexing Configuration</td>
</tr>
<tr>
<td>0x1C</td>
<td>RESET_DEV</td>
<td>0x0000</td>
<td>Reset Device</td>
</tr>
<tr>
<td>0x1E</td>
<td>DRIVE_CURRENT_CH0</td>
<td>0x0000</td>
<td>Channel 0 sensor current drive configuration</td>
</tr>
<tr>
<td>0x1F</td>
<td>DRIVE_CURRENT_CH1</td>
<td>0x0000</td>
<td>Channel 1 sensor current drive configuration</td>
</tr>
<tr>
<td>0x20</td>
<td>DRIVE_CURRENT_CH2</td>
<td>0x0000</td>
<td>Channel 2 sensor current drive configuration</td>
</tr>
<tr>
<td>0x21</td>
<td>DRIVE_CURRENT_CH3</td>
<td>0x0000</td>
<td>Channel 3 sensor current drive configuration</td>
</tr>
<tr>
<td>0x7E</td>
<td>MANUFACTURER_ID</td>
<td>0x5449</td>
<td>Manufacturer ID</td>
</tr>
<tr>
<td>0x7F</td>
<td>DEVICE_ID</td>
<td>0x3054</td>
<td>Device ID (FDC2112, FDC2114 only)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0x3055</td>
<td>Device ID (FDC2212, FDC2214 only)</td>
</tr>
</tbody>
</table>
7.6.2 Address 0x00, DATA_CH0

Figure 19. Address 0x00, DATA_CH0

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:14</td>
<td>RESERVED</td>
<td>R</td>
<td>00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>13</td>
<td>CH0_ERR_WD</td>
<td>R</td>
<td>0</td>
<td>Channel 0 Conversion Watchdog Timeout Error Flag. Cleared by reading the bit.</td>
</tr>
<tr>
<td>12</td>
<td>CH0_ERR_AW</td>
<td>R</td>
<td>0</td>
<td>Channel 0 Amplitude Warning. Cleared by reading the bit.</td>
</tr>
<tr>
<td>11:0</td>
<td>DATA0</td>
<td>R</td>
<td>0000 0000</td>
<td>Channel 0 Conversion Result</td>
</tr>
</tbody>
</table>

Table 12. Address 0x00, DATA_CH0 Field Descriptions

7.6.3 Address 0x01, DATA_LSB_CH0 (FDC2212 / FDC2214 only)

Figure 20. Address 0x01, DATA_LSB_CH0

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:0</td>
<td>DATA0[15:0]</td>
<td>R</td>
<td>0000 0000</td>
<td>Channel 0 Conversion Result</td>
</tr>
</tbody>
</table>

Table 13. Address 0x01, DATA_CH0 Field Descriptions

7.6.4 Address 0x02, DATA_CH1

Figure 21. Address 0x02, DATA_CH1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:14</td>
<td>RESERVED</td>
<td>R</td>
<td>00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>13</td>
<td>CH1_ERR_WD</td>
<td>R</td>
<td>0</td>
<td>Channel 1 Conversion Watchdog Timeout Error Flag. Cleared by reading the bit.</td>
</tr>
<tr>
<td>12</td>
<td>CH1_ERR_AW</td>
<td>R</td>
<td>0</td>
<td>Channel 1 Amplitude Warning. Cleared by reading the bit.</td>
</tr>
<tr>
<td>11:0</td>
<td>DATA1</td>
<td>R</td>
<td>0000 0000</td>
<td>Channel 1 Conversion Result</td>
</tr>
</tbody>
</table>

Table 14. Address 0x02, DATA_CH1 Field Descriptions
7.6.5 Address 0x03, DATA_LSB_CH1 (FDC2212 / FDC2214 only)

Figure 22. Address 0x03, DATA_LSB_CH1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:0</td>
<td>DATA1[15:0]</td>
<td>R</td>
<td>0000 0000</td>
<td>Channel 1 Conversion Result</td>
</tr>
</tbody>
</table>

7.6.6 Address 0x04, DATA_CH2 (FDC2114, FDC2214 only)

Figure 23. Address 0x04, DATA_CH2

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:14</td>
<td>RESERVED</td>
<td>R</td>
<td>00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>13</td>
<td>CH2_ERR_WD</td>
<td>R</td>
<td>0</td>
<td>Channel 2 Conversion Watchdog Timeout Error Flag. Cleared by reading the bit.</td>
</tr>
<tr>
<td>12</td>
<td>CH2_ERR_AW</td>
<td>R</td>
<td>0</td>
<td>Channel 2 Amplitude Warning. Cleared by reading the bit.</td>
</tr>
<tr>
<td>11:0</td>
<td>DATA2 (FDC2112 / FDC2114 only)</td>
<td>R</td>
<td>0000 0000</td>
<td>Channel 2 Conversion Result</td>
</tr>
</tbody>
</table>

7.6.7 Address 0x05, DATA_LSB_CH2 (FDC2214 only)

Figure 24. Address 0x05, DATA_LSB_CH2

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:0</td>
<td>DATA2[15:0]</td>
<td>R</td>
<td>0000 0000</td>
<td>Channel 2 Conversion Result</td>
</tr>
</tbody>
</table>
7.6.8 Address 0x06, DATA_CH3 (FDC2114, FDC2214 only)

Figure 25. Address 0x06, DATA_CH3

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:14</td>
<td>RESERVED</td>
<td>R</td>
<td>00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>13</td>
<td>CH3_ERR_WD</td>
<td>R</td>
<td>0</td>
<td>Channel 3 Conversion Watchdog Timeout Error Flag. Cleared by reading the bit.</td>
</tr>
<tr>
<td>12</td>
<td>CH3_ERR_AW</td>
<td>R</td>
<td>0</td>
<td>Channel 3 Amplitude Warning. Cleared by reading the bit.</td>
</tr>
<tr>
<td>11:0</td>
<td>DATA3</td>
<td>R</td>
<td>0000 0000 0000</td>
<td>Channel 3 Conversion Result</td>
</tr>
</tbody>
</table>

Table 18. Address 0x06, DATA_CH3 Field Descriptions

7.6.9 Address 0x07, DATA_LSB_CH3 (FDC2214 only)

Figure 26. Address 0x07, DATA_LSB_CH3

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:0</td>
<td>DATA3[15:0]</td>
<td>R</td>
<td>0000 0000 0000</td>
<td>Channel 3 Conversion Result</td>
</tr>
</tbody>
</table>

Table 19. Address 0x07, DATA_CH3 Field Descriptions

7.6.10 Address 0x08, RCOUNT_CH0

Figure 27. Address 0x08, RCOUNT_CH0

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:0</td>
<td>CH0_RCOUNT</td>
<td>R/W</td>
<td>0000 0000 1000 0000</td>
<td>Channel 0 Reference Count Conversion Interval Time 0x0000-0x00FF: Reserved 0x0100-0xFFFF: Conversion Time (tC0) = (CH0_RCOUNT×16)/fREF0</td>
</tr>
</tbody>
</table>

Table 20. Address 0x08, RCOUNT_CH0 Field Descriptions
7.6.11 Address 0x09, RCOUNT_CH1

Figure 28. Address 0x09, RCOUNT_CH1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:0</td>
<td>CH1_RCOUNT</td>
<td>R/W</td>
<td>0000 0000 1000 0000</td>
<td>Channel 1 Reference Count Conversion Interval Time</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0000-0x00FF: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0100-0xFFFF: Conversion Time (t_{C1}) = (CH1_RCOUNT \times 16)/f_{REF1}</td>
</tr>
</tbody>
</table>

7.6.12 Address 0x0A, RCOUNT_CH2 (FDC2114, FDC2214 only)

Figure 29. Address 0x0A, RCOUNT_CH2

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:0</td>
<td>CH2_RCOUNT</td>
<td>R/W</td>
<td>0000 0000 1000 0000</td>
<td>Channel 2 Reference Count Conversion Interval Time</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0000-0x00FF: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0100-0xFFFF: Conversion Time (t_{C2}) = (CH2_RCOUNT \times 16)/f_{REF2}</td>
</tr>
</tbody>
</table>

7.6.13 Address 0x0B, RCOUNT_CH3 (FDC2114, FDC2214 only)

Figure 30. Address 0x0B, RCOUNT_CH3

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:0</td>
<td>CH3_RCOUNT</td>
<td>R/W</td>
<td>0000 0000 1000 0000</td>
<td>Channel 3 Reference Count Conversion Interval Time</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0000-0x00FF: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0100-0xFFFF: Conversion Time (t_{C3}) = (CH3_RCOUNT \times 16)/f_{REF3}</td>
</tr>
</tbody>
</table>
7.6.14 Address 0x0C, OFFSET_CH0 (FDC21112 / FDC2114 only)

Figure 31. Address 0x0C, CH0_OFFSET

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>CH0_OFFSET</td>
<td>R/W</td>
<td>0000 0000</td>
<td>Channel 0 Conversion Offset. fOFFSET_0 = (CH0_OFFSET/2^16) * fREF0</td>
</tr>
</tbody>
</table>

Table 24. CH0_OFFSET Field Descriptions

7.6.15 Address 0x0D, OFFSET_CH1 (FDC21112 / FDC2114 only)

Figure 32. Address 0x0D, OFFSET_CH1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>CH1_OFFSET</td>
<td>R/W</td>
<td>0000 0000</td>
<td>Channel 1 Conversion Offset. fOFFSET_1 = (CH1_OFFSET/2^16) * fREF1</td>
</tr>
</tbody>
</table>

Table 25. Address 0x0D, OFFSET_CH1 Field Descriptions

7.6.16 Address 0x0E, OFFSET_CH2 (FDC2114 only)

Figure 33. Address 0x0E, OFFSET_CH2

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>CH2_OFFSET</td>
<td>R/W</td>
<td>0000 0000</td>
<td>Channel 2 Conversion Offset. fOFFSET_2 = (CH2_OFFSET/2^16) * fREF2</td>
</tr>
</tbody>
</table>

Table 26. Address 0x0E, OFFSET_CH2 Field Descriptions
7.6.17  Address 0x0F, OFFSET CH3 (FDC2114 only)

Figure 34. Address 0x0F, OFFSET CH3

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:0</td>
<td>CH3_OFFSET</td>
<td>R/W</td>
<td>0000 0000 0000 0000</td>
<td>Channel 3 Conversion Offset. fOFFSET_3 = (CH3_OFFSET/2¹⁶) / fREF3</td>
</tr>
</tbody>
</table>

7.6.18  Address 0x10, SETTLECOUNT CH0

Figure 35. Address 0x10, SETTLECOUNT CH0

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 15:0 | CH0_SETTLECOUNT | R/W   | 0000 0000 0000 0000 | Channel 0 Conversion Settling  
|      |          |       |                                 | The FDC will use this settling time to allow the LC sensor to stabilize before initiation of a conversion on Channel 0. If the amplitude has not settled prior to the conversion start, an Amplitude warning will be generated if reporting of this type of warning is enabled.  
|      |          |       |                                 | 0x000: Settle Time (tS0) = 32 / fREF0  
|      |          |       |                                 | 0x001: Settle Time (tS0) = 32 / fREF0  
|      |          |       |                                 | 0x002 - 0xFFFF: Settle Time (tS0) = (CH0_SETTLECOUNT x 16) / fREF0 |

7.6.19  Address 0x11, SETTLECOUNT CH1

Figure 36. Address 0x11, SETTLECOUNT CH1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 15:0 | CH1_SETTLECOUNT | R/W   | 0000 0000 0000 0000 | Channel 1 Conversion Settling  
|      |          |       |                                 | The FDC will use this settling time to allow the LC sensor to stabilize before initiation of a conversion on Channel 1. If the amplitude has not settled prior to the conversion start, an Amplitude warning will be generated if reporting of this type of warning is enabled.  
|      |          |       |                                 | 0x000: Settle Time (tS1) = 32 / fREF1  
|      |          |       |                                 | 0x001: Settle Time (tS1) = 32 / fREF1  
|      |          |       |                                 | 0x002 - 0xFFFF: Settle Time (tS1) = (CH1_SETTLECOUNT x 16) / fREF1 |
7.6.20  Address 0x12, SETTLECOUNT_CH2 (FDC2114, FDC2214 only)

Figure 37. Address 0x12, SETTLECOUNT_CH2

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 15:0| CH2_SETTLECOUNT | R/W  | 0000 0000 0000 0000 | Channel 2 Conversion Settling Time 
The FDC will use this settling time to allow the LC sensor to stabilize before initiation of a conversion on Channel 2. If the amplitude has not settled prior to the conversion start, an Amplitude warning will be generated if reporting of this type of warning is enabled.
0x0000: Settle Time (t\textsubscript{S2}) = 32 ÷ f\textsubscript{REF2}
0x0001: Settle Time (t\textsubscript{S2}) = 32 ÷ f\textsubscript{REF2}
0x0002 - 0xFFFF: Settle Time (t\textsubscript{S2}) = (CH2_SETTLECOUNT \times 16) ÷ f\textsubscript{REF2} |

7.6.21  Address 0x13, SETTLECOUNT_CH3 (FDC2114, FDC2214 only)

Figure 38. Address 0x13, SETTLECOUNT_CH3

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 15:0| CH3_SETTLECOUNT | R/W  | 0000 0000 0000 0000 | Channel 3 Conversion Settling Time 
The FDC will use this settling time to allow the LC sensor to stabilize before initiation of a conversion on Channel 3. If the amplitude has not settled prior to the conversion start, an Amplitude warning will be generated if reporting of this type of warning is enabled.
0x0000: Settle Time (t\textsubscript{S3}) = 32 ÷ f\textsubscript{REF3}
0x0001: Settle Time (t\textsubscript{S3}) = 32 ÷ f\textsubscript{REF3}
0x0002 - 0xFFFF: Settle Time (t\textsubscript{S3}) = (CH3_SETTLECOUNT \times 16) ÷ f\textsubscript{REF3} |
7.6.22 Address 0x14, CLOCK_DIVIDERS_CH0

**Figure 39. Address 0x14, CLOCK_DIVIDERS_CH0**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:14</td>
<td>RESERVED</td>
<td>R/W</td>
<td>00</td>
<td>Reserved. Set to b00.</td>
</tr>
<tr>
<td>13:12</td>
<td>CH0_FIN_SEL</td>
<td>R/W</td>
<td>00</td>
<td>Channel 0 Sensor frequency select for differential sensor configuration:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b01: divide by 1. Choose for sensor frequencies between 0.01 MHz and 8.75 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b10: divide by 2. Choose for sensor frequencies between 5 MHz and 10 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>for single-ended sensor configuration:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b10: divide by 2. Choose for sensor frequencies between 0.01 MHz and 10 MHz</td>
</tr>
<tr>
<td>11:10</td>
<td>RESERVED</td>
<td>R/W</td>
<td>00</td>
<td>Reserved. Set to b00.</td>
</tr>
<tr>
<td>9:0</td>
<td>CH0_FREF_DIVIDER</td>
<td>R/W</td>
<td>00 0000 0000</td>
<td>Channel 0 Reference Divider Sets the divider for Channel 0 reference. Use this to scale the maximum conversion frequency. b00'0000'0000: Reserved. Do not use. CH0_FREF_DIVIDER ≥ b00'0000'0001: fREF0 = fCLK / CH0_FREF_DIVIDER</td>
</tr>
</tbody>
</table>

7.6.23 Address 0x15, CLOCK_DIVIDERS_CH1

**Figure 40. Address 0x15, CLOCK_DIVIDERS_CH1**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:14</td>
<td>RESERVED</td>
<td>R/W</td>
<td>00</td>
<td>Reserved. Set to b00.</td>
</tr>
<tr>
<td>13:12</td>
<td>CH1_FIN_SEL</td>
<td>R/W</td>
<td>0000</td>
<td>Channel 1 Sensor frequency select for differential sensor configuration:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b01: divide by 1. Choose for sensor frequencies between 0.01 MHz and 8.75 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b10: divide by 2. Choose for sensor frequencies between 5 MHz and 10 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>for single-ended sensor configuration:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b10: divide by 2. Choose for sensor frequencies between 0.01 MHz and 10 MHz</td>
</tr>
<tr>
<td>11:10</td>
<td>RESERVED</td>
<td>R/W</td>
<td>00</td>
<td>Reserved. Set to b00.</td>
</tr>
<tr>
<td>9:0</td>
<td>CH1_FREF_DIVIDER</td>
<td>R/W</td>
<td>00 0000 0000</td>
<td>Channel 1 Reference Divider Sets the divider for Channel 1 reference. Use this to scale the maximum conversion frequency. b00'0000'0000: Reserved. Do not use. CH1_FREF_DIVIDER ≥ b00'0000'0001: fREF1 = fCLK / CH1_FREF_DIVIDER</td>
</tr>
</tbody>
</table>
### 7.6.24 Address 0x16, CLOCK_DIVIDERS_CH2 (FDC2114, FDC2214 only)

**Figure 41. Address 0x16, CLOCK_DIVIDERS_CH2**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:14</td>
<td>RESERVED</td>
<td>R/W</td>
<td>00</td>
<td>Reserved. Set to b00.</td>
</tr>
<tr>
<td>13:12</td>
<td>CH2_FIN_SEL</td>
<td>R/W</td>
<td>0000</td>
<td>Channel 2 Sensor frequency select for differential sensor configuration:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b01: divide by 1. Choose for sensor frequencies between 0.01 MHz and 8.75 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b10: divide by 2. Choose for sensor frequencies between 5 MHz and 10 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>for single-ended sensor configuration:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b10: divide by 2. Choose for sensor frequencies between 0.01 MHz and 10 MHz</td>
</tr>
<tr>
<td>11:10</td>
<td>RESERVED</td>
<td>R/W</td>
<td>00</td>
<td>Reserved. Set to b00.</td>
</tr>
<tr>
<td>9:0</td>
<td>CH2_FREF_DIVIDER</td>
<td>R/W</td>
<td>00 0000 0000</td>
<td>Channel 2 Reference Divider Sets the divider for Channel 2 reference. Use this to scale the maximum conversion frequency. b00'0000'0000: Reserved. Do not use. CH2_FREF_DIVIDER ≥ b00'0000'0001: fREF2 = fCLK/CH2_FREF_DIVIDER</td>
</tr>
</tbody>
</table>

### 7.6.25 Address 0x17, CLOCK_DIVIDERS_CH3 (FDC2114, FDC2214 only)

**Figure 42. Address 0x17, CLOCK_DIVIDERS_CH3**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:14</td>
<td>RESERVED</td>
<td>R/W</td>
<td>00</td>
<td>Reserved. Set to b00.</td>
</tr>
<tr>
<td>13:12</td>
<td>CH3_FIN_SEL</td>
<td>R/W</td>
<td>0000</td>
<td>Channel 3 Sensor frequency select for differential sensor configuration:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b01: divide by 1. Choose for sensor frequencies between 0.01 MHz and 8.75 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b10: divide by 2. Choose for sensor frequencies between 5 MHz and 10 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>for single-ended sensor configuration:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b10: divide by 2. Choose for sensor frequencies between 0.01 MHz and 10 MHz</td>
</tr>
<tr>
<td>11:10</td>
<td>RESERVED</td>
<td>R/W</td>
<td>00</td>
<td>Reserved. Set to b00.</td>
</tr>
<tr>
<td>9:0</td>
<td>CH3_FREF_DIVIDER</td>
<td>R/W</td>
<td>00 0000 0000</td>
<td>Channel 3 Reference Divider Sets the divider for Channel 3 reference. Use this to scale the maximum conversion frequency. b00'0000'0000: reserved CH3_FREF_DIVIDER ≥ b00'0000'0001: fREF3 = fCLK/CH3_FREF_DIVIDER</td>
</tr>
</tbody>
</table>
### 7.6.26 Address 0x18, STATUS

#### Figure 43. Address 0x18, STATUS

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:14</td>
<td>ERR_CHAN</td>
<td>R</td>
<td>00</td>
<td>Error Channel</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Indicates which channel has generated a Flag or Error. Once flagged, any</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>reported error is latched and maintained until either the STATUS register or</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the DATA_CHx register corresponding to the Error Channel is read.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b00: Channel 0 is source of flag or error.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b01: Channel 1 is source of flag or error.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b10: Channel 2 is source of flag or error (FDC2114, FDC2214 only).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b11: Channel 3 is source of flag or error (FDC2114, FDC2214 only).</td>
</tr>
<tr>
<td>13:12</td>
<td>RESERVED</td>
<td>R</td>
<td>00</td>
<td>Reserved</td>
</tr>
<tr>
<td>11</td>
<td>ERR_WD</td>
<td>R</td>
<td>0</td>
<td>Watchdog Timeout Error</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b0: No Watchdog Timeout error was recorded since the last read of the STATUS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b1: An active channel has generated a Watchdog Timeout error. Refer to</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>STATUS.ERR_CHAN field to determine which channel is the source of this error.</td>
</tr>
<tr>
<td>10</td>
<td>ERR_AHW</td>
<td>R</td>
<td>0</td>
<td>Amplitude High Warning</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b0: No Amplitude High warning was recorded since the last read of the STATUS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b1: An active channel has generated an Amplitude High warning. Refer to</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>STATUS.ERR_CHAN field to determine which channel is the source of this error.</td>
</tr>
<tr>
<td>9</td>
<td>ERR_ALW</td>
<td>R</td>
<td>0</td>
<td>Amplitude Low Warning</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b0: No Amplitude Low warning was recorded since the last read of the STATUS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b1: An active channel has generated an Amplitude Low warning. Refer to</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>STATUS.ERR_CHAN field to determine which channel is the source of this error.</td>
</tr>
<tr>
<td>8:7</td>
<td>RESERVED</td>
<td>R</td>
<td>00</td>
<td>Reserved</td>
</tr>
<tr>
<td>6</td>
<td>DRDY</td>
<td>R</td>
<td>0</td>
<td>Data Ready Flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b0: No new conversion result was recorded in the STATUS register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b1: A new conversion result is ready. When in Single Channel Conversion,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>this indicates a single conversion is available. When in sequential mode,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>this indicates that a new conversion result for all active channels is now</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>available.</td>
</tr>
<tr>
<td>3</td>
<td>CH0_UNREADCONV</td>
<td>R</td>
<td>0</td>
<td>Channel 0 Unread Conversion b0: No unread conversion is present for Channel 0.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b1: An unread conversion is present for Channel 0.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Read Register DATA_CH0 to retrieve conversion results.</td>
</tr>
<tr>
<td>2</td>
<td>CH1_UNREADCONV</td>
<td>R</td>
<td>0</td>
<td>Channel 1 Unread Conversion b0: No unread conversion is present for Channel 1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b1: An unread conversion is present for Channel 1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Read Register DATA_CH1 to retrieve conversion results.</td>
</tr>
<tr>
<td>1</td>
<td>CH2_UNREADCONV</td>
<td>R</td>
<td>0</td>
<td>Channel 2 Unread Conversion b0: No unread conversion is present for Channel 2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b1: An unread conversion is present for Channel 2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Read Register DATA_CH2 to retrieve conversion results (FDC2114, FDC2214 only)</td>
</tr>
<tr>
<td>0</td>
<td>CH3_UNREADCONV</td>
<td>R</td>
<td>0</td>
<td>Channel 3 Unread Conversion b0: No unread conversion is present for Channel 3.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b1: An unread conversion is present for Channel 3.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Read Register DATA_CH3 to retrieve conversion results (FDC2114, FDC2214 only)</td>
</tr>
</tbody>
</table>
7.6.27 Address 0x19, ERROR_CONFIG

Figure 44. Address 0x19, ERROR_CONFIG

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:14</td>
<td>RESERVED</td>
<td>R/W</td>
<td>00</td>
<td>Reserved (set to b000)</td>
</tr>
<tr>
<td></td>
<td>WD_ERR2OUT</td>
<td>R/W</td>
<td>0</td>
<td>Watchdog Timeout Error to Output Register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b0: Do not report Watchdog Timeout errors in the DATA_CHx registers.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b1: Report Watchdog Timeout errors in the DATA_CHx.CHx_ERR_WD register field corresponding to the channel that generated the error.</td>
</tr>
<tr>
<td></td>
<td>AH_WARN2OUT</td>
<td>R/W</td>
<td>0</td>
<td>Amplitude High Warning to Output Register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b0: Do not report Amplitude High warnings in the DATA_CHx registers.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b1: Report Amplitude High warnings in the DATA_CHx.CHx_ERR_AW register field corresponding to the channel that generated the warning.</td>
</tr>
<tr>
<td></td>
<td>AL_WARN2OUT</td>
<td>R/W</td>
<td>0</td>
<td>Amplitude Low Warning to Output Register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b0: Do not report Amplitude Low warnings in the DATA_CHx registers.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b1: Report Amplitude High warnings in the DATA_CHx.CHx_ERR_AW register field corresponding to the channel that generated the warning.</td>
</tr>
<tr>
<td>10:6</td>
<td>RESERVED</td>
<td>R/W</td>
<td>0 0000</td>
<td>Reserved (set to b0 0000)</td>
</tr>
<tr>
<td>5</td>
<td>WD_ERR2INT</td>
<td>R/W</td>
<td>0</td>
<td>Watchdog Timeout Error to INTB b0: Do not report Under-range errors by asserting INTB pin and STATUS register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b1: Report Watchdog Timeout errors by asserting INTB pin and updating STATUS.ERR_WD register field.</td>
</tr>
<tr>
<td>4:1</td>
<td>Reserved</td>
<td>R/W</td>
<td>0000</td>
<td>Reserved (set to b000)</td>
</tr>
<tr>
<td>0</td>
<td>DRDY_2INT</td>
<td>R/W</td>
<td>0</td>
<td>Data Ready Flag to INTB b0: Do not report Data Ready Flag by asserting INTB pin and STATUS register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b1: Report Data Ready Flag by asserting INTB pin and updating STATUS.DRDY register field.</td>
</tr>
</tbody>
</table>
### Figure 45. Address 0x1A, CONFIG

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 15:14 | ACTIVE_CHAN   | R/W  | 00    | Active channel selection. Selects channel for continuous conversions when MUX_CONFIG.SEQUENTIAL is 0. b00: Perform continuous conversions on Channel 0  
b01: Perform continuous conversions on Channel 1  
b10: Perform continuous conversions on Channel 2 (FDC2114, FDC2214 only)  
b11: Perform continuous conversions on Channel 3 (FDC2114, FDC2214 only)                                                                                                                                         |
| 13   | SLEEP_MODE_EN | R/W  | 1     | Sleep mode enable. Enter or exit low power sleep mode. b0: Device is active.  
b1: Device is in sleep mode.                                                                                                                                                                                                                                                                                   |
| 12   | RESERVED      | R/W  | 0     | Reserved. Set to b1.                                                                                                                                                                                                                                                                                                                                                     |
| 11   | SENSOR_ACTIVATE_SEL | R/W  | 1     | Sensor activation mode selection. Set the mode for sensor initialization. b0: Full current activation mode – the FDC will drive maximum sensor current for a shorter sensor activation time.  
b1: Low power activation mode – the FDC uses the value programmed in DRIVE_CURRENT_CHx during sensor activation to minimize power consumption.                                                                                                               |
| 10   | RESERVED      | R/W  | 0     | Reserved. Set to b1.                                                                                                                                                                                                                                                                                                                                                     |
| 9    | REF_CLK_SRC   | R/W  | 0     | Select Reference Frequency Source  
b0: Use Internal oscillator as reference frequency  
b1: Reference frequency is provided from CLKIN pin.                                                                                                                                                                                                                                                                    |
| 8    | RESERVED      | R/W  | 0     | Reserved. Set to b0.                                                                                                                                                                                                                                                                                                                                                     |
| 7    | INTB_DIS      | R/W  | 0     | INTB Disable  
b0: INTB pin is asserted when status register updates.  
b1: INTB pin is not asserted when status register updates                                                                                                                                                                                                                                                                                                             |
| 6    | HIGH_CURRENT_DRV | R/W  | 0     | High Current Sensor Drive  
b0: The FDC drives all channels with normal sensor current (1.5 mA maximum).  
b1: The FDC drives Channel 0 with current >1.5 mA. This mode is not supported if AUTOSCAN_EN = b1 (multi-channel mode)                                                                                                                                    |
| 5:0  | RESERVED      | R/W  | 00 0001 | Reserved Set to b00’0001
7.6.29 Address 0x1B, MUX_CONFIG

Figure 46. Address 0x1B, MUX_CONFIG

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>AUTOSCAN_EN</td>
<td>R/W</td>
<td>0</td>
<td>Auto-Scan mode enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b0: Continuous conversion on the single channel selected by CONFIG.ACTIVE_CHAN register field.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b1: Auto-Scan conversions as selected by MUX_CONFIG.RR_SEQUENCE register field.</td>
</tr>
<tr>
<td>14:13</td>
<td>RR_SEQUENCE</td>
<td>R/W</td>
<td>00</td>
<td>Auto-Scan sequence configuration</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Configure multiplexing channel sequence. The FDC performs a single conversion on each channel in the sequence selected, and then restart the sequence continuously.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b00: Ch0, Ch1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b01: Ch0, Ch1, Ch2 (FDC2114, FDC2214 only)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b10: Ch0, Ch1, Ch2, Ch3 (FDC2114, FDC2214 only)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>b11: Ch0, Ch1</td>
</tr>
</tbody>
</table>

7.6.30 Address 0x1C, RESET_DEV

Figure 47. Address 0x1C, RESET_DEV

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>RESET_DEV</td>
<td>R/W</td>
<td>0</td>
<td>Device Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Write b1 to reset the device. Will always readback 0.</td>
</tr>
<tr>
<td>14:11</td>
<td>RESERVED</td>
<td>R/W</td>
<td>0000</td>
<td>Reserved. Set to b0000</td>
</tr>
<tr>
<td>10:9</td>
<td>OUTPUT_GAIN</td>
<td>R/W</td>
<td>00</td>
<td>Output gain control (FDC2112, FDC2114 only)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00: Gain =1 (0 bits shift)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>01: Gain = 4 (2 bits shift)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10: Gain = 8 (3 bits shift)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11: Gain = 16 (4 bits shift)</td>
</tr>
<tr>
<td>8:0</td>
<td>RESERVED</td>
<td>R/W</td>
<td>0 0000 0000</td>
<td>Reserved, Set to b0 0000 0000</td>
</tr>
</tbody>
</table>
### 7.6.31 Address 0x1E, DRIVE_CURRENT_CH0

**Figure 48. Address 0x1E, DRIVE_CURRENT_CH0**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 15:11 | CH0_IDRIVE | R/W | 0000 0 | Channel 0 Sensor drive current  
This field defines the Drive Current used during the settling + conversion time of Channel 0 sensor clock. Set such that $1.2V \leq$ sensor oscillation amplitude (pk) $\leq 1.8V$  
00000: 0.016 mA  
00001: 0.018 mA  
00010: 0.021 mA  
00011: 0.025 mA  
00100: 0.028 mA  
00101: 0.033 mA  
00110: 0.038 mA  
00111: 0.044 mA  
01000: 0.052 mA  
01001: 0.060 mA  
01010: 0.069 mA  
01011: 0.081 mA  
01100: 0.093 mA  
01101: 0.108 mA  
01110: 0.126 mA  
01111: 0.146 mA  
10000: 0.169 mA  
10001: 0.196 mA  
10010: 0.228 mA  
10011: 0.254 mA  
10100: 0.307 mA  
10101: 0.356 mA  
10110: 0.413 mA  
10111: 0.479 mA  
11000: 0.555 mA  
11001: 0.644 mA  
11010: 0.747 mA  
11011: 0.887 mA  
11100: 1.006 mA  
11101: 1.167 mA  
11110: 1.354 mA  
11111: 1.571 mA |
| 10:0 | RESERVED | – | 000 0000 | Reserved |

Table 41. Address 0x1E, DRIVE_CURRENT_CH0 Field Descriptions
7.6.32 Address 0x1F, DRIVE_CURRENT_CH1

Figure 49. Address 0x1F, DRIVE_CURRENT_CH1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:11</td>
<td>CH1_IDRIVE</td>
<td>R/W</td>
<td>0000 0</td>
<td>Channel 1 Sensor drive current</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field defines the drive current used during</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the settling + conversion time of Channel 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>sensor clock. Set such that 1.2 V ≤ sensor</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>oscillation amplitude (pk) ≤ 1.8 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00000: 0.016 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00001: 0.018 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00010: 0.021 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>...</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11111: 1.571 mA</td>
</tr>
</tbody>
</table>

10:0  RESERVED – 000 0000 0000  Reserved

7.6.33 Address 0x20, DRIVE_CURRENT_CH2 (FDC2114 / FDC2214 only)

Figure 50. Address 0x20, DRIVE_CURRENT_CH2

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:11</td>
<td>CH2_IDRIVE</td>
<td>R/W</td>
<td>0000 0</td>
<td>Channel 2 Sensor drive current</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field defines the drive current to be used</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>during the settling + conversion time of Channel</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2 sensor clock. Set such that 1.2 V ≤ sensor</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>oscillation amplitude (pk) ≤ 1.8 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00000: 0.016 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00001: 0.018 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00010: 0.021 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>...</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11111: 1.571 mA</td>
</tr>
</tbody>
</table>

10:0  RESERVED – 000 0000 0000  Reserved
7.6.34  Address 0x21, DRIVE_CURRENT_CH3 (FDC2114 / FDC2214 only)

Figure 51. Address 0x21, DRIVE_CURRENT_CH3

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:11</td>
<td>CH3_IDRIVE</td>
<td>R/W</td>
<td>0000 0</td>
<td>Channel 3 Sensor drive current</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field defines the drive current to be used during the settling time</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>+ conversion time of Channel 3 sensor clock. Set such that 1.2V ≤</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>sensor oscillation amplitude (pk) ≤ 1.8 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00000: 0.016 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00001: 0.018 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00010: 0.021 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>...</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11111: 1.571 mA</td>
</tr>
<tr>
<td>10:0</td>
<td>RESERVED</td>
<td>–</td>
<td>0000 0</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0000 0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

7.6.35  Address 0x7E, MANUFACTURER_ID

Figure 52. Address 0x7E, MANUFACTURER_ID

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:0</td>
<td>MANUFACTURER_ID</td>
<td>R</td>
<td>0101 0100</td>
<td>Manufacturer ID = 0x5449</td>
</tr>
</tbody>
</table>

7.6.36  Address 0x7F, DEVICE_ID

Figure 53. Address 0x7F, DEVICE_ID

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>DEVICE_ID</td>
<td>R</td>
<td>0011 0000</td>
<td>Device ID</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0101 0100</td>
<td>0x3054 (FDC2112, FDC2114 only)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x3055 (FDC2212, FDC2214 only)</td>
</tr>
</tbody>
</table>
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Sensor Configuration

The FDC supports two sensor configurations. Both configurations use an LC tank to set the frequency of oscillation. A typical choice is an 18-μH shielded SMD inductor in parallel with a 33-pF capacitor, which result in a 6.5-MHz oscillation frequency. In the single-ended configuration in Figure 54, a conductive plate is connected IN0A. Together with a target object, the conductive plate forms a variable capacitor.

Figure 54. Single-ended Sensor Configuration

In the differential sensor configuration in Figure 55, one conductive plate is connected to IN0A, and a second conductive plate is connected to IN0B. Together, they form a variable capacitor. When using an single-ended sensor configuration, set CHx_FIN_SEL to b10 (divide by 2).

Figure 55. Differential Sensor Configuration

The single-ended configuration allows higher sensing range than the differential configuration for a given total sensor plate area. In applications in which high sensitivity at close proximity is desired, the differential configuration performs better than the single-ended configuration.
Application Information (continued)

8.1.2 Shield

In order to minimize interference from external objects, some applications require an additional plate which acts as a shield. The shield can either be:

- actively driven shield: The shield is a buffered signal of the INxA pin. The signal is buffered by an external amplifier with a gain of 1.
- passive shield: The shield is connected to GND. Adding a passive shield decreases sensitivity of the sensor, but is dependent on the distance between the distance between the sensing plate and the shield. The distance between the sensing plate and the shield should be adjusted to achieve the required sensitivity.

8.1.3 Power-Cycled Applications

For applications which do not require high sample rates or maximum conversion resolution, the total active conversion time of the FDC can be minimized to reduce power consumption. This can be done by either by using sleep mode or shutdown mode during times in which conversions are not required (see Device Functional Modes).

As an example, for an application which only needs 10 samples per second with a resolution of 16 bits can utilize the low-power modes. The sensor requires SETTLECOUNT = 16 and IDRIVE of 01111b (0.146 mA). Given FREF = 40 MHz and RCOUNT = 4096 will provide the resolution required. This corresponds to 4096 × 16 × 10 / 40 MHz → 16.4 ms of active conversion time per second. Start-up time and channel switch delay account for an additional 0.34 ms. For the remainder of the time, the device can be in sleep mode: Therefore, the average current is 19.4 ms * 3.6 mA active current + 980.6 ms of 35 µA of sleep current, which is approximately 104.6 µA of average supply current. Sleep mode retains register settings and therefore requires less I2C writes to wake up the FDC than shutdown mode.

Greater current savings can be realized by use of shutdown mode during inactive periods. In shutdown mode, device configuration is not retained, so the device must be configured for each sample. For this example, configuring each sample takes approximately 1.2 ms (13 registers × 92.5 µs per register). The total active time is 20.6 ms. The average current is 20 ms × 3.6 mA active current + 980 ms × 2 µA of shutdown current, which is approximately 75 µA of average supply current.

For further information on power-cycled applications, refer to Power Reduction Techniques for the FDC2214/2212/2114/2112 in Capacitive Sensing Applications.

8.1.4 Inductor Self-Resonant Frequency

Every inductor has a distributed parasitic capacitance, which is dependent on construction and geometry. At the self-resonant frequency (SRF), the reactance of the inductor cancels the reactance of the parasitic capacitance. Above the SRF, the inductor will electrically appear to be a capacitor. Because the parasitic capacitance is not well-controlled or stable, TI recommends: \( f_{\text{SENSOR}} < 0.8 \times f_{\text{SR}} \).

![Figure 56. Example Coil Inductance vs Frequency](image)

The example inductor in Figure 56, has a SRF at 6.38 MHz; therefore, the inductor must not be operated above 0.8 × 6.38 MHz, or 5.1 MHz.
Application Information (continued)

8.1.5 Application Curves for Proximity Sensing

Common test conditions (unless specified otherwise): Sensor capacitor: 1 layer, 20.9 × 13.9 mm, Bourns CMH322522-180KL sensor inductor with L=18 µH and 33 pF 1% COG/NP0 Target: Grounded aluminum plate (176 × 123 mm), Channel = Channel 0 (continuous mode) CKIN = 40 MHz, CHx_FIN_SEL = b10, CHx_FREF_DIVIDER = b00 0000 0001 CH0_RCOUNT = 0xFFFF, SETTLECOUNT_CH0 = 0x0100, DRIVE_CURRENT_CH0 = 0x7800

8.2 Typical Application

The FDC can be used to measure liquid level in non-conductive containers. Due to its very high excitation rate capability, it is able to measure soapy water, ink, soap, and other conductive liquids. Capacitive sensors can be attached to the outside of the container or be located remotely from the container, allowing for contactless measurements.

The working principle is based on a ratiometric measurement; Figure 60 shows a possible system implementation which uses three electrodes. The level electrode provides a capacitance value proportional to the liquid level. The reference environmental electrode and the reference liquid electrode are used as references. The reference liquid electrode accounts for the liquid dielectric constant and its variation, while the reference environmental electrode is used to compensate for any other environmental variations that are not due to the liquid itself. Note that the reference environmental electrode and the reference liquid electrode are the same physical size (hREF).

For this application, single-ended measurements on the active channels are appropriate, as the tank is grounded. Use to determine the liquid level from the measured capacitances:
Typical Application (continued)

\[ \text{Level} = h_{\text{ref}} \frac{C_{\text{Lev}} - C_{\text{Lev}}(0)}{C_{\text{RL}} - C_{\text{RE}}} \]

where

- \( C_{\text{RE}} \) is the capacitance of the reference environmental electrode,
- \( C_{\text{RL}} \) is the capacitance of the reference liquid electrode,
- \( C_{\text{Lev}} \) is the current value of the capacitance measured at the level electrode sensor,
- \( C_{\text{Lev}}(0) \) is the capacitance of the Level electrode when the container is empty, and
- \( h_{\text{REF}} \) is the height in the desired units of the container or liquid reference electrodes.

The ratio between the capacitance of the level and the reference electrodes allows simple calculation of the liquid level inside the container itself. Very high sensitivity values (that is, many LSB/mm) can be obtained due to the high resolution of the FDC2x1x, even when the sensors are located remotely from the container. Note that this approach assumes that the container has a uniform cross section from top to bottom, so that each incremental increase or decrease in the liquid represents a change in volume that is directly related to the height of the liquid.

\[ \text{Figure 60. FDC (Liquid Level Measurement)} \]

8.2.1 Design Requirements

The liquid level measurement should be independent of the liquid, which can be achieved using the 3-electrode design described above. Moreover, the sensor should be isolated from environmental interferers such as a human body, other objects, or EMI.

8.2.2 Detailed Design Procedure

In capacitive sensing systems, the design of the sensor plays an important role in determining system performance and capabilities. In most cases the sensor is simply a metal plate that can be designed on the PCB.
Typical Application (continued)

The sensor used in this example is implemented with a two-layer PCB. On the top layer, which faces the tank, there are the 3 electrodes (reference environmental, reference liquid, and level) with a ground plane surrounding the electrodes.

Depending on the shape of the container, the FDC can be located on the sensor PCB to minimize the length of the traces between the input channels and the sensors. In case the shape of the container or other mechanical constraints do not allow having the sensors and the FDC on the same PCB, the traces which connect the channels to the sensor need to be shielded with the appropriate shield.

8.2.3 Application Performance Plot

A liquid level sensor with 3 electrodes like the one shown in the schematic was connected to the EVM. The plot shows the capacitance measured by Level sensor at different levels of liquid in the tank. The capacitance of the Reference Liquid and Reference Environmental sensors have a steady value because they experience consistent exposure to liquid and air, while the capacitance of the level sensor (Level) increases linearly with the height of the liquid in the tank.

Figure 61. Electrodes’ Capacitance vs Liquid Level

8.2.4 Recommended Initial Register Configuration Values

The application requires 100SPS ($T_{SAMPLE} = 10$ ms). A sensor with an 18-µH inductor and a 33-pF capacitor is used. Additional pin, trace, and wire capacitance accounts for 20 pF, so the total capacitance is 53-pF.

Using $L$ and $C$, $f_{SENSOR} = 1/2\pi\sqrt{(LC)} = 1/2\pi\sqrt{(18 \times 10^{-6} \times 50 \times 10^{-12})} = 5.15$ MHz. This represents the maximum sensor frequency. When the sensor capacitance is added, the frequency will decrease.

Using a system master clock of 40 MHz applied to the CLkin pin allows flexibility for setting the internal clock frequencies. The sensor coils are connected to channel 0 (IN0A and IN0B pins), channel 1 (IN1A and IN1B pins), and channel 2 (IN2A and IN2B pins).

After powering on the FDC, it will be in Sleep Mode. Program the registers as follows (example sets registers for channel 0 only; channel 1 and channel 2 registers can use equivalent configuration):

1. Set the dividers for channel 0.
   (a) Because the sensor is in an single-ended configuration, the sensor frequency select register should be set to 2, which means setting field CH0_FIN_SELto b10.
   (b) The design constraint for $f_{REF0}$ is $> 4 \times f_{SENSOR}$. To satisfy this constraint, $f_{REF0}$ must be greater than 20.6 MHz, so the reference divider should be set to 1. This is done by setting the CH0_FREF_DIVIDER field to 0x01.
   (c) The combined value for Chan. 0 divider register (0x14) is 0x2001.

2. Sensor drive current: to ensure that the oscillation amplitude is between 1.2V and 1.8V, measure the oscillation amplitude on an oscilloscope and adjust the IDRIVE value, or use the integrated FDC GUI feature to determine the optimal setting. In this case the IDRIVE value should be set to 15 (decimal), which results in an oscillation amplitude of 1.68 V(pk). The INIT_DRIVE current field should be set to 0x00. The combined value for the DRIVE_CURRENT_CH0 register (addr 0xE) is 0x7C00.
Typical Application (continued)

3. Program the settling time for Channel 0 (see Multi-Channel and Single-Channel Operation).
   (a) \( \text{CHx_SETTLECOUNT} > V_{\text{pk}} \times f_{\text{REF}} \times C \times \pi^2 / (32 \times \text{IDRIVE}_x) \rightarrow 7.5 \), rounded up to 8. To provide margin to account for system tolerances, a higher value of 10 is chosen.
   (b) Register 0x10 should be programmed to a minimum of 10.
   (c) The settle time is: \((10 \times 16)/40,000,000 = 4 \mu s\)
   (d) The value for Channel 0 SETTLECOUNT register (0x10) is 0x000A.

4. The channel switching delay is approximately 1 \( \mu \)s for \( f_{\text{REF}} = 40 \) MHz (see Multi-Channel and Single-Channel Operation)

5. Set the conversion time by programming the reference count for Channel 0. The budget for the conversion time is: \(1/N \times (T_{\text{SAMPLE}} - \text{settling time} - \text{channel switching delay}) = 1/3 \times (10,000 - 4 - 1) = 3.33 \text{ ms}\)
   (a) To determine the conversion time register value, use the following equation and solve for \( \text{CH0_RCOUNT} \); Conversion Time \((t_{\text{CD0}}) = (\text{CH0_RCOUNT} \times 16)/f_{\text{REF0}}\).
   (b) This results in \( \text{CH0_RCOUNT} \) having a value of 8329 decimal (rounded down). Note that this yields an ENOB > 13 bits.
   (c) Set the \( \text{CH0_RCOUNT} \) register (0x08) to 0x2089.

6. Use the default values for the \( \text{ERROR_CONFIG} \) register (address 0x19). By default, no interrupts are enabled

7. Program the \( \text{MUX_CONFIG} \) register
   (a) Set the \( \text{AUTOSCAN_EN} \) to b1 bit to enable sequential mode
   (b) Set \( \text{RR_SEQUENCE} \) to b10 to enable data conversion on three channels (channel 0, channel 1, channel 2)
   (c) Set \( \text{DEGLITCH} \) to b101 to set the input deglitch filter bandwidth to 10 MHz, the lowest setting that exceeds the oscillation tank frequency.
   (d) The combined value for the \( \text{MUX_CONFIG} \) register (address 0x1B) is 0xC20D

8. Finally, program the \( \text{CONFIG} \) register as follows:
   (a) Set the \( \text{ACTIVE_CHAN} \) field to b00 to select channel 0.
   (b) Set \( \text{SLEEP_MODE_EN} \) field to b0 to enable conversion.
   (c) Set \( \text{SENSOR_ACTIVATE_SEL} = \text{b0} \), for full current drive during sensor activation
   (d) Set the \( \text{REF_CLK_SRC} \) field to b1 to use the external clock source.
   (e) Set the other fields to their default values.
   (f) The combined value for the \( \text{CONFIG} \) register (address 0x1A) is 0x1601.

We then read the conversion results for channel 0 to channel 2 every 10ms from register addresses 0x00 to 0x05.

Based on the example configuration above, TI recommends the following register write sequence is recommended:

### Table 47. Recommended Initial Register Configuration Values (Multi-channel Operation)

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>VALUE</th>
<th>REGISTER NAME</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x08</td>
<td>0x8329</td>
<td>RCOUNT_CH0</td>
<td>Reference count calculated from timing requirements (100 SPS) and resolution requirements</td>
</tr>
<tr>
<td>0x09</td>
<td>0x8329</td>
<td>RCOUNT_CH1</td>
<td>Reference count calculated from timing requirements (100 SPS) and resolution requirements</td>
</tr>
<tr>
<td>0x0A</td>
<td>0x8329</td>
<td>RCOUNT_CH2</td>
<td>Reference count calculated from timing requirements (100 SPS) and resolution requirements</td>
</tr>
<tr>
<td>0x10</td>
<td>0x000A</td>
<td>SETTLECOUNT_CH0</td>
<td>Minimum settling time for chosen sensor</td>
</tr>
<tr>
<td>0x11</td>
<td>0x000A</td>
<td>SETTLECOUNT_CH1</td>
<td>Minimum settling time for chosen sensor</td>
</tr>
<tr>
<td>0x12</td>
<td>0x000A</td>
<td>SETTLECOUNT_CH2</td>
<td>Minimum settling time for chosen sensor</td>
</tr>
<tr>
<td>0x14</td>
<td>0x2002</td>
<td>CLOCK_DIVIDER_CH0</td>
<td>CH0_FIN_DIVIDER = 1, CH0_FREF_DIVIDER = 2</td>
</tr>
<tr>
<td>0x15</td>
<td>0x2002</td>
<td>CLOCK_DIVIDER_CH1</td>
<td>CH1_FIN_DIVIDER = 1, CH1_FREF_DIVIDER = 2</td>
</tr>
<tr>
<td>0x16</td>
<td>0x2002</td>
<td>CLOCK_DIVIDER_CH2</td>
<td>CH1_FIN_DIVIDER = 1, CH1_FREF_DIVIDER = 2</td>
</tr>
<tr>
<td>0x19</td>
<td>0x0000</td>
<td>ERROR_CONFIG</td>
<td>Can be changed from default to report status and error conditions</td>
</tr>
</tbody>
</table>
Typical Application (continued)

Table 47. Recommended Initial Register Configuration Values (Multi-channel Operation) (continued)

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>VALUE</th>
<th>REGISTER NAME</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x1B</td>
<td>0xC20D</td>
<td>MUX_CONFIG</td>
<td>Enable Ch 0, Ch 1, and Ch 2 (sequential mode), set Input deglitch bandwidth to 10MHz</td>
</tr>
<tr>
<td>0x1E</td>
<td>0x7C00</td>
<td>DRIVE_CURRENT_CH0</td>
<td>Sets sensor drive current on ch 0</td>
</tr>
<tr>
<td>0x1F</td>
<td>0x7C00</td>
<td>DRIVE_CURRENT_CH1</td>
<td>Sets sensor drive current on ch 1</td>
</tr>
<tr>
<td>0x20</td>
<td>0x7C00</td>
<td>DRIVE_CURRENT_CH2</td>
<td>Sets sensor drive current on ch 2</td>
</tr>
<tr>
<td>0x1A</td>
<td>0x1601</td>
<td>CONFIG</td>
<td>Enable full current drive during sensor activation, select external clock source, wake up device to start conversion. This register write must occur last because device configuration is not permitted while the FDC is in active mode.</td>
</tr>
</tbody>
</table>

8.3 Do's and Don'ts
- Do leave a small gap between sensor plates in differential configurations. 2-3mm minimum separation is recommended.
- The FDC does not support hot-swapping of the sensors. Do not hot-swap sensors, for example by using external multiplexers.

9 Power Supply Recommendations

The FDC requires a voltage supply within 2.7 V and 3.6 V. TI recommends multilayer ceramic bypass X7R capacitors of 0.1 μF and 1 μF between the VDD and GND pins. If the supply is located more than a few inches from the FDC, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 10 μF is a typical choice.

The optimum placement is closest to the VDD and GND pins of the device. Care should be taken to minimize the loop area formed by the bypass capacitor connection, the VDD pin, and the GND pin of the device. See Figure 62 and Figure 65 for layout examples.

10 Layout

10.1 Layout Guidelines
- Avoid long traces to connect the sensor to the FDC. Short traces reduce parasitic capacitances between sensor inductor and offer higher system performance.
- Systems that require matched channel response need to have matched trace length on all active channels.

10.2 Layout Examples
Figure 62 to Figure 65 show the FDC2114 / FDC2214 evaluation module (EVM) layout.
Figure 62. Example PCB Layout: Top Layer (Signal)
Figure 63. Example PCB Layout: Mid-Layer 1 (GND)
Layout Examples (continued)

Figure 64. Example PCB Layout: Mid-layer 2 (Power)
Figure 65. Example PCB Layout: Bottom Layer (Signal)
11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support
For related links, see the following:
Texas Instruments' WEBENCH® tool: http://www.ti.com/webench

11.2 Documentation Support

11.2.1 Related Documentation
For related documentation, refer to the following:
For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report (SPRA953)

11.3 Community Resources
The following links connect to TI community resources. Linked contents are provided “AS IS” by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community Ti’s Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support Ti’s Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Related Links
The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

### Table 48. Related Links

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<th>PARTS</th>
<th>PRODUCT FOLDER</th>
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<th>TECHNICAL DOCUMENTS</th>
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</table>

11.5 Trademarks
E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

⚠️ These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## Packaging Information

<table>
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<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
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(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- ** OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
- **TBD:** The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF FDC2112-Q1, FDC2114-Q1, FDC2212-Q1, FDC2214-Q1:

- Catalog: FDC2112, FDC2114, FDC2212, FDC2214

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
### TAPE AND REEL INFORMATION

#### REEL DIMENSIONS

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<th>Package Type</th>
<th>Package Drawing</th>
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<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
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*All dimensions are nominal.*

<table>
<thead>
<tr>
<th>A0</th>
<th>Dimension designed to accommodate the component width</th>
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<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
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<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
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<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
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<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
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*www.ti.com 20-Sep-2016*
<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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<td>35.0</td>
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</tbody>
</table>

*All dimensions are nominal*
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
NOTES:
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is designed to be soldered to a thermal pad on the board for thermal and mechanical performance. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).
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