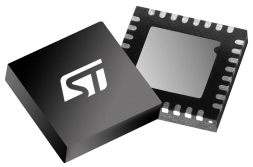
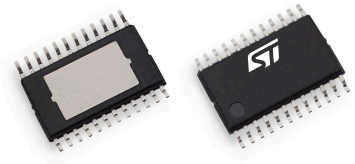
L9026

Data brief

Automotive configurable multi-channel relay driver 2HS + 6HS/LS



VFQFPN32 exposed pad down
(5x5x1 mm)



HTSSOP24 exposed pad down
(7.8x6.4x1 mm)

Product status link
L9026

Product summary	
Order code	**L9026-B03N-TR**
Package	VFQFPN32
Packing	Tape & Reel
Order code	**L9026-YO-TR**
Package	HTSSOP24
Packing	Tape & Reel

Features

- AEC-Q100 qualified
- Six Configurable LS/HS drivers
- Two High Side drivers
- 2 parallel input pins with Input Mapping functionality
- Cranking capability down to VBATT = 3 V
- Digital supply voltage compatible with 3.3 V and 5 V microcontroller
- Reverse battery protection on VBATT and on drain pins without external components
- LED mode
- Bulb Inrush Mode (BIM) to drive lamps and electronic loads
- 2 Internal PWM Generator for microcontroller offload
- Very low quiescent current (with usage of IDLE pin)
- Limp Home mode (with usage of IDLE and IN pins)
- Green Product (RoHS compliant)
- Safety features
  - Temperature Sensor and Monitoring
  - Serial communications using address feedback, 1 parity bit, frame counter & short frame detection
- 16-bit serial peripheral interface for control and diagnosis
- Daisy Chain capability SPI, also compatible with 8-bit SPI devices
- Package options: HTSSOP24, VFQFPN32
- Full ISO26262 compliant, ASIL-B systems ready

Description

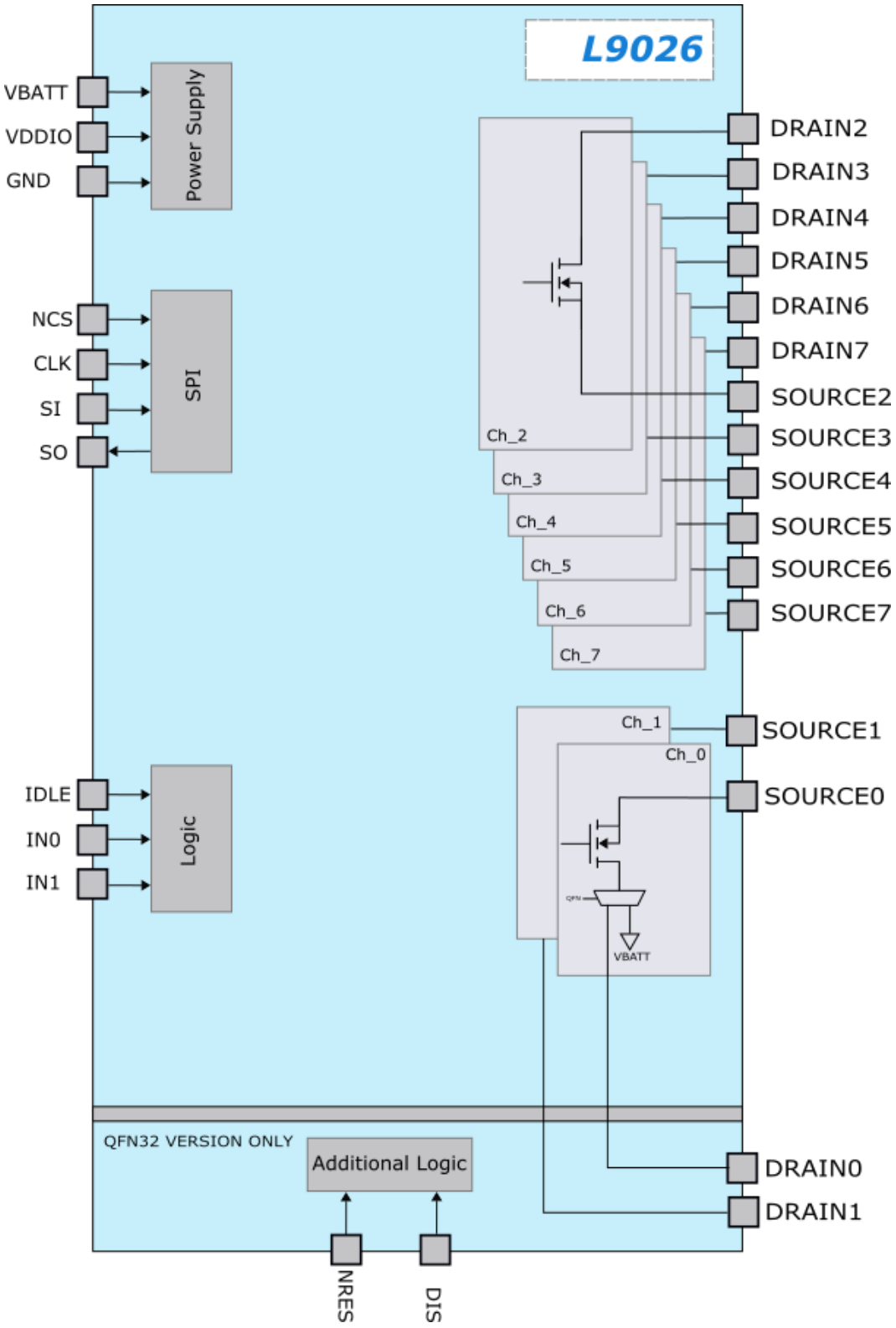
The L9026 is an eight-channel IC, with 2 fixed HS drivers and 6 configurable HS/LS drivers designed for Automotive applications (LEDs and Relays) and compatible with resistive, inductive and capacitive loads. The device offers advanced diagnostic and protection functionalities such as: short to GND, open load, overcurrent, over-temperature detections. The 8 output channels can be either driven by SPI or by 2 dedicated parallel inputs. Limp home functionality is also featured, which allows using 2 selected drivers in particularly faulty conditions, such as SPI fault, micro fault or supply UV. Daisy chain compatible even with 8bit SPI is available. The device is able to guarantee operations under cranking scenario down to VBATT = 3 V and guarantees very low quiescent current under RESET condition.

A serial peripheral interface (SPI) is used for control and configuration of the loads as well as of the device; besides, status feedback of all diagnostic functions is provided. For direct control and PWM there are two input pins available: these are connected to two defined outputs by default, but additional or different output mapping can be controlled by SPI.

As reported above, the device is available in two package versions: HTSSOP24 and VFQFPN32. Only for the QFN package 2 additional pins are available for safety reasons. In details, the NRES pin is used to reset internal registers to their default values and the DIS pin is used to disable all channels.

1 Block diagram

Figure 1. **Block diagram**



2 Application circuit

Here below two general application circuits:

- Figure 2 reports L9026 with the HTSSOP24 version package
- Figure 3 shows the application of L9026 with the VFQFPN32 version package

In the list of external components, the different parts are marked following the items reported below:

1. mandatory components for L9026 functionality
2. recommended components for EMC robustness
3. recommended components for ESD trials
4. recommended System component

Note: recommended components may depend on the requirements at system levels and shall be confirmed by specific tests on the final application.

Figure 2. HTSSOP24 Application schematic

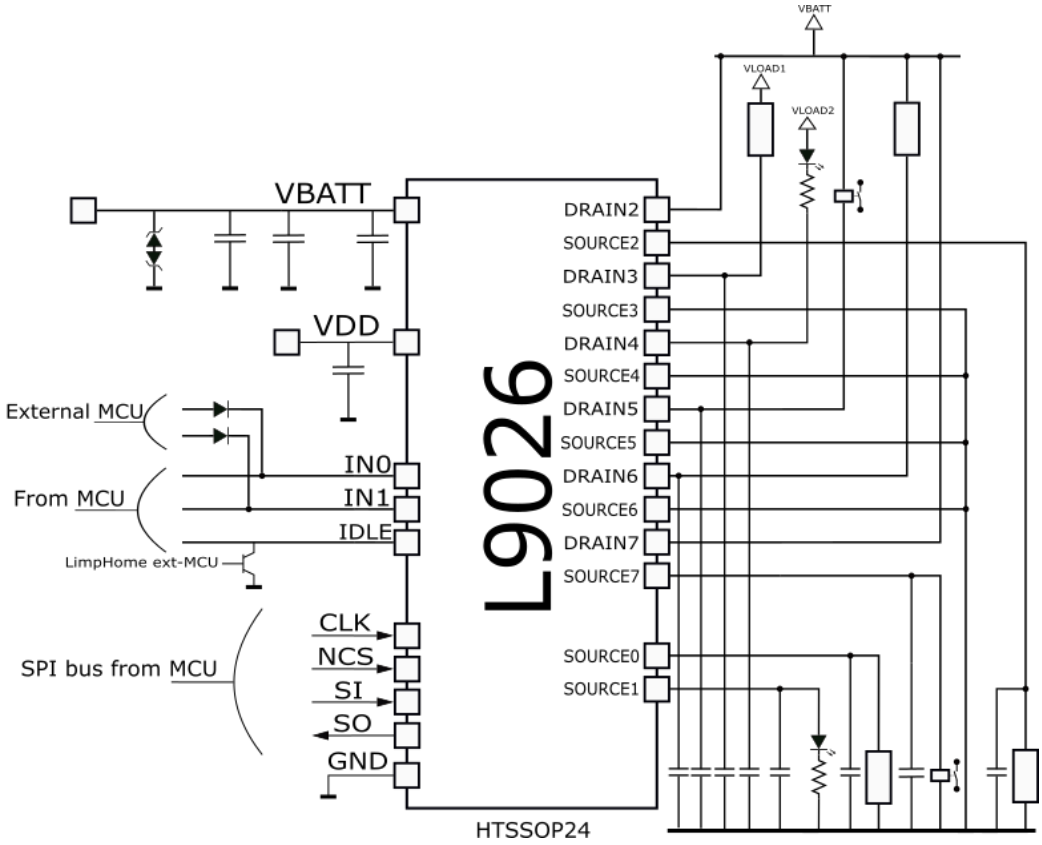


Figure 3. **VFQFPN32 Application schematic**

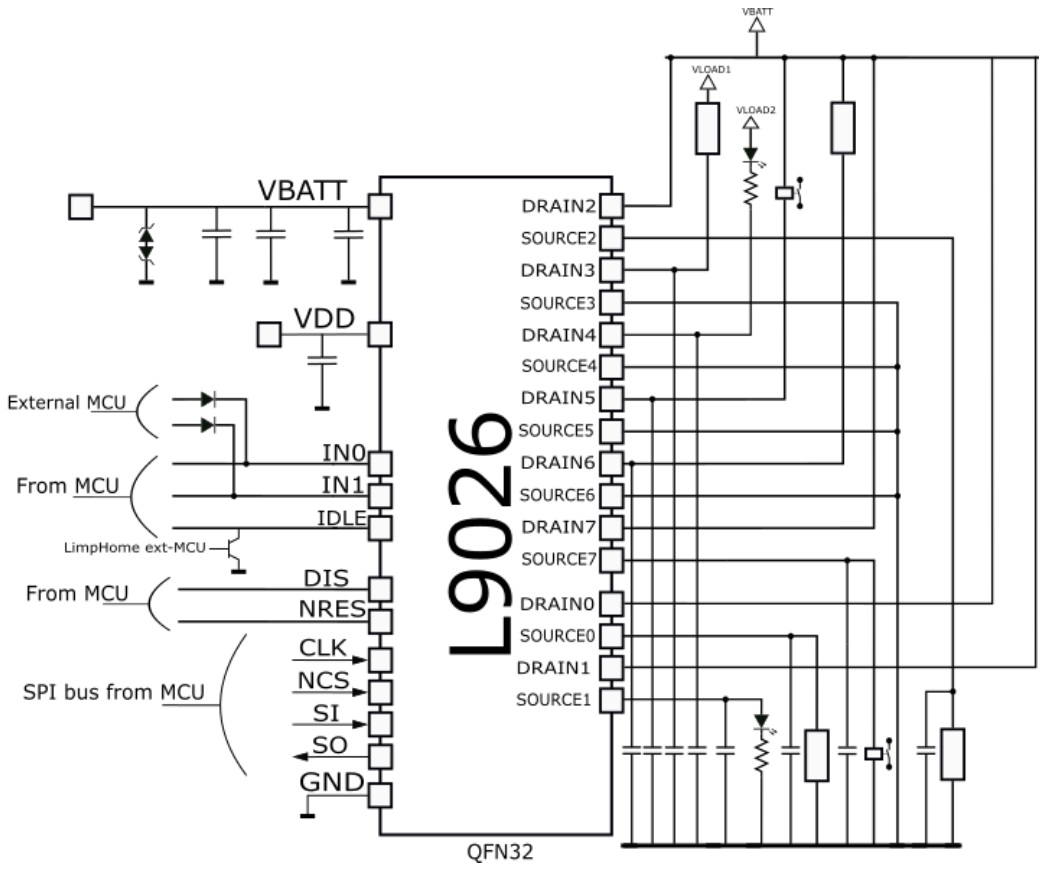
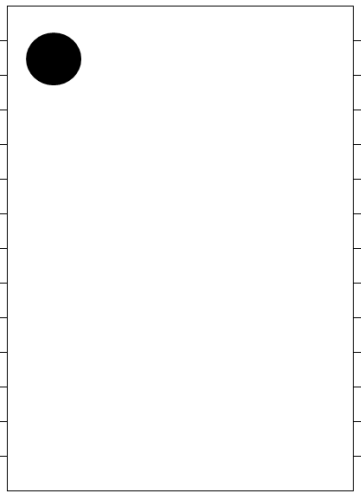


Table 1. **External components list for L9026 application circuit**

Pin	External components					Requirement	Comment
	Type	Min	Typ	Max	Unit		
VBATT	Capacitor	-	120	-	nF	(2), (3)	Tolerance ±20% 50 V
	Capacitor	-	100	-	µF	(2)	50 V, Transient and load dump protection
	TVS	- 15	-	38	V	(4)	Transient voltage suppressor
	Capacitor	-	10	-	µF	(2), (3)	Tolerance ±20% 50 V, Transient and load dump protection
VDDIO	Capacitor	-	100	-	nF	(2)	Tolerance ±10% 50 V
DRAIN2 DRAIN7	Capacitor	-	-	12	nF	(3)	Maximum total capacitance value at output load (channel configured as low side)
DRAIN0 DRAIN7		47	-	-		(4)	Minimum capacitance value at load supply (channel configured as high side, DRAIN0 and DRAIN1 if available)
SOURCE0 SOURCE7	Capacitor	-	-	12	nF	(3)	Maximum total capacitance value as output load (channel configured as high side)

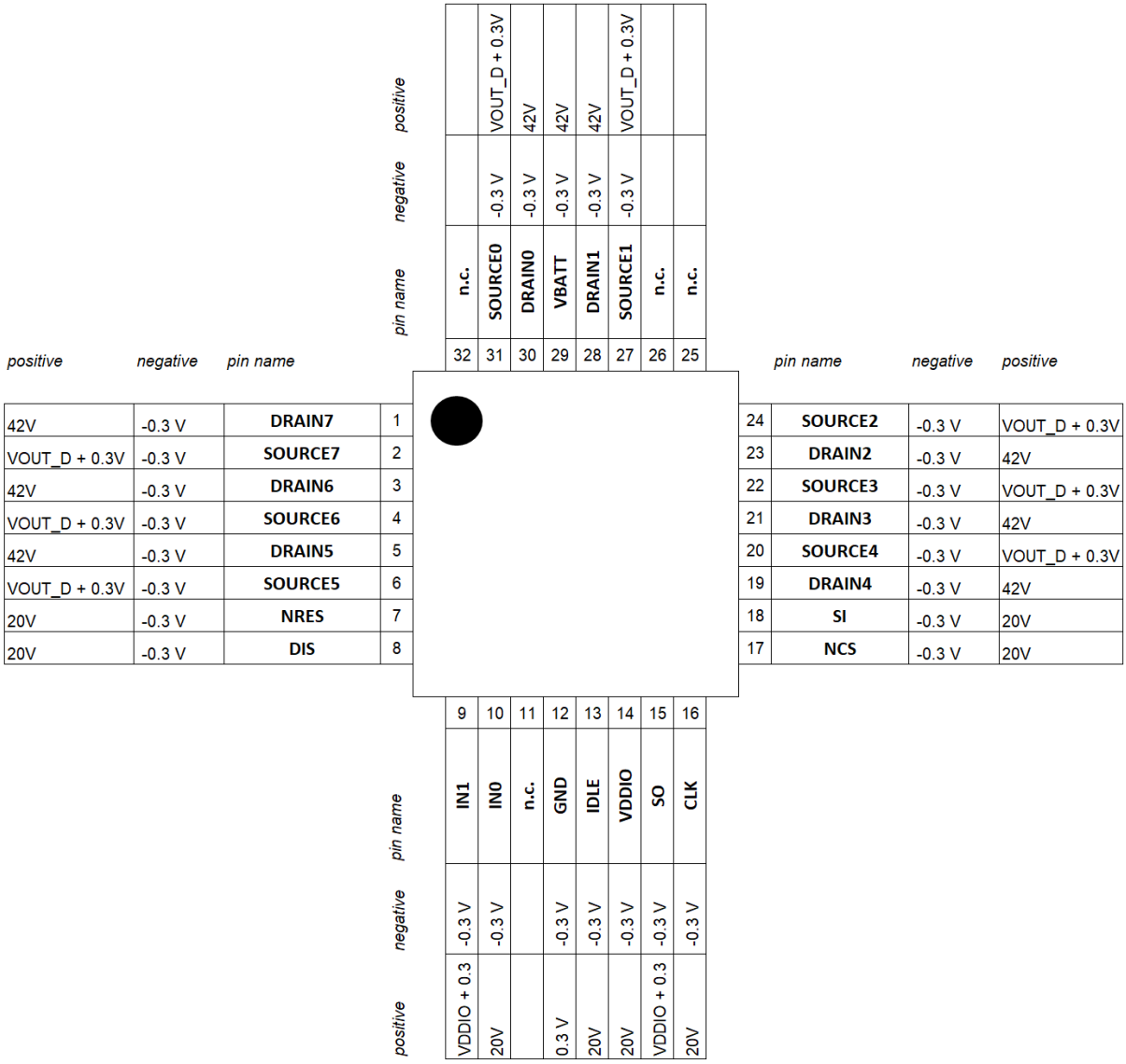
3 Pins description

Figure 4. HTSSOP-24 pinout diagram



positive	negative	pin name		pin name	negative	positive
42V	-0.3 V	VBATT	1	24 SOURCE1	-0.3 V	VOUT_D + 0.3V
VOUT_D + 0.3V	-0.3 V	SOURCE0	2	23 SOURCE2	-0.3 V	VOUT_D + 0.3V
42V	-0.3 V	DRAIN7	3	22 DRAIN2	-0.3 V	42V
VOUT_D + 0.3V	-0.3 V	SOURCE7	4	21 SOURCE3	-0.3 V	VOUT_D + 0.3V
42V	-0.3 V	DRAIN6	5	20 DRAIN3	-0.3 V	42V
VOUT_D + 0.3V	-0.3 V	SOURCE6	6	19 SOURCE4	-0.3 V	VOUT_D + 0.3V
42V	-0.3 V	DRAIN5	7	18 DRAIN4	-0.3 V	42V
VOUT_D + 0.3V	-0.3 V	SOURCE5	8	17 SI	-0.3 V	20V
VDDIO + 0.3	-0.3 V	IN1	9	16 NCS	-0.3 V	20V
20V	-0.3 V	IN0	10	15 CLK	-0.3 V	20V
0.3 V	-0.3 V	GND	11	14 SO	-0.3 V	VDDIO + 0.3
20V	-0.3 V	IDLE	12	13 VDDIO	-0.3 V	20V

Figure 5. **VFQFPN32 pinout diagram**



positive	negative	pin name		pin name	negative	positive
42V	-0.3 V	**DRAIN7**	1	24	**SOURCE2**	-0.3 V	VOUT_D + 0.3V
VOUT_D + 0.3V	-0.3 V	**SOURCE7**	2	23	**DRAIN2**	-0.3 V	42V
42V	-0.3 V	**DRAIN6**	3	22	**SOURCE3**	-0.3 V	VOUT_D + 0.3V
VOUT_D + 0.3V	-0.3 V	**SOURCE6**	4	21	**DRAIN3**	-0.3 V	42V
42V	-0.3 V	**DRAIN5**	5	20	**SOURCE4**	-0.3 V	VOUT_D + 0.3V
VOUT_D + 0.3V	-0.3 V	**SOURCE5**	6	19	**DRAIN4**	-0.3 V	42V
20V	-0.3 V	**NRES**	7	18	**SI**	-0.3 V	20V
20V	-0.3 V	**DIS**	8	17	**NCS**	-0.3 V	20V

32	31	30	29	28	27	26	25	
n.c.	**SOURCE0**	**DRAIN0**	**VBATT**	**DRAIN1**	**SOURCE1**	**n.c.**	**n.c.**	*pin name*
	-0.3 V	-0.3 V	-0.3 V	-0.3 V	-0.3 V			*negative*
	VOUT_D + 0.3V	42V	42V	42V	VOUT_D + 0.3V			*positive*

9	10	11	12	13	14	15	16	
IN1	**IN0**	**n.c.**	**GND**	**IDLE**	**VDDIO**	**SO**	**CLK**	*pin name*
-0.3 V	-0.3 V		-0.3 V	-0.3 V	-0.3 V	-0.3 V	-0.3 V	*negative*
VDDIO + 0.3	20V		0.3 V	20V	20V	VDDIO + 0.3	20V	*positive*

Table 2. **HTSSOP-24 pins list**

Pin number	Symbol	Function
1	VBATT	Battery voltage
2	SOURCE0	HS Source 0
3	DRAIN7	LS/HS Drain 7
4	SOURCE7	LS/HS Source 7
5	DRAIN6	LS/HS Drain 6
6	SOURCE6	LS/HS Source 6
7	DRAIN5	LS/HS Drain 5
8	SOURCE5	LS/HS Source 5
9	IN1	Parallel command input 1
10	IN0	Parallel command input 0
11	GND	Ground pin
12	IDLE	Idle function
13	VDDIO	IO supply
14	SO	SPI output stream
15	CLK	SPI clock
16	NCS	SPI Chip Select
17	SI	SPI input stream
18	DRAIN4	LS/HS Drain 4
19	SOURCE4	LS/HS Source 4
20	DRAIN3	LS/HS Drain 3
21	SOURCE3	LS/HS Source 3
22	DRAIN2	LS/HS Drain 2
23	SOURCE2	LS/HS Source 2
24	SOURCE1	HS Source 1

Table 3. **VFQFPN32 pins list**

Pin number QFN32	Symbol	Function
1	DRAIN7	LS/HS Drain 7
2	SOURCE7	LS/HS Source 7
3	DRAIN6	LS/HS Drain 6
4	SOURCE6	LS/HS Source 6
5	DRAIN5	LS/HS Drain 5
6	SOURCE5	LS/HS Source 5
7	NRES	NRES function – available only in VFQFPN32 package
8	DIS	Channel disable – available only in VFQFPN32 package
9	IN1	Parallel command input 1
10	IN0	Parallel command input 0
11	N.C.	-
12	GND	Ground pin
13	IDLE	Idle function
14	VDDIO	IO supply
15	SO	SPI output stream
16	CLK	SPI clock
17	NCS	SPI Chip Select
18	SI	SPI input stream
19	DRAIN4	LS/HS Drain 4
20	SOURCE4	LS/HS Source 4
21	DRAIN3	LS/HS Drain 3
22	SOURCE3	LS/HS Source 3
23	DRAIN2	LS/HS Drain 2
24	SOURCE2	LS/HS Source 2
25	N.C.	-
26	N.C.	-
27	SOURCE1	HS Source 1
28	DRAIN1	HS Drain 1
29	VBATT	Battery voltage
30	DRAIN0	HS Drain 0
31	SOURCE0	HS Source 0
32	N.C.	-

Note:

- *In case of VFQFPN32 package, CFG_0.DIS_EN and bit CFG_0.NRES_N needs to be set through SPI.*
- *In case of HTSSOP24 package, NRES and DIS pins are not available; CFG_0.DIS_EN and bit CFG_0.NRES_N must be considered as reserved, kept at '0'.*
- *For both package options the exposed pad must be left floating to guarantee the reverse battery protection feature.*

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 VFQFPN32 (5x5x1 mm exp. pad down 3.5x3.5) package information

Figure 6. VFQFPN32 (5x5x1 mm exp. pad down 3.5x3.5) package outline

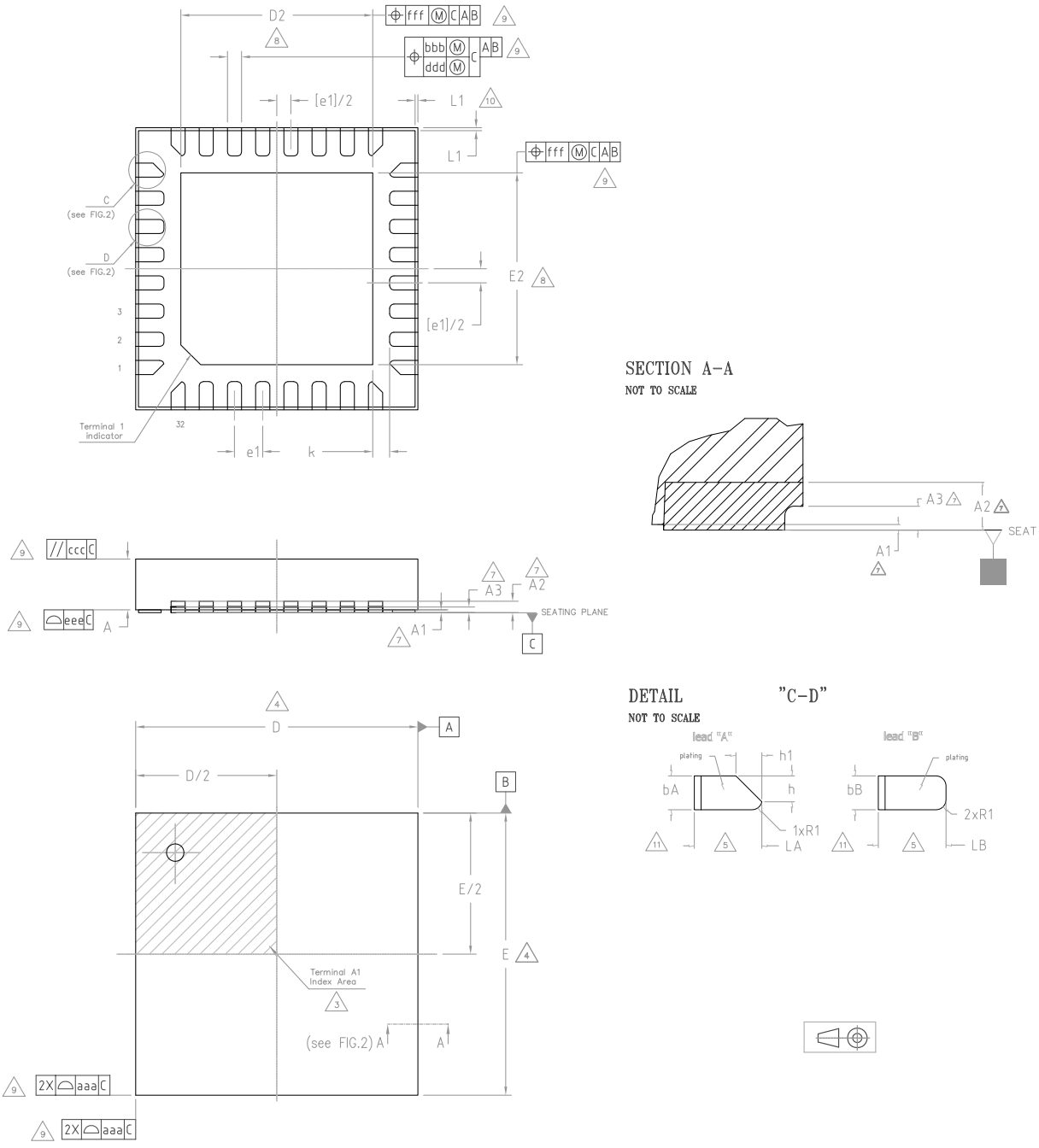


Table 4. VFQFPN32 (5x5x1 mm exp. pad down 3.5x3.5) mechanical data

Symbol	Dimensions			Note
	Min	Typ	Max	
A	0.80	0.90	1.00	
A1	0.00	-	0.05	
A2		0.2 REF		
A3	0.1	-	-	
D		5.00 BSC		4
D2	3.40	3.50	3.60	8
E		5.00 BSC		4
E2	3.40	3.50	3.60	8
e1		0.5 BSC		
k	0.20	-	-	
L1	-	-	0.05	10
La	0.40	0.50	0.60	11
bA	0.20	0.25	0.30	11
h		0.19 REF		11
h1		0.19 REF		11
LB	0.45	0.50	0.55	11
bB	0.20	0.25	0.30	11
N		32		6
R1	-	-	0.1	
Tolerance of form and position				
aaa		0.15		1, 2
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
fff		0.10		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. All Dimensions are in millimeters.
3. Terminal A1 identifier and terminal numbering convention shall conform to JEP95 SPP-002. Terminal A1 identifier must be located within the zone indicated on the outline drawing. Topside terminal A1 indicator may be a molded, or metalized feature. Optional indicator on bottom surface may be a molded, marked or metallized feature.
4. Outlines with “D” and “E” increments less than 0.5 mm should be registered as “stand alone” outlines. These outlines should use as many of the algorithms and dimensions states in the design standard as possible to insure predictability in manufacturing.
5. Inner edge of corner terminals may be chamfered or rounded in order to achieve minimum gap “k”. This feature should not affect the terminal width “b”, which is measured L/2 from the edge of the package body.
6. “N” is the maximum number of terminal positions for the specified body size. Depopulation is allowed, but only under the following conditions.
   – Depopulation scheme must be consistent in each quadrant of the package.
   – Non-symmetric variations should be broken out as separate mechanical outline variations, including depopulation graphics.
7. A1 is defined as the distance from the seating plane to the lowest point on the package body (standoff).
8. Dimension D2 and E2 refer to exposed pad.
9. For Tolerance of Form and Position see Table 4.
10. Critical dimensions: 10.1 L1
11. Dimensions “b” and “L” are measured at terminal plating surface.
12. For Symbols, Recommended Values and Tolerances see Table below: (ACCORDING TO PACKAGE OR JEDEC SPEC IF REGISTERED)

4.2 HTSSOP24 (7.8x6.4x1 mm exp. pad down 5.0x3.2) package information

Figure 7. **HTSSOP24 (7.8x6.4x1 mm exp. pad down 5.0x3.2) package outline**

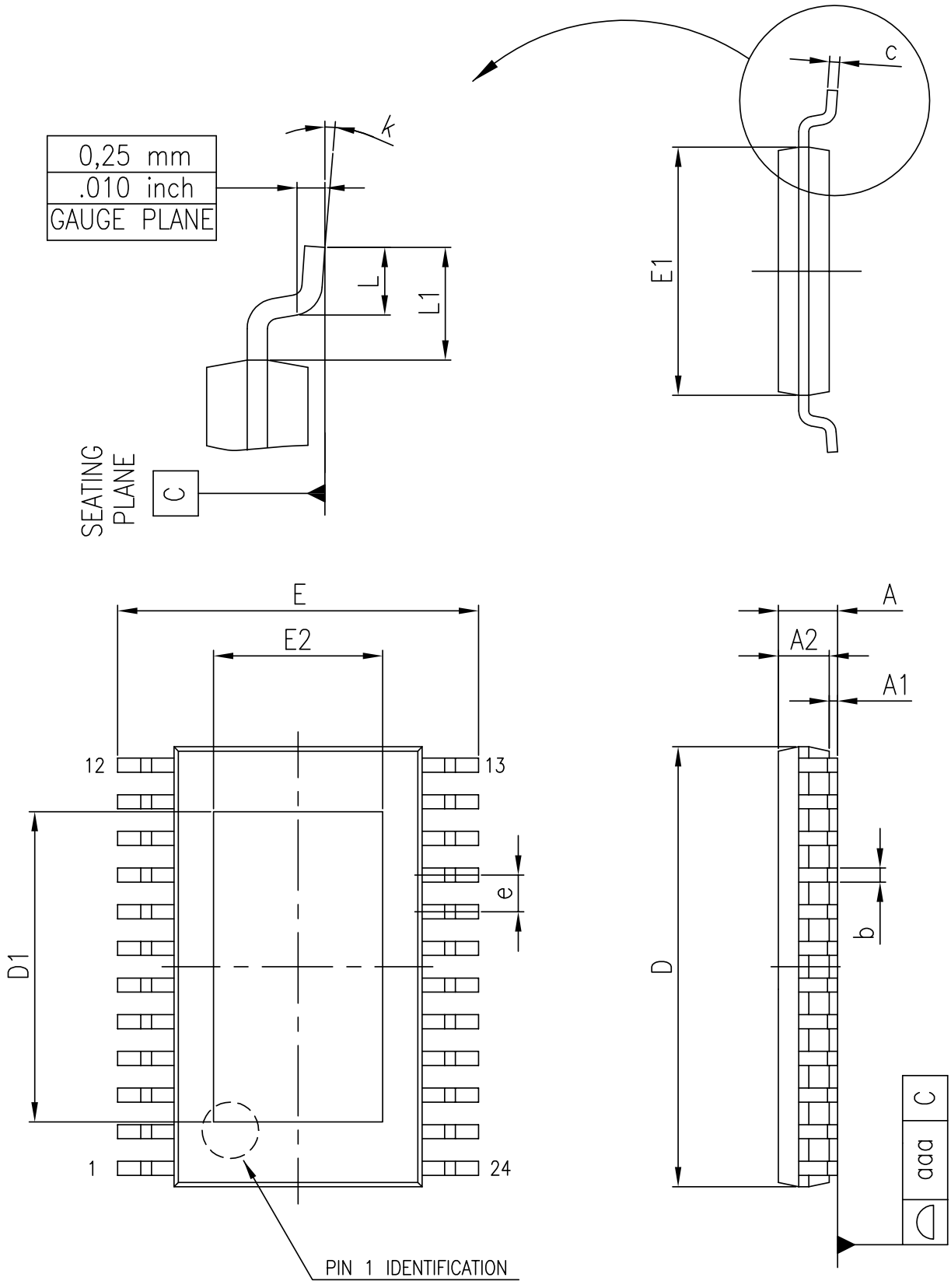


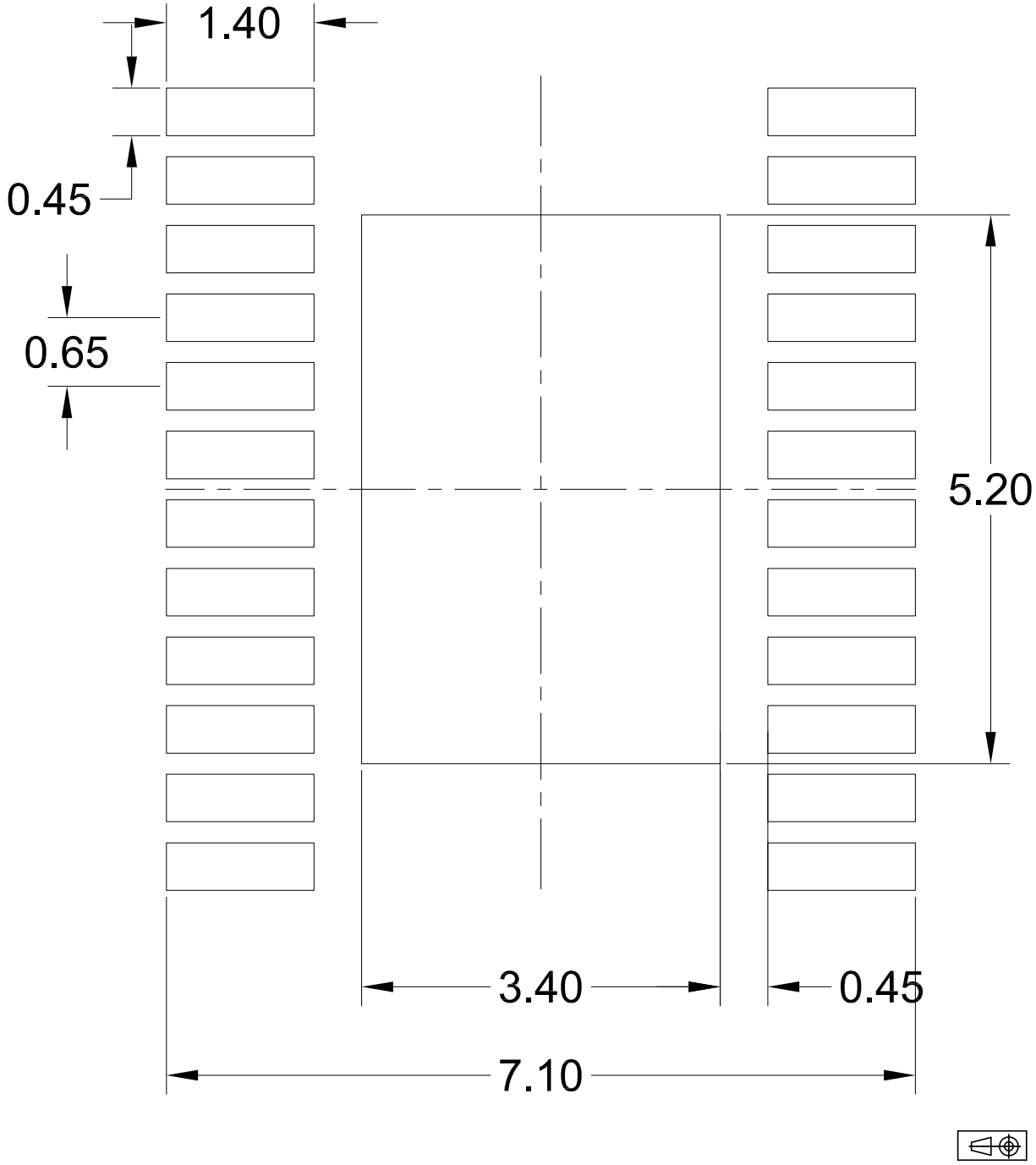
Table 5. HTSSOP24 (7.8x4.4x1.1 mm exp. pad down 5.0x3.2) mechanical data

Symbol	Dimensions			Note
	Min	Typ	Max	
A	1.05	1.10	1.20	1
A1	0.05	-	0.15	
A2	0.80	1.00	1.2	
b	0.19	-	0.30	
D	7.70	7.80	7.90	
D1	4.80	5.00	5.20	
E	6.20	6.40	6.60	
E1	4.30	4.40	4.50	2
E2	3.00	3.20	3.40	
e	0.65 BSC			
L	0.45	0.60	0.75	
L1	-	1.00	-	
K	0	-	8	Degrees
aaa	-	-	0.15	

Notes:

1. Very thin: 0.80 < A ≤ 1.00 mm / Fine pitch: e < 1.00mm
2. The pin #1 identifier must be present on the top surface of the package by using indentation mark or other feature of package body. Exact shape and size of this feature are optional.

Figure 8. **HTSSOP24 (7.8x4.4x1.1 mm exp. pad down 5.0x3.2) recommended footprint**



Revision history

Table 6. **Document revision history**

Date	Version	Changes
10-Nov-2020	1	Initial release.

Contents

List of tables

List of figures