Application Note

Atmel

Single-Wire and I²C Interfaces Seamless Debugging Using Saleae Logic Analyzer

ATSHA204A, ATECC108A, and ATECC508A

Prerequisites

- Hardware Prerequisites
 - Atmel[®] AT88CK490 or AT88CK590 Demo-Evaluation Board or Atmel AT88CK101-() Kit
 - Saleae Logic Analyzer
- Software Prerequisites
 - Atmel Crypto Evaluation Studio (ACES)

Introduction

The purpose of this document is to help the user gain a better understanding of how to use the Atmel CryptoAuthentication[™] ATSHA204A, ATECC108A, and ATECC508A devices (crypto device) with the Saleae Logic Analyzer. The Saleae Logic Analyzer is a powerful tool to debug and evaluate the commands coming to and from these devices. The tool supports both the standard I²C and the Atmel Single-Wire Interface (SWI) protocols.

The goal of this application note is to:

- Understand the bus interfaces of the crypto device using the Saleae Logic Analyzer.
- Develop and debug with the crypto device using the Saleae Logic Analyzer.

Summary

The Saleae Logic Analyzer provides an in depth tool to quickly develop and debug integration of the crypto device into a customer's system. The bus decoding allows for easy understanding of all bus traffic to the crypto device. By reducing the development time, the Saleae Logic Analyzer greatly reduces the cost of adding the crypto device.

1. Saleae Logic Analyzer

On load of the analyzer, either 8 or 16 channels will display depending on the analyzer used. Protocol specific settings are located on the far right under the heading, *Analyzers*.

Figure 1-1.	Channels and	Protocol Settings
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Q Salese Logic 11.13 - [Convected]	6	. 🛛 🕺
S0 M Semples • 24 MHz • Start		Options
The bast hope bay by but to be bad the lands be-		
		_
0-Channel 0	 Measurements 	
	Width: ###	
· · · · · · · · · · · · · · · · · · ·	Period: ###	
	IL ***	
1- Channel	120 T1 - T2 = ***	
	· testerer	-
	 Analyzers 	
2 - Channel 2 - Channel 2		
3-Ound3		

The crypto device supports either a Single-Wire Interface (SWI) or I²C Interface depending on the P/N.

- SWI Supported through the use of a DLL library. Use version 1.1.16 or greater. This version comes with support on Win, LNX, and IOS.
- I^2C Supported by the use of the built-in I^2C interface that is included in the Saleae download.



2. Single-Wire Interface (SWI)

Use the SWI DLL library version 1.1.16 or greater.

- Copy the DLL into the Saleae LLC\Analyzers directory on the user's PC. Once the driver has been copied to the correct folder, the Atmel SWI option will appear and be listed in the *Analyzer* drop-down options. The SWI Analyzer has three display modes:
 - Token
 - Byte
 - Packet (as described in the datasheet)

Salese Logic 11.15 - (Connected)			Deters
av manipital an mite avers			
0 - Channel 0 5	Analyzers	·	
		Atmel SWI	Width: ### Period: ### Frequency: ###
1- Channel IIII	Enlargement of the Analyzer	CAN	12: *** T1 - T2 = ***
	pull-down options.	DMX-512	▼ Analyzers Atmel SWI
2 - Channel 2		12C	CAN DMX-S12 I2C
		I2S / PCM	125 / PCM Manchester
3 - Channel J		Manchester	1-Wire Async Serial Simple Parallel
		1-Wire	SPI UNI/O
		Async Ser	Remove all
4 - Channel 4 5			

Figure 2-1. Atmel SWI Option

- 2. Select the Atmel SWI Analyzer from the list.
- 3. After selecting Atmel SWI Analyzer, rename the channel when prompted,
- 4. Select the *Falling Edge Trigger* option and start sampling. Using ACES, select a command and send it to the device. For an overview of the ACES tool, please see "Using ACES Application Note". This will cause the bus to become active and the Analyzer will trigger on the first falling edge and data line.

In the screen shot below, the Wake command has been captured followed by Wake Status Read. The Wake command is a special token designed to wake the device and reset the watchdog timer.







The token view displays each logic bit which is made up of seven bits on the wire. Each group of seven bits is encoded either as a Logic 1 or Logic 0 as follows:

- A Logic 1 is one low bit followed by six high bits.
- A Logic 0 is one low bit followed by one high bit, then by one low bit, and then by four high bits.

Solees Logic 1.1.1.5 - (Connected) = (24 MHz 50 M Samples) 50 M Samples • (24 MHz 50 M Samples) 50 M Samples • (24 MHz 50 M Samples) 50 Samples • (24 MHz 50 M Samples) 50

Figure 2-3. Token View

Figure 2-4. Logic Bits



The byte view builds on the token view by combining eight tokens into a single byte. This view allows for easy matching of information on the data bus to the command set defined in the datasheet. The byte view is transmitted with the less significant bit first.

Figure 2-5. Bytes

Saleae Logic 50 M Samples	1.1.15 · [Connected] ·	(24 MHz, 50 Start	M Samples]													- 0 ×	
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0 - SWI SDA 1 - Channel 1	J-1-														Measurements Width: ### Period: ### Frequency: ### IL: ### IL: ### T1 - T2 = ###	•	
															▼ Analyzers		
	W W														Atmel SWI	10	

The packet view further builds on the byte view by ordering the data into logic packets based on the datasheet definition. This allow for quick and easy review of the commands without the need to reference the datasheet.

Figure 2-6. Packets



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CryptoAuthentication for Single-Wire and I²C Interfaces Seamless Debugging Using Saleae Logic Analyzer [APPLICATION NOTE] Atmel-8847B-CryptoAuth-SWI-I2C-Seamless-Debugging-Saleae-Logic-Analyzer-ApplicationNote_082015



3. I²C Interface

The crypto device supports an I²C interface that is directly supported by the Saleae tool.

1. To configure the Analyzer for I²C, select the *I2C* option from the Analyzer drop-down list and follow the configuration guide.

Figure 3-1. I2C Analyzer Option



2. Select the clock and data channels that will be used for the I2C bus. Different encoding options can also be selected. The crypto device uses the default 8-bit encoding.

Figure 3-2. Clock and Data Channels

Q Salese Logic 1.1.15 - [Connected] 50 M Samples - 24 MHz - Start		- 0 X
1 Cound I Cound	 ✓ Measurements Width: ### Period: ### Frequency: ### T2: ### T2: ### T1: 17: 17: ### 	87
		Ŧ
2 - Channel 2 Jan Tan		
3 - Channel 3 SDA 0 · Channel 0 · · SCL 1 · Channel 1 · · Address Display 8-bit, read/write bit included [default] ·		
4 - Channel 4 J T.		W MA COM



5

3. Next, the *Update Channel Names* dialog box will be prompted to rename the channels to reflect SCL and SDA. This is an optional step, but helps when analyzing more then one bus at a time.

Q Salese Logic 1.1.15 - [Connected]		1 8
50 M Samples • 24 MHz • Start		Options
the bast maps has been been band the basis har-		
		_
0 - Channel 0	 Measurements 	97
	Width: 222 Period: ### Frequency: ### II: ### II: ###	
I - Channel I	T1 - T2 = ***	
	 Analyzers 	••
	₽C	
3 - Channel 3 3 - Channel 3 3 - Channel abels used by this analyzer?		
Sun Channed Sun		
A - Channel 4 - France Don't show again. Rename Don't Rename		

Figure 3-3. Update Channel Names

4. Now that the analyzer is configured, set-up the trigger settings. The Saleae has a One Shot trigger that can be triggered on either the falling or rising edge of the SCL channel. The bus is normally held high; therefore, setting a falling edge trigger is recommended.

Figure 3-4. Trigger Settings

Q_Saleae Logic 1.1.15 - (Connected)		0 ×
50 M Samples C 24 MHz C Start		Options
the base has the total ter and the ter		
0-SDA	 Measurements Width: ### Period. ### Frequency.### Ta: ### T2: ### 	97
	T1 - T2 = ###	92
	BC.	× •



5. Once the analyzer has been started, execute a command in order to generate data on the bus.

Figure 3-5. Execute a Command

Q Saleae Logic 1.1.15 - (Connected) - [24 MHz, 50 M Samples]	-	o x
50 M Samples 🔹 🖉 24 MHz 🔹 Start		Options
0-SDA	✓ Measurements	• -
	Width: FFF	
	Period: ###	
	II: ###	
	111-121=	
	 Analyzers 	
	DC[0%]	20
2 - Channel 2 - Channel 2		
J - Channel J - Channel -		
Waiting for Ingget		
Samples Collected: 44 M		
Sample receiping sectory to M		
4 - Channels (J _ L _) Memory Used: 0 MB		
Les Debi		

After the Analyzer has been triggered, it will collect the waveform information and display it in the viewer. The first token shown is the ATSHA204 Wake.

Figure 3-6. First Token — ATSHA204 Wake

Q Saleae Logi	1.1.15 - [Connected] - [24	MHz, 50 M Samples]							0 X
50 M Samples	• © 24 MHz •	Start							
	+8,ms	+9 ms		+1,ms	+3,ms	+4 ms	+5 ms	+6 ms	
0 - SDA	J, Y		•					Measurements Width: ### Period: ### Trequency: ### IL: ### IL: ### IL: ###	
1-50	2				in pui			* Analyzers	Ŧ
	- In the second second							DC	∞ ∞

The Wake command is a special command that is required to wake-up the device. The command consists of a I^2C Start event followed by a long period of Logic 0 on the SDA line, then followed a Stop event.

Figure	3-7.	Wake	Command

Q. Saleae Logi	c 1.1.15 - [Conne	cted] - [24 M	Hz, 50 M Sa	mples]																		le la	- 0	×
50 M Samples	• 🛛 24 MHz	•	Start																					tions =
+30 µs	+40 µs +50	µs +60jµa	•70 µs	+80 µs	+90 µs		+30 µs	+40 µs	+50 µs	s +60 μs	+70 µs	+90 µs	100 µs •	+10 µs	+20 µs	+30 µs	+40 µs	+50 µs	+60 µs	+70 µs	+80 µs	+90 µs	200 µs +	+10 µ
0 - SDA	[f, -, t, -																				 Measure Width: Period: Frequency T2: 	ements		0 -
1 - SCL		.]] [T1 - T2 : • Analyze	*** 15		**
																					₽C			× •



After a Wake command, an optional Read can be performed to read the status of the crypto device as shown in the waveform below. After the Read command is issued, the device will send four bytes of data (1-count, 1-data, and 2-CRC).





The Saleae tool supports a variety of display options for the I^2C interface including Binary, Hex, and ASCII to help quickly and easily evaluate the data. It can be selected by clicking the *Configuration* button next to the analyzer of interest on the right.



Figure 3-9. Display Options

4. Revision History

Doc. Rev.	Date	Comments
8847B	08/2015	Updated for ATSHA204A, ATECC108A, and ATECC508A devices.
8847A	01/2013	Initial document release.



Atmel Enabling Unlimited Possibilities



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Atmel Corporation

1600 Technology Drive, San Jose, CA 95110 USA T:

T: (+1)(408) 441.0311

F: (+1)(408) 436.4200

www.atmel.com

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