SARA-R5 series

LTE-M / NB-IoT modules with secure cloud

System integration manual

Abstract

This document describes the features and the integration of the size-optimized SARA-R5 series cellular modules, based on the u-blox UBX-R5 cellular chipset. The modules are specifically designed for IoT, integrating an in-house developed cellular modem, end-to-end trusted domain security and u-blox's leading GNSS technology. The modules deliver high performance satellite positioning alongside data connectivity in the very small and compact SARA form factor.

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Functional sample	Draft	For functional testing. Revised and supplementary data will be published later.
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Engineering sample	Advance information	Data based on early testing. Revised and supplementary data will be published later.
Initial production	Early production information	Data from product verification. Revised and supplementary data may be published later.
Mass production / End of life	Production information	Document contains the final product specification.

This document applies to the following products:

Product name	Type number	Modem version	Application version	PCN reference	Product status
SARA-R500S	SARA-R500S-00B-00	02.05	A00.01	UBX-20037360	Obsolete
	SARA-R500S-00B-01	02.06	A00.01	UBX-20053099	Initial production
	SARA-R500S-01B-00	03.14	A00.01	UBX-21028004	Engineering sample
SARA-R510S	SARA-R510S-00B-00	02.05	A00.01	UBX-20037360	Obsolete
	SARA-R510S-00B-01	02.06	A00.01	UBX-20053099	Initial production
	SARA-R510S-01B-00	03.14	A00.01	UBX-21028004	Engineering sample
SARA-R510M8S	SARA-R510M8S-00B-00	02.05	A00.01	UBX-20037360	Obsolete
	SARA-R510M8S-00B-01	02.06	A00.01	UBX-20053099	Initial production
	SARA-R510M8S-01B-00	03.14	A00.01	UBX-21028004	Engineering sample

Contents

1 System description

1.1 Overview

The SARA-R5 series LTE Cat M1 / NB2 modules are ideal solutions for IoT, in the miniature SARA LGA form factor (26.0 x 16.0 mm, 96-pin). They allow an easy integration into compact designs and a seamless drop-in migration from other u-blox cellular module families.

SARA-R5 series modules are form-factor compatible with u-blox LISA, LARA and TOBY cellular module families and are pin-to-pin compatible with u-blox SARA-R4, SARA-N, SARA-G and SARA-U cellular module families. This facilitates migration from u-blox cellular modules supporting various radio access technologies, maximizes customer investments, simplifies logistics, and enables very short time-to-market. See Table 1 for a summary of the main features and interfaces.

Model	Region	RAT			Positioning				Interfaces							Features														Grade		
		3GPP Release Baseline	3GPP LTE category	LTE FDD bands	Integrated GNSS receiver	External GNSS control via modem	AssistNow software	CellLocate®	UART	USB (for diagnostics)	SPI	SDIO	I2C	GPIOs	Digital audio (I2S)	Secure Cloud services Ver 1.1	Embedded Secure Element EAL5+ High	Antenna dynamic tuning	CellTime™	Ultra-low power consumption in PSM / eDRX	Embedded TCP/UDP stack	Embedded HTTP, FTP	Embedded TLS, DTLS	FW update via serial (FOAT)	u-blox Firmware update Over the Air (uFOTA)	LwM2M with dynamically loaded objects	Embedded MQTT, MQTT-SN	Embedded CoAP	Last gasp	Jamming detection	Antenna and SIM detection	Standard	Professional	Automotive
SARA-R500S	Multi Region	14	M1 NB2	*		•	•	•	•	•	○	○	•	•	○	•	•	•	•		•	•	•	•	•	•	•	•	•	•	•		•	
SARA-R510S	Multi Region	14	M1 NB2	*		•	•	•	•	•	○	○	•	•	○	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•		•	
SARA-R510M8S	Multi Region	14	M1 NB2	*	•		•	•	•	•	○	○	•	•	○	•	•	•	•		•	•	•	•	•	•	•	•	•	•	•		•	

* = LTE Bands 1, 2, 3, 4, 5, 8, 12, 13, 18, 19, 20, 25, 26, 28, 66, 71, 85

• = supported by all FW versions ○ = supported by future FW versions

Table 1: SARA-R5 series main features summary

☞ The “00B” product versions of the SARA-R5 series modules do not support the LTE NB-IoT Radio Access Technology, and the LTE FDD bands 66, 71, 85.

With a discrete, hardware-based secure element and a lightweight pre-shared key management system, u-blox offers state-of-the-art security that is ideal for IoT applications and includes local data protection, zero touch provisioning, anti-cloning, and local secure chip-to-chip communication. SARA-R5 series modules are the optimal choice for LPWA applications with low to medium data throughput rates, as well as devices that require long battery lifetimes, such as used in smart metering, smart cities, telematics, and connected health.

The modules support handover capability and delivers the technology necessary for use in applications such as vehicle, asset and people tracking where mobility is a pre-requisite. Other applications where the modules are well-suited include and are not limited to: smart home, security systems, industrial monitoring and control.

The modules support multi-band data communication over an extended operating temperature range of –40 to +85 °C, with extremely low power consumption, and with coverage enhancement for deeper range into buildings and basements (and underground with NB2).

SARA-R5 series modules include the following variants / product versions:

- SARA-R500S LTE Cat M1 / NB2 module for multi-region use, cost effective solution for devices that do not need to reach ultra-low power consumption in PSM / eDRX deep-sleep mode
- SARA-R510S LTE Cat M1 / NB2 module for multi-region use, designed to achieve extremely low current consumption in PSM / eDRX deep-sleep mode
- SARA-R510M8S LTE Cat M1 / NB2 module for multi-region use, integrating the u-blox M8 GNSS receiver for global position acquisition

Table 2 summarizes cellular and GNSS characteristics of the modules.

Item	SARA-R500S	SARA-R510S	SARA-R510M8S
Cellular protocol stack	3GPP release 14	3GPP release 14	3GPP release 14
Cellular RAT	LTE Cat M1 Half-Duplex LTE Cat NB2 Half-Duplex	LTE Cat M1 Half-Duplex LTE Cat NB2 Half-Duplex	LTE Cat M1 Half-Duplex LTE Cat NB2 Half-Duplex
Cellular LTE FDD bands	Band 1 (2100 MHz) Band 2 (1900 MHz) Band 3 (1800 MHz) Band 4 (1700 MHz) Band 5 (850 MHz) Band 8 (900 MHz) Band 12 (700 MHz) Band 13 (750 MHz) Band 18 (850 MHz) Band 19 (850 MHz) Band 20 (800 MHz) Band 25 (1900 MHz) Band 26 (850 MHz) Band 28 (700 MHz) Band 66 (1700 MHz) Band 71 (600 MHz) Band 85 (700 MHz)	Band 1 (2100 MHz) Band 2 (1900 MHz) Band 3 (1800 MHz) Band 4 (1700 MHz) Band 5 (850 MHz) Band 8 (900 MHz) Band 12 (700 MHz) Band 13 (750 MHz) Band 18 (850 MHz) Band 19 (850 MHz) Band 20 (800 MHz) Band 25 (1900 MHz) Band 26 (850 MHz) Band 28 (700 MHz) Band 66 (1700 MHz) Band 71 (600 MHz) Band 85 (700 MHz)	Band 1 (2100 MHz) Band 2 (1900 MHz) Band 3 (1800 MHz) Band 4 (1700 MHz) Band 5 (850 MHz) Band 8 (900 MHz) Band 12 (700 MHz) Band 13 (750 MHz) Band 18 (850 MHz) Band 19 (850 MHz) Band 20 (800 MHz) Band 25 (1900 MHz) Band 26 (850 MHz) Band 28 (700 MHz) Band 66 (1700 MHz) Band 71 (600 MHz) Band 85 (700 MHz)
Cellular power class	LTE power class 3 (23 dBm)	LTE power class 3 (23 dBm)	LTE power class 3 (23 dBm)
Cellular data rate	LTE category M1: up to 1200 kbit/s UL up to 375 kbit/s DL LTE category NB2: up to 140 kbit/s UL up to 125 kbit/s DL	LTE category M1: up to 1200 kbit/s UL up to 375 kbit/s DL LTE category NB2: up to 140 kbit/s UL up to 125 kbit/s DL	LTE category M1: up to 1200 kbit/s UL up to 375 kbit/s DL LTE category NB2: up to 140 kbit/s UL up to 125 kbit/s DL
GNSS receiver	-	-	72-channel u-blox M8 engine GPS L1C/A, SBAS L1C/A, QZSS L1C/A, QZSS L1-SAIF, GLONASS L1OF, BeiDou B1I, Galileo E1B/C

Table 2: SARA-R5 series modules cellular and GNSS characteristics summary

☞ The “00B” product versions of the SARA-R5 series modules do not support the LTE NB-IoT Radio Access Technology, and the LTE FDD bands 66, 71, 85.

☞ The “00B” product versions of the SARA-R5 series modules do not support eDRX deep-sleep mode.

1.2 Architecture

Figure 1, Figure 2 and Figure 3 summarize the internal architecture of the SARA-R500S modules, SARA-R510S modules, and SARA-R510M8S modules, respectively.

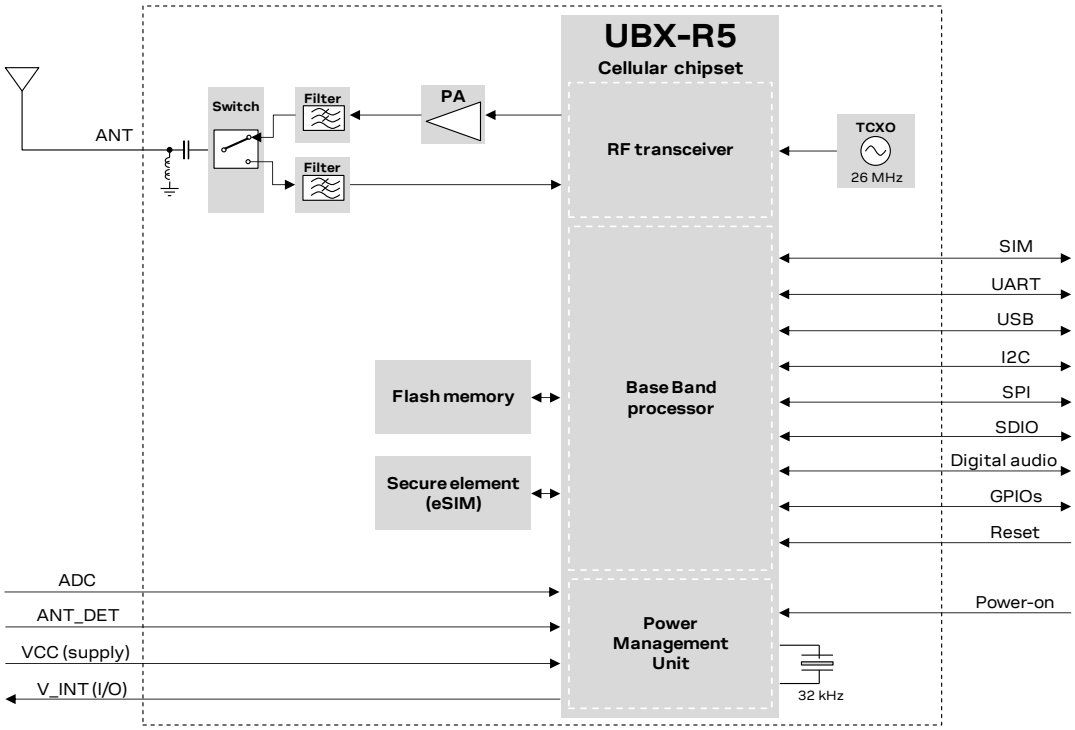

Figure 1: SARA-R500S block diagram

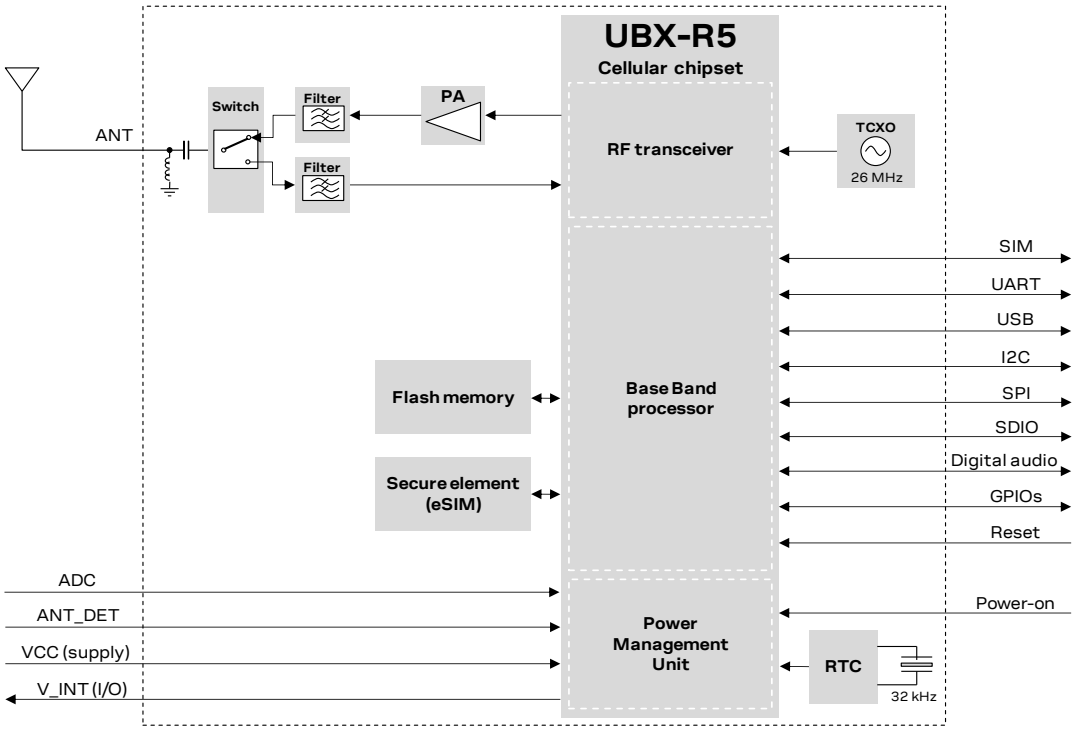

Figure 2: SARA-R510S block diagram

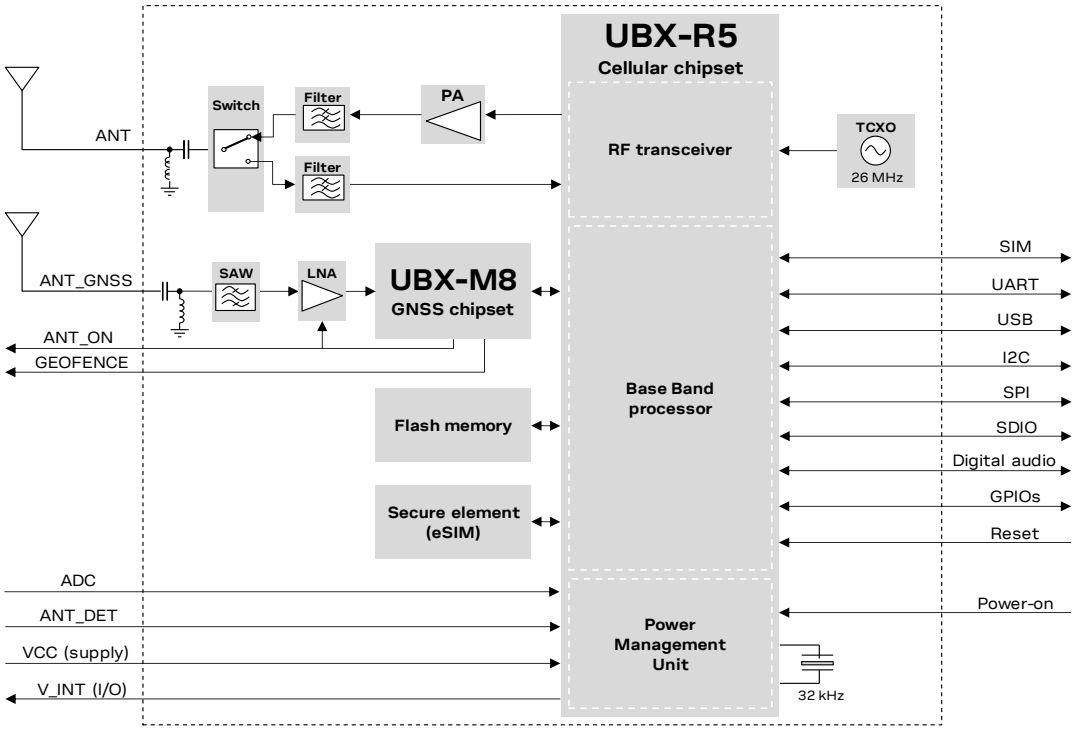

Figure 3: SARA-R510M8S block diagram

☞ The “00B” product versions of the SARA-R5 series modules do not support the following interfaces, which should be left unconnected and should not be driven by external devices:

- SPI interface
- SDIO interface
- Digital audio (I2S) interface
- ADC
- ANT_ON
- GEOFENCE

☞ The “01B” product versions of the SARA-R5 series modules do not support the following interfaces, which should be left unconnected and should not be driven by external devices:

- SPI interface
- SDIO interface
- Digital audio (I2S) interface

SARA-R5 series modules internally consist of the following sections described herein with more details than the simplified block diagrams of Figure 1, Figure 2 and Figure 3.

RF section

The RF section is composed of the following main elements:

- RF switch connecting the antenna port (**ANT**) to the suitable RF Tx / Rx paths for LTE Cat M1 / NB2 Half-Duplex operations
- Power Amplifiers (PA) amplifying the Tx signal modulated and pre-amplified by the RF transceiver
- RF filters along the Tx and Rx signal paths providing RF filtering

- RF transceiver integrated in the u-blox UBX-R5 cellular chipset, performing modulation, up-conversion and pre-amplification of the baseband signals for LTE transmission, and performing down-conversion and demodulation of the RF signal for LTE reception
- 26 MHz Temperature-Controlled Crystal Oscillator (TCXO) generating the reference clock signal for the cellular RF transceiver, the baseband system and the GNSS system, when the related system is in active mode or connected mode.

Baseband and power management section

The baseband and power management section, based on the u-blox UBX-R5 cellular chipset, is composed of the following main elements:

- On-chip modem processor, vector signal processor, with dedicated hardware assistance for signal processing and system timing
- On-chip modem processor, with interfaces control functions
- On-chip voltage regulators to derive all the internal or external (**V_SIM**, **V_INT**) supply voltages from the module supply input **VCC**
- On-chip cryptographic hardware acceleration with Root of Trust
- On-chip memory system, including PSRAM and secure boot ROM
- Dedicated flash memory IC
- Dedicated secure element
- 32.768 kHz crystal oscillator to provide the clock reference in the low power idle mode, which can be enabled using the +UPSV AT command, and in the PSM / eDRX[1] deep-sleep mode

GNSS section

The GNSS section, based on the u-blox UBX-M8 GNSS chipset, is composed of the following main elements illustrated in Figure 4:

- u-blox UBX-M8030 concurrent GNSS chipset with SPG 3.01 firmware version
- Dedicated SAW filter
- Additional Low Noise Amplifier (LNA)
- 26 MHz Temperature-Controlled Crystal Oscillator (TCXO) generating the reference clock signal for the cellular RF transceiver, the baseband system and the GNSS system

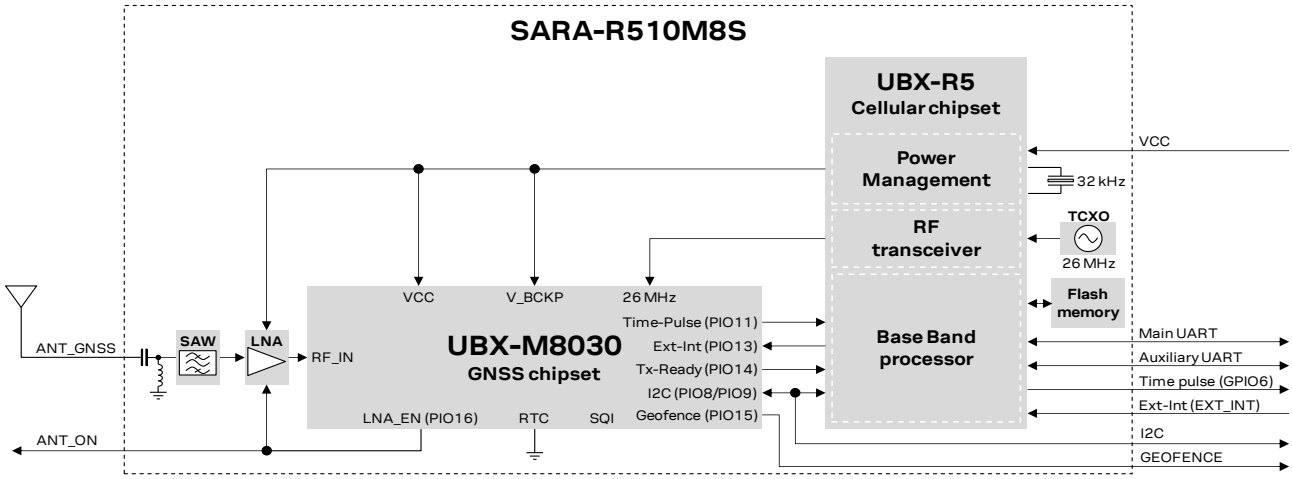

Figure 4: SARA-R510M8S modules GNSS section block diagram

[1] eDRX deep-sleep mode is not supported by "00B" product versions

1.3 Pin-out

Table 3 lists the pin-out of the SARA-R5 series modules, with pins grouped by function.

Function	Pin name	Pin no.	I/O	Description	Remarks
Power	VCC	51,52,53	I	Module supply input	VCC supply circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.5.1 for functional description / requirements. See section 2.2.1 for external circuit design-in.
	GND	1,3,5,14 20,21[2] 22,30,32 43,50,54 55,57-61 63-96	N/A	Ground	GND pins are internally connected to each other. External ground connection affects the RF and thermal performance of the device. See section 1.5.1 for functional description. See section 2.2.1 for external circuit design-in.
	V_INT	4	O	Generic digital interfaces supply output	V_INT = 1.8 V (typical) generated by internal regulator when the module is switched on, outside the low power PSM / eDRX[3] deep-sleep mode. See section 1.5.2 for functional description. See section 2.2.2 for external circuit design-in. Provide test point for diagnostic purposes.
System	PWR_ON	15	I	Power-on input	Internal active pull-up. Active low. See sections 1.6.1, 1.6.2 for functional description. See section 2.3.1 for external circuit design-in. Provide test point for diagnostic purposes.
	RESET_N	18	I	External reset input	Internal active pull-up. Active low. See section 1.6.3 for functional description. See section 2.3.2 for external circuit design-in. Provide test point for diagnostic purposes.
Antenna	ANT	56	I/O	Cellular antenna	50 Ω nominal characteristic impedance. Antenna circuit affects the RF performance and application device compliance with required certification schemes. See section 1.7.1 for functional description / requirements. See section 2.4.2 for external circuit design-in.
	ANT_GNSS	31	I	GNSS antenna [4]	50 Ω nominal characteristic impedance. See section 1.7.2 for functional description / requirements. See section 2.4.3 for external circuit design-in.
	ANT_DET	62	I	Antenna detection	ADC for antenna presence detection function. See section 1.7.3 for functional description. See section 2.4.5 for external circuit design-in.
SIM	VSIM	41	O	SIM supply output	VSIM = 1.8 V / 3 V output as per the connected SIM type. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_IO	39	I/O	SIM data	Data input/output for 1.8 V / 3 V SIM. Internal pull-up to VSIM. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_CLK	38	O	SIM clock	Clock output for 1.8 V / 3 V SIM. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_RST	40	O	SIM reset	Reset output for 1.8 V / 3 V SIM. See section 1.8 for functional description. See section 2.5 for external circuit design-in.

[2] "00B" product versions only
[3] eDRX deep-sleep mode is not supported by "00B" product versions
[4] Not supported by SARA-R500S and SARA-R510S modules

Function	Pin name	Pin no.	I/O	Description	Remarks
UART	RXD	13	O	UART data output	USIO variants 0 / 1 / 2 / 3 / 4: Primary UART circuit 104 (RxD) in ITU-T V.24, for AT, data, Mux, FOAT, FW update via u-blox EasyFlash tool. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in. Provide test point for FW update purposes.
	TXD	12	I	UART data input	USIO variants 0 / 1 / 2 / 3 / 4: Primary UART circuit 103 (TxD) in ITU-T V.24, for AT, data, Mux, FOAT, FW update via u-blox EasyFlash tool. Internal active pull-up enabled. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in. Provide test point for FW update purposes.
	CTS	11	O	UART clear to send output	USIO variants 0 / 1 / 2 / 3 / 4: Primary UART circuit 106 (CTS) in ITU-T V.24. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	RTS	10	I	UART request to send input	USIO variants 0 / 1 / 2 / 3 / 4: Primary UART circuit 105 (RTS) in ITU-T V.24. Internal active pull-up enabled. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	DSR	6	O / I	UART data set ready output / AUX UART request to send input	USIO variant 0: Pin disabled USIO variant 1: Primary UART circuit 107 (DSR) in ITU-T V.24. USIO variants 2 / 3 / 4: Auxiliary UART circuit 105 (RTS) in ITU-T V.24. Internal active pull-up enabled. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	RI	7	O / O	UART ring indicator output / AUX UART clear to send output	USIO variants 0 / 1: Primary UART circuit 125 (RI) in ITU-T V.24. USIO variants 2 / 3 / 4: Auxiliary UART circuit 106 (CTS) in ITU-T V.24. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	DTR	9	I / I	UART data terminal ready input / AUX UART data input	USIO variants 0 / 1: Primary UART circuit 108/2 (DTR) in ITU-T V.24. Internal active pull-up enabled. USIO variants 2 / 3 / 4: Auxiliary UART circuit 103 (TxD) in ITU-T V.24, for AT, data, GNSS tunneling, FOAT, diagnostics. Internal active pull-up enabled. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in. Provide test point for diagnostic purposes.
	DCD	8	O / O	UART data carrier detect output / AUX UART data output	USIO variant 0: Pin disabled. USIO variant 1: Primary UART circuit 109 (DCD) in ITU-T V.24. USIO variants 2 / 3 / 4: Auxiliary UART circuit 104 (RxD) in ITU-T V.24, for AT, data, GNSS tunneling, FOAT, diagnostics. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in. Provide test point for diagnostic purposes.

Function	Pin name	Pin no.	I/O	Description	Remarks
USB	VUSB_DET	17	I	USB detect input	VBUS USB supply generated by the host must be connected to this input pin to enable the USB interface. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in. Provide test point for diagnostic purposes.
	USB_D-	28	I/O	USB Data Line D-	USB interface for diagnostics. 90 Ω nominal differential impedance. Pull-up, pull-down and series resistors, as required by the USB 2.0 specification [4], are part of the USB pin driver and shall not be provided externally. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in. Provide test point for diagnostic purposes.
	USB_D+	29	I/O	USB Data Line D+	USB interface for diagnostics. 90 Ω nominal differential impedance. Pull-up, pull-down and series resistors, as required by the USB 2.0 specification [4], are part of the USB pin driver and shall not be provided externally. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in. Provide test point for diagnostic purposes.
SPI	SDIO_D0	47	I/O	SPI data output	SPI data output, alternatively settable as SDIO. SPI supported by “00B” / “01B” versions for diagnostics only.
	SDIO_D1	49	I/O	SPI data input	SPI data input, alternatively settable as SDIO. SPI supported by “00B” / “01B” versions for diagnostics only.
	SDIO_D2	44	I/O	SPI clock	SPI clock, alternatively configurable as SDIO. SPI supported by “00B” / “01B” versions for diagnostics only.
	SDIO_D3	48	I/O	SPI Chip Select	SPI Chip Select, alternatively configurable as SDIO. SPI supported by “00B” / “01B” versions for diagnostics only.
SDIO	SDIO_D0	47	I/O	SDIO serial data [0]	Alternatively configurable as SPI MOSI. SDIO not supported by “00B” and “01B” versions.
	SDIO_D1	49	I/O	SDIO serial data [1]	Alternatively configurable as SPI MISO. SDIO not supported by “00B” and “01B” versions.
	SDIO_D2	44	I/O	SDIO serial data [2]	Alternatively configurable as SPI clock. SDIO not supported by “00B” and “01B” versions.
	SDIO_D3	48	I/O	SDIO serial data [3]	Alternatively settable as SPI Chip Select. SDIO not supported by “00B” and “01B” versions.
	SDIO_CLK	45	O	SDIO serial clock	SDIO not supported by “00B” and “01B” versions.
	SDIO_CMD	46	I/O	SDIO command	Alternatively configurable by +UGPIOC AT command. SDIO not supported by “00B” and “01B” versions.
I2C	SCL	27	O	I2C bus clock line	Fixed open drain, for communication with I2C-local devices. Internal active pull-up: external pull-up is not required. See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.
	SDA	26	I/O	I2C bus data line	Fixed open drain, for communication with I2C-local devices. Internal active pull-up: external pull-up is not required. See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.
Audio	I2S_TXD	35	O	I2S transmit data	Alternatively configurable by +UTEST AT command. I2S not supported by “00B” and “01B” versions.
	I2S_RXD	37	I	I2S receive data	I2S not supported by “00B” and “01B” versions.
	I2S_CLK	36	I/O	I2S clock	I2S not supported by “00B” and “01B” versions.
	I2S_WA	34	I/O	I2S word alignment	Alternatively configurable by +UTEST AT command. I2S not supported by “00B” and “01B” versions.

Function	Pin name	Pin no.	I/O	Description	Remarks
ADC	ADC	21 [5]	I	ADC input	See section 1.11 for functional description. See section 2.8 for external circuit design-in.
GPIO	GPIO1	16	I/O	GPIO	Pin with alternatively configurable functions. See section 1.12 for functional description. See section 2.9 for external circuit design-in.
	GPIO2	23	I/O	GPIO	Pin with alternatively configurable functions. See section 1.12 for functional description. See section 2.9 for external circuit design-in.
	GPIO3	24	I/O	GPIO	Pin with alternatively configurable functions. See section 1.12 for functional description. See section 2.9 for external circuit design-in.
	GPIO4	25	I/O	GPIO	Pin with alternatively configurable functions. See section 1.12 for functional description. See section 2.9 for external circuit design-in.
	GPIO5	42	I/O	GPIO	Pin with alternatively configurable functions. See sections 1.8.2 and 1.12 for functional description. See sections 2.5 and 2.9 for external circuit design-in.
	GPIO6	19	I/O	GPIO	Pin with alternatively configurable functions. See section 1.12 for functional description. See section 2.9 for external circuit design-in.
	I2S_TXD	35	O	Pin for antenna dynamic tuning	Configurable as output for antenna dynamic tuning. See section 1.12 for functional description. See section 2.9 for external circuit design-in.
	I2S_WA	34	O	Pin for antenna dynamic tuning	Configurable as output for antenna dynamic tuning. See section 1.12 for functional description. See section 2.9 for external circuit design-in.
	EXT_INT	33	I	External interrupt	Configurable as interrupt input triggering the generation of an URC time stamp. Internal active pull-down enabled. See section 1.12 for functional description. See section 2.9 for external circuit design-in.
	SDIO_CMD	46	I	External GNSS time pulse input	Configurable as input for external GNSS time pulse. Not supported by SARA-R510M8S modules. See section 1.12 for functional description. See section 2.9 for external circuit design-in.
GNSS PIOs	GEOFENCE [6] (I2S_CLK)	36	O	Geofencing status indication	Configurable to provide optional indication of the geofencing status. See section 1.13 for functional description. See section 2.10 for external circuit design-in.
	ANT_ON [6] (I2S_RXD)	37	O	Antenna or LNA enable	External GNSS active antenna and/or LNA on/off signal driven by u-blox M8 chipset, connected to internal LNA. See section 1.13 for functional description. See section 2.10 for external circuit design-in.
Reserved	RSVD	2	N/A	Reserved pin	Leave unconnected. See sections 1.14 and 2.11.

Table 3: SARA-R5 series modules pin definition, grouped by function

[5] Not supported by "00B" product versions
[6] Not supported by SARA-R500S, SARA-R510S and SARA-R510M8S-00B modules

1.4 Operating modes

SARA-R5 series modules have several operating modes as defined in Table 4.

General Status	Operating Mode	Definition
Power-down	**Not-powered mode**	**VCC** supply not present or below operating range: module is switched off.
	Power-off mode	**VCC** supply within operating range and module is switched off.
Normal operation	**Deep-sleep mode**	RTC runs with 32 kHz reference internally generated.
	Idle mode	Module processor runs with 32 kHz reference internally generated.
	Active mode	Module processor runs with 26 MHz reference internally generated.
	Connected mode	RF Tx/Rx data connection enabled and processor core runs with 26 MHz reference.

Table 4: SARA-R5 series modules operating modes definition

Figure 5 describes the transition between the different operating modes.

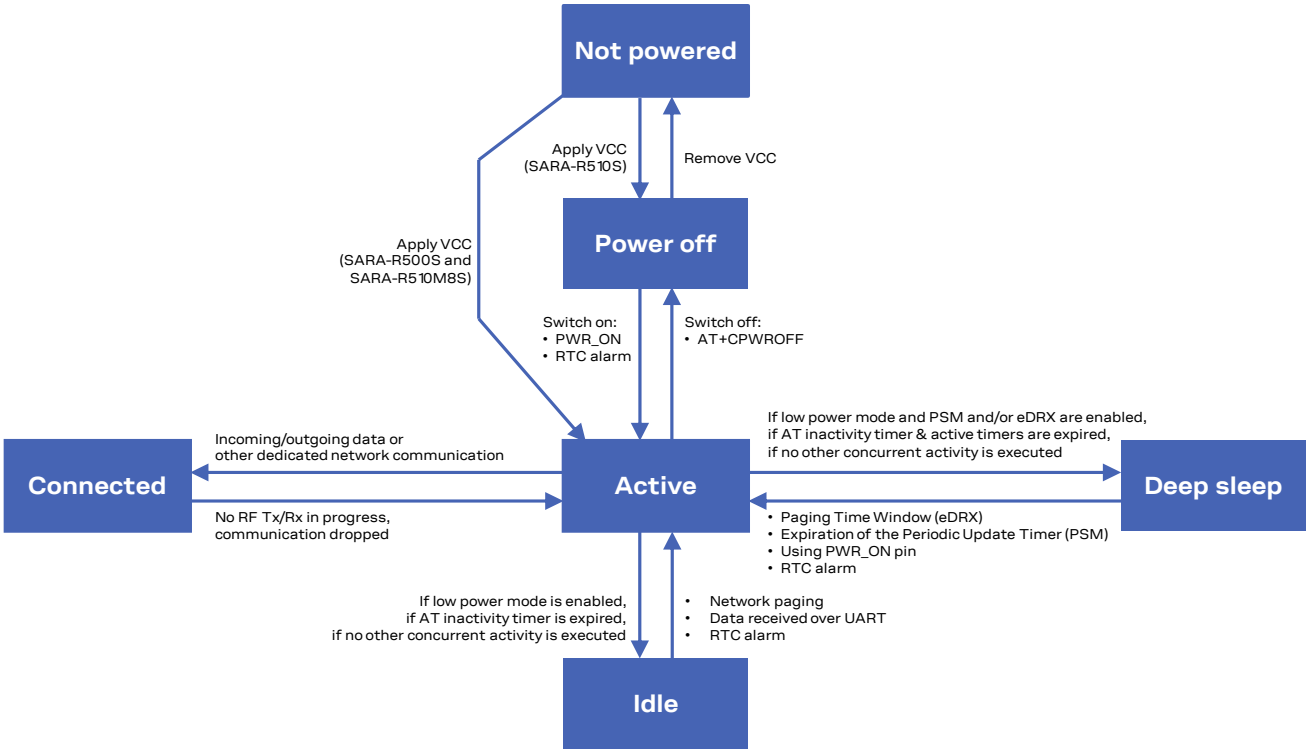

Figure 5: SARA-R5 series modules operating modes transitions

The initial operating mode of SARA-R5 series modules is the one with **VCC** supply not present or below the operating range: the modules are switched off in not-powered mode.

Once a valid **VCC** supply is applied to the SARA-R500S and the SARA-R510M8S modules, this event triggers the switch-on routine of the modules that subsequently enter the active mode.

Instead, once a valid **VCC** supply is applied to the SARA-R510S modules, they remain switched off in power-off mode. Then the proper toggling of the **PWR_ON** input line is necessary to trigger the switch-on routine of the modules that subsequently enter the active mode.

SARA-R5 series modules are fully ready to operate when in active mode: the available communication interfaces are completely functional and the module can accept and respond to any AT command, entering connected mode upon LTE signal reception / transmission.

The internal GNSS functionality can be concurrently enabled on the SARA-R510M8S modules by the dedicated +UGPS AT command, as well as the possible external GNSS function can be concurrently enabled using SARA-R500S or SARA-R510S modules by the dedicated +UGPS AT command.

Then, the SARA-R5 series modules switch from active mode to the low power idle mode whenever possible, if the low power configuration is enabled by the dedicated +UPSV AT command. The low power idle mode can last for different time periods according to the specific +UPSV AT command setting, according to the specific +CEDRXS / +CEDRXRDP AT commands setting, and according to the concurrent activities executed by the module, as for example according to the concurrent GNSS activities. For eDRX cycles equal or longer than 327.68 s, the SARA-R500S and SARA-R510M8S modules can enter the eDRX deep-sleep mode and the SARA-R510S modules can enter the ultra-low power eDRX deep-sleep mode, out of the Paging Time Window (PTW).

Then, after having enabled the low power configuration by the dedicated +UPSV AT command, according to the +CPSMS / +UCPSMS AT commands setting, and according to the concurrent activities executed by the module (for example according to the concurrent GNSS activities), whenever possible the SARA-R500S and SARA-R510M8S modules can enter the PSM deep-sleep mode and the SARA-R510S modules can enter the ultra-low power PSM deep-sleep mode.

Once the modules enter the PSM / eDRX deep-sleep mode (SARA-R500S and SARA-R510M8S modules) or the ultra-low power PSM / eDRX deep-sleep mode (SARA-R510S modules), the available communication interfaces are not functional: the expiration of the “Periodic Update Timer” negotiated with the LTE network (for PSM cycles), the PTW occurrence (for eDRX cycles) or a wake up event, consisting in proper toggling of the **PWR_ON** input line, is necessary to trigger the wake up routine of the modules that subsequently enter back into the active mode.

SARA-R5 series modules can be gracefully switched off by the dedicated +CPWROFF AT command.

☞ The “00B” product versions of the SARA-R5 series modules do not support eDRX deep-sleep mode.

☞ See the SARA-R5 series AT commands manual [2], +UPSV, +CEDRXS, +CEDRXRDP, +CPSMS, +UCPSMS, +UPSMVER, +UGPS, +CALA, +CPWROFF AT commands, for possible configurations and settings of different operating modes.

1.5 Supply interfaces

1.5.1 Module supply input (VCC)

The modules must be supplied via the three **VCC** pins that represent the module power supply input.

Voltage must be stable, because during operation, the current drawn by the SARA-R5 series modules through the **VCC** pins may vary significantly, depending on the operating mode and state (as described in sections 1.5.1.2, 1.5.1.3, 1.5.1.4 and 1.5.1.5).

It is important that the supply source can withstand the average current consumption occurring during Tx / Rx call at maximum RF power level (see the SARA-R5 series data sheet [1]).

The 3 **VCC** pins of SARA-R5 series modules are internally connected each other to both the internal power amplifier and the internal baseband power management unit.

Figure 6 provides a simplified block diagram of SARA-R5 series modules’ internal VCC supply routing.

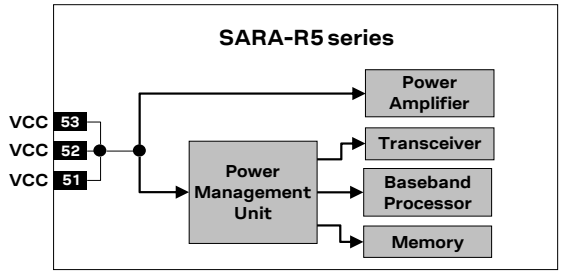

Figure 6: Block diagram of SARA-R5 series modules’ internal VCC supply routing

1.5.1.1 VCC supply requirements

Table 5 summarizes the requirements for the VCC modules supply. See section 2.2.1 for suggestions to correctly design a **VCC** supply circuit compliant with the requirements listed in Table 5.

⚠ The supply circuit affects the RF compliance of the device integrating SARA-R5 series modules with applicable required certification schemes as well as antenna circuit design. Compliance is guaranteed if the requirements summarized in the Table 5 are fulfilled.

Item	Requirement	Remark
VCC nominal voltage	Within **VCC** normal operating range: 3.3 V / 4.4 V	RF performance is guaranteed when **VCC** voltage is inside the normal operating range limits. RF performance may be affected when **VCC** voltage is outside the normal operating range limits, though the module is still fully functional until the **VCC** voltage is inside the extended operating range limits.
VCC voltage during normal operation	Within **VCC** extended operating range: 3.0 V / 4.5 V	**VCC** voltage must be above the extended operating range minimum limit to switch-on the module. The module may switch-off when the **VCC** voltage drops below the extended operating range minimum limit. Operation above **VCC** extended operating range is not recommended and may affect device reliability.
VCC current	Support with adequate margin the highest averaged **VCC** current consumption value during Tx conditions specified in the SARA-R5 series data sheet [1]	The maximum average current consumption can be greater than the specified value according to the actual antenna mismatching, temperature and supply voltage. Section 1.5.1.2 describes current consumption profiles in connected mode.
VCC voltage ripple	Noise in the supply pins must be minimized	High supply voltage ripple values during RF transmissions in connected mode directly affect the RF compliance with the applicable certification schemes.

Table 5: Summary of VCC modules supply requirements

1.5.1.2 VCC current consumption in LTE connected mode

During an LTE connection, the SARA-R5 series modules transmit and receive in half duplex mode. The current consumption depends on output RF power, which is always regulated by the network (the current base station) sending power control commands to the module. These power control commands are logically divided into a slot of 0.5 ms (time length of one Resource Block), thus the rate of power change can reach a maximum rate of 2 kHz.

Figure 7 shows an example of SARA-R5 series modules' current consumption profile versus time in connected mode: transmission is enabled for one sub-frame (1 ms) according to LTE Category M1 half-duplex connected mode. For detailed consumption values, see the SARA-R5 series data sheet [1].

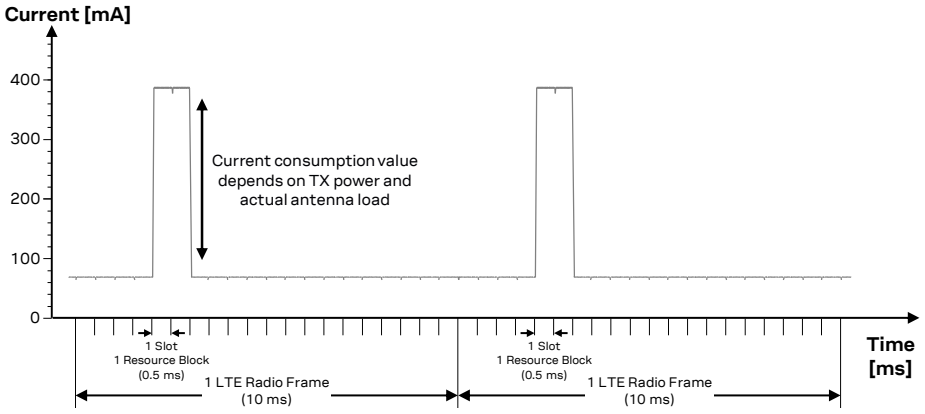

Figure 7: VCC current consumption profile versus time during LTE Cat M1 half-duplex connection

1.5.1.3 VCC consumption in deep-sleep mode

☞ The "00B" product versions of the SARA-R5 series modules do not support eDRX deep-sleep mode.

The low power mode and the PSM / eDRX configurations are by default disabled, but they can be enabled using the +UPSV and +CPSMS / +CEDRXS AT commands (see the SARA-R5 series AT commands manual [2]).

When low power mode and PSM / eDRX are enabled, whenever possible the modules automatically enter the PSM / eDRX deep-sleep mode (SARA-R500S and SARA-R510M8S modules) or the ultra-low power PSM / eDRX deep-sleep mode (SARA-R510S), reducing current consumption down to the lowest steady value: only the RTC runs with internal 32 kHz reference clock frequency. Detailed current consumption values can be found in the SARA-R5 series data sheet [1].

1.5.1.4 VCC consumption in low power idle mode

The low power mode configuration is by default disabled, but it can be enabled using the +UPSV AT command (see the SARA-R5 series AT commands manual [2]).

When low power mode is enabled, the module automatically enters the low power idle mode whenever possible, but it must periodically monitor the paging channel of the current base station (paging block reception), in accordance to the LTE system requirements, even if connected mode is not enabled by the application. When the module monitors the paging channel, it wakes up to the active mode to enable the reception of the paging block. In between, the module switches to low power mode. This is known as discontinuous reception (DRX) or extended discontinuous reception (eDRX).

Figure 8 illustrates an example of the module current consumption profile when low power mode configuration is enabled: the module is registered with the network, automatically enters the low power idle mode, and periodically wakes up to active mode to monitor the paging channel for the paging block reception in discontinuous reception (DRX) mode.

Detailed current consumption values can be found in the SARA-R5 series data sheet [1].

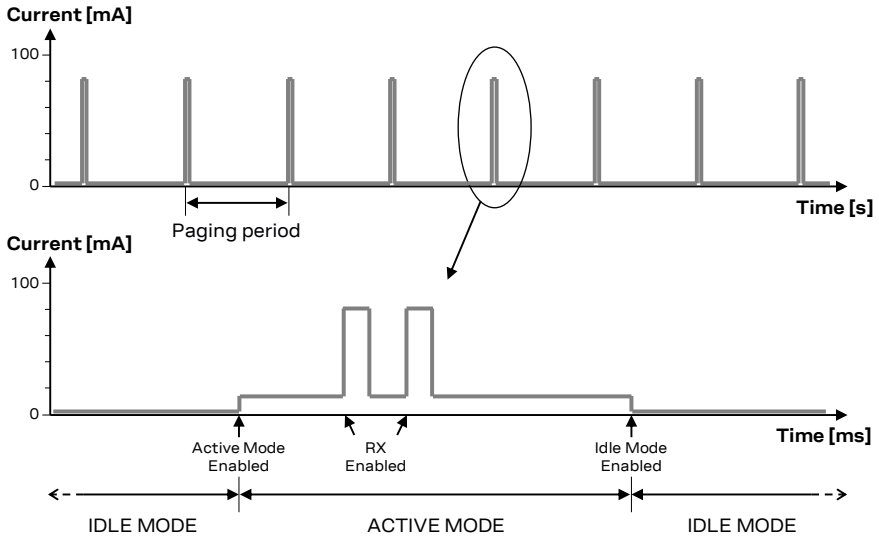

Figure 8: VCC current consumption profile with low power mode enabled and module registered with the network: the module is in low power idle mode and periodically wakes up to active mode to monitor the paging channel for paging block reception

1.5.1.5 VCC consumption in active mode

The active mode is the state where the module is switched on and ready to communicate with an external device by means of the application interfaces (as the UART serial interface). The module processor core is active and the 26 MHz reference clock frequency is used.

If low power mode configuration is disabled, as it is by default (see the SARA-R5 series AT commands manual [2], +UPSV AT commands for details), the module remains in active mode. Otherwise, if low power mode configuration is enabled, the module enters low power idle mode (and deep-sleep mode, if enabled) whenever possible.

Figure 9 shows a typical example of the module current consumption profile when the module is in active mode. Here, the module is registered with the network and, while active mode is maintained, the receiver is periodically activated to monitor the paging channel for paging block reception. Detailed current consumption values can be found in the SARA-R5 series data sheet [1].

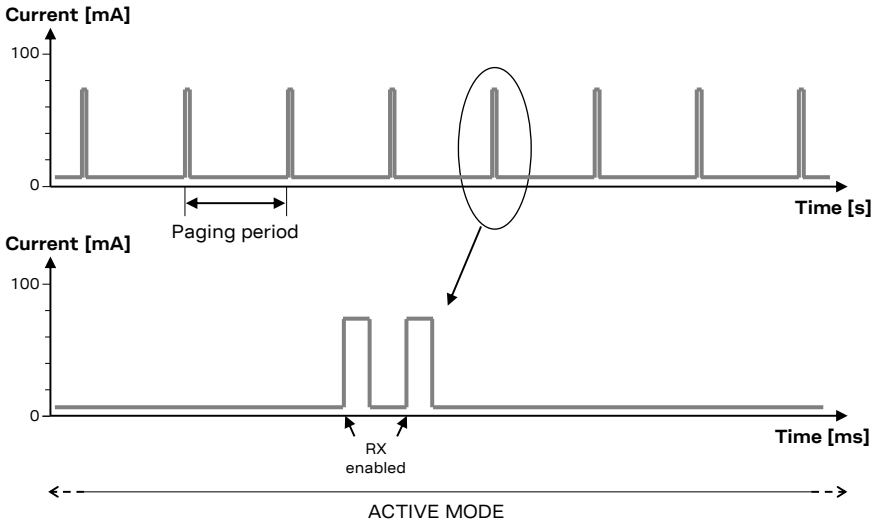

Figure 9: VCC current consumption profile with low power mode disabled and module registered with the network: active mode is always held and the receiver is periodically activated to monitor the paging channel for paging block reception

1.5.2 Generic digital interfaces supply output (V_INT)

The same voltage domain internally used as supply for the generic digital interfaces of SARA-R5 series modules is also available on the **V_INT** output pin, as illustrated in Figure 10.

The internal regulator that generates the **V_INT** supply output is a switching (DC-DC) converter, which is directly supplied from the **VCC** main supply input of the module.

The **V_INT** voltage regulator output of SARA-R5 series modules is disabled (i.e. 0 V) when the module is switched off, and it can be used to monitor the operating mode of the module as follows:

- When the module is off, or in deep-sleep mode, the voltage level is low (i.e. 0 V)
- When the module is on, outside deep-sleep mode, the voltage level is high (i.e. 1.8 V)

The current capability is specified in the SARA-R5 series data sheet [1]. The **V_INT** voltage domain can be used in place of an external discrete regulator as a reference voltage rail for external components.

The **V_INT** regulator output provides internal short circuit protection to limit the start-up current and protect the device in short circuit situations. No additional external short circuit protection is required.

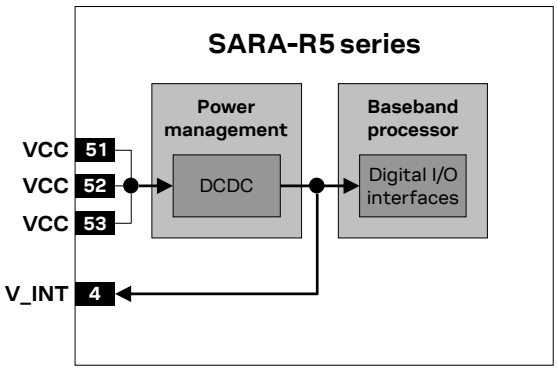

Figure 10: SARA-R5 series interfaces supply output (V_INT) simplified block diagram

1.6 System function interfaces

1.6.1 Module power-on

1.6.1.1 Switch-on events

When the SARA-R500S and SARA-R510M8S modules are in the not-powered mode (i.e. switched off, with the **VCC** module supply not applied), the switch-on routine can be triggered by:

- Applying a voltage at the **VCC** module supply input within the operating range (see SARA-R5 series data sheet [1]).

When the SARA-R510S modules are in the not-powered mode (i.e. switched off, with the **VCC** module supply not applied), the switch-on routine can be triggered by:

- Applying a voltage at the **VCC** module supply input within the operating range, and then forcing a low level at the **PWR_ON** input pin (normally high due to internal pull-up) for a valid time period (see SARA-R5 series data sheet [1]).

When the SARA-R5 series modules are in the power-off mode (i.e. switched off, but with a valid voltage present at the **VCC** module supply input) or in deep-sleep mode, they can be switched on or they can be woken up as following:

- Forcing a low level at the **PWR_ON** input pin (normally high due to internal pull-up) for a valid time period (see SARA-R5 series data sheet [1]).

As illustrated in Figure 11, the **PWR_ON** input pin is equipped with an internal pull-up resistor. Detailed electrical characteristics with voltages and timings are described in the SARA-R5 series data sheet [1].

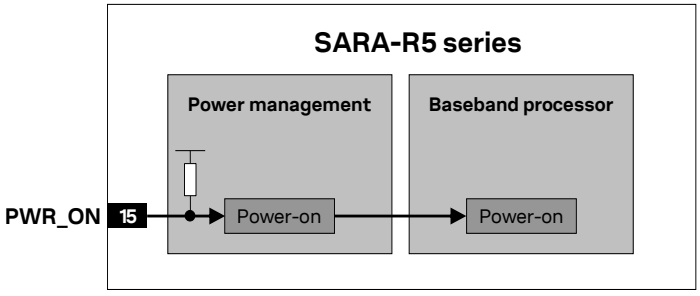

Figure 11: SARA-R5 series PWR_ON input equivalent circuit description

1.6.1.2 Switch-on sequence from not-powered mode

Figure 12 shows the SARA-R500S / SARA-R510M8S switch-on sequence from not-powered mode:

- The external power supply is applied to the **VCC** module pins, representing the start-up event.
- All the generic digital pins are tri-stated until the switch-on of their supply source (**V_INT**).
- The baseband core and all digital pins are held in reset state; then, any digital pin is set in the correct sequence from the reset state to the default operational configured state. The duration of this phase differs within generic digital interfaces and USB interface due to host / device enumeration timings.
- If enabled, a greeting message is sent on the **RXD** pin (for more details, see SARA-R5 series AT commands manual [2]).
- The module is fully ready to operate after all interfaces are configured.

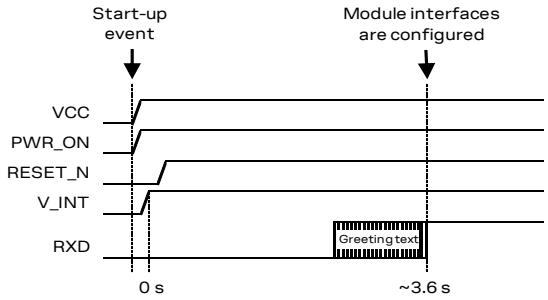

Figure 12: SARA-R500S / SARA-R510M8S switch-on sequence description from not-powered mode

Figure 13 shows the SARA-R510S modules switch-on sequence from the not-powered mode:

- The external power supply is applied to the **VCC** module pins.
- The **PWR_ON** pin is held low for a valid time period, representing the start-up event.
- All the generic digital pins are tri-stated until the switch-on of their supply source (**V_INT**).
- The baseband core and all digital pins are held in reset state; then, any digital pin is set in the correct sequence from the reset state to the default operational configured state. The duration of this phase differs within generic digital interfaces and USB interface due to host / device enumeration timings.
- If enabled, a greeting message is sent on the **RXD** pin (for more details, see SARA-R5 series AT commands manual [2]).
- The module is fully ready to operate after all interfaces are configured.

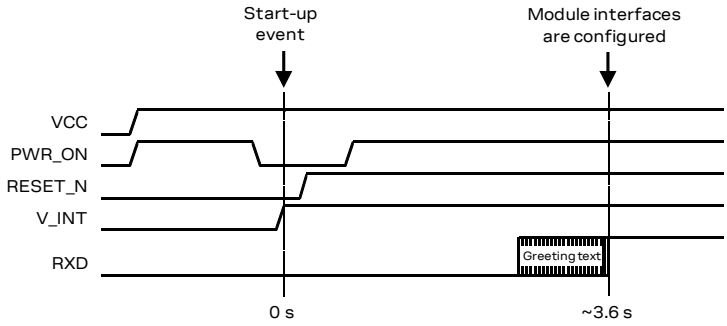

Figure 13: SARA-R510S switch-on sequence description from not-powered mode

1.6.1.3 Switch-on / wake-up sequence from power-off / deep-sleep mode

Figure 14 shows the SARA-R5 series modules switch-on or wake-up sequence from the power-off or deep-sleep mode:

- The external power supply is still applied to the VCC module pins, with the module being previously switched off (by means of the +CPWROFF AT command or by proper **PWR_ON** pin toggling), or with the module being previously entered deep-sleep mode.
- The **PWR_ON** pin is held low for a valid time period, representing the start-up event.
- All the generic digital pins are tri-stated until the switch-on of their supply source (**V_INT**).
- The baseband core and all digital pins are held in reset state; then, any digital pin is set in the correct sequence from the reset state to the default operational configured state. The duration of this phase differs within generic digital interfaces and USB interface due to host / device enumeration timings.
- If enabled, a greeting message is sent on the **RXD** pin (for more details, see SARA-R5 series AT commands manual [2]).
- The module is fully ready to operate after all interfaces are configured.

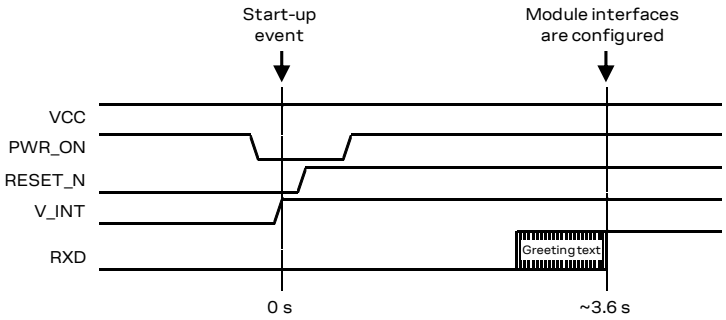

Figure 14: SARA-R5 series switch-on / wake-up sequence description from power-off / deep-sleep mode

1.6.1.4 General considerations for the switch-on procedure

If the greeting text is not used by the external application to detect that the module is ready to reply to AT commands, then the only way of checking it is polling: the external application can start sending "AT" after that the **CTS** line is set to the ON state (in case UART is used as AT interface with HW flow control enabled as default), but any AT command sent before the time when the module is ready to reply may be not buffered and may be lost.

☞ It is highly recommended to monitor:
- the **V_INT** pin, to sense the start of the SARA-R5 series module switch-on sequence
- the **GPIO** pin configured to provide the module status indication or module operating mode indication (see SARA-R5 series AT commands manual [2], +UGPIOC), to sense when the module is ready to operate

☞ No voltage driven by an external application should be applied to any generic digital interface of the module before the initialization of the interfaces has been finished, detectable by "greeting text" (if enabled) or by **CTS** line going low (if HW flow control is enabled as default).

☞ The duration of the SARA-R5 series modules' switch-on routine can vary depending on the application / network settings and the concurrent module activities: Figure 12, Figure 13 and Figure 14 illustrate indicative typical timings only.

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply once the boot of SARA-R5 series modules has been triggered.

1.6.2 Module power-off

1.6.2.1 Switch-off events

The proper graceful power-off of the SARA-R5 series modules, with storage of the current parameter settings in the non-volatile memory of the module and a clean network detach, can be triggered by:

- AT+CPWROFF command (see SARA-R5 series AT commands manual [2])

☞ The recommended method to properly switch off the SARA-R5 series modules is to use the +CPWROFF AT command.

A faster and safe power-off procedure of the modules, with storage of the current parameter settings in the module's non-volatile memory and without a clean network detach, can be triggered by:

- AT+CFUN=10 command (see SARA-R5 series AT commands manual [2])
- Toggling the GPIO input configured with the faster and safe power-off function (see section 1.12)

☞ The graceful switch-off procedure triggered by the +CPWROFF AT command is preferred to the faster power-off procedure triggered by the AT+CFUN=10 command or by toggling the configured GPIO pin. Frequent switching off without performing a clean network detach is not recommended.

An abrupt emergency hardware shutdown of the modules, without storage of the current parameter settings in the module's non-volatile memory and without clean network detach, can be executed by:

- Forcing a low pulse at the **PWR_ON** and **RESET_N** input pins, in the proper sequence described in the SARA-R5 series data sheet [1].

☞ It is recommended to avoid abrupt emergency hardware shutdowns during SARA-R5 series modules normal operations. An abrupt software reset, consisting in asserting the **RESET_N** input, is preferred, if considered necessary (see section 1.6.3).

An abrupt under-voltage shutdown occurs on SARA-R5 series modules when the **VCC** supply is removed. If this occurs, it is not possible to perform the storing of the current parameter settings in the module's non-volatile memory or to perform the proper network detach.

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply during SARA-R5 series modules normal operations. An abrupt software reset, consisting in asserting the **RESET_N** input, must be preferred, if considered necessary (see section 1.6.3).

☞ In case of applications where an abrupt power removal cannot be avoided, it is recommended to set the **RESET_N** input line at the low logic level as soon as the power failure in the supply source is detected, so that the under-voltage shutdown may be executed more safely since ~405 ms after the falling edge at the **RESET_N** input line.

An over-temperature or an under-temperature shutdown occurs on the SARA-R5 series modules when the temperature measured within the module reaches the dangerous area, if the optional "Smart temperature supervisor" feature is enabled and configured by dedicated +USTS AT command. For more details see SARA-R5 series data sheet [1] and SARA-R5 series AT commands manual [2].

If the "last gasp" feature is enabled, SARA-R5 series modules "01B" product versions automatically switch off after sending the last gasp, with storage of the current parameter settings in the module's internal non-volatile memory and without performing a clean network detach. (See the SARA-R5 series AT commands manual [2], +ULGASP AT command).

1.6.2.2 Switch-off sequence by +CPWROFF AT command

Figure 15 describes the switch-off sequence of the modules started by the +CPWROFF AT command, allowing storage of parameter settings in the non-volatile memory and a clean network detach:

- When the +CPWROFF AT command is sent the module starts the switch-off routine.
- Then the module replies OK on the AT interface: the switch-off routine is in progress.
- At the end of the switch-off routine, all the digital pins are tri-stated and all the internal voltage regulators are turned off, including the generic digital interfaces supply (**V_INT**).
- Then, the module remains in switch-off mode as long as a switch-on event does not occur (e.g. applying a low level to **PWR_ON**), or enters not-powered mode if the **VCC** supply is removed.

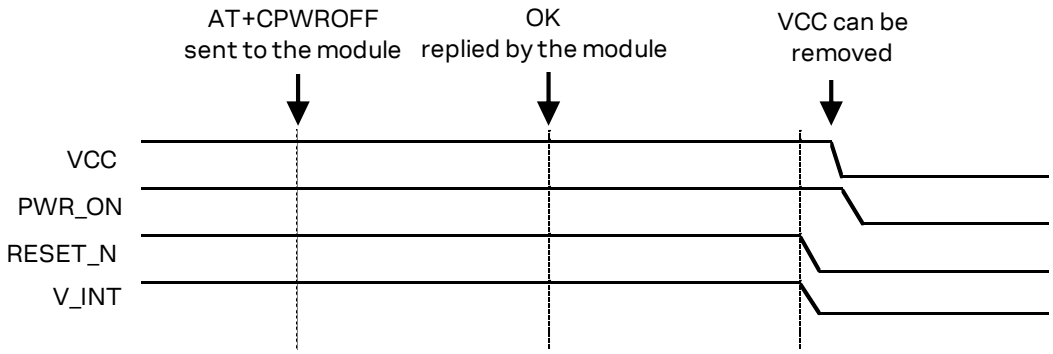

Figure 15: SARA-R5 series modules switch-off sequence by means of +CPWROFF AT command

☞ It is highly recommended to monitor the **V_INT** pin to sense the end of the switch-off sequence.

☞ The duration of each phase in the SARA-R5 series modules' switch-off routines can largely vary, depending on the application / network settings and the concurrent module activities.

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply before that the **V_INT** output of the modules goes low: **VCC** supply can be removed only after **V_INT** goes low.

☞ In case of applications where an abrupt power removal cannot be avoided, it is recommended to set the **RESET_N** input line at the low logic level as soon as the power failure in the supply source is detected, so that the under-voltage shutdown may be executed more safely since ~405 ms after the falling edge at the **RESET_N** input line.

1.6.3 Module reset

SARA-R5 series modules can be gracefully reset (re-booted), triggering the storage of the current parameter settings in the non-volatile memory of the module and performing a clean network detach procedure, by:

- AT+CFUN=16 command (see SARA-R5 series AT commands manual [2] for further details).

An abrupt software reset of the modules, without storage of the current parameter in the module's non-volatile memory and without proper network detach, can be triggered by:

- Forcing a low pulse on the **RESET_N** pin (normally high due to internal pull-up) for a valid time period (see the SARA-R5 series data sheet [1]).

☞ If considered necessary, an abrupt software reset must be preferred to an abrupt emergency hardware shutdown or an abrupt removal of the **VCC** supply.

☞ In case of applications where an abrupt power removal cannot be avoided, it is recommended to set the **RESET_N** input line at the low logic level as soon as the power failure in the supply source is detected, so that the under-voltage shutdown may be executed more safely since ~405 ms after the falling edge at the **RESET_N** input line.

As described in Figure 16, the **RESET_N** input pin is directly connected to the processor core, with an integrated active pull-up, in order to perform an abrupt software reset when asserted, excluding the power management unit. Detailed electrical characteristics with voltages and timings are described in the SARA-R5 series data sheet [1].

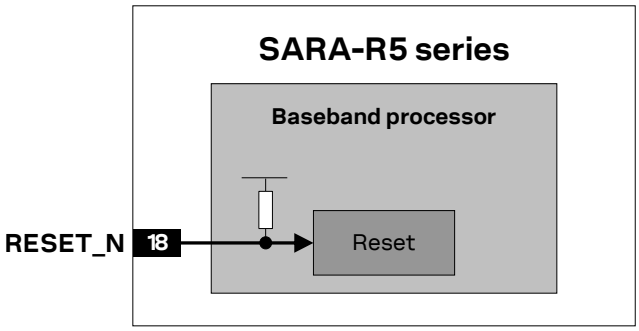

Figure 16: SARA-R5 series RESET_N input equivalent circuit description

1.7 Antenna interfaces

1.7.1 Cellular antenna RF interface (ANT)

SARA-R5 series modules provide an RF interface for connecting the external cellular antenna. The **ANT** pin represents the RF input/output for transmission and reception of LTE RF signals.

The **ANT** pin has a nominal characteristic impedance of 50 Ω and must be connected to the Tx / Rx cellular antenna through a 50 Ω transmission line to allow proper RF transmission and reception.

1.7.1.1 Cellular antenna RF interface requirements

Table 6 summarizes the requirements for the cellular antenna RF interface. See section 2.4.2 for suggestions to correctly design antennas circuits compliant with these requirements.

⚠ The antenna circuits affect the RF compliance of the device integrating SARA-R5 series modules with applicable required certification schemes (for more details see section 4). Compliance is guaranteed if the antenna RF interface requirements summarized in Table 6 are fulfilled.

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of the **ANT** port.
Frequency range	See the SARA-R5 series data sheet [1]	The required frequency range of the antenna connected to **ANT** port depends on the operating bands of the used cellular module and the used mobile network.
Return loss	S_{11} < -10 dB (VSWR < 2:1) recommended S_{11} < -6 dB (VSWR < 3:1) acceptable	The return loss or the S_{11}, as the VSWR, refers to the amount of reflected power, measuring how well the antenna RF connection matches the 50 Ω characteristic impedance of the **ANT** port. The impedance of the antenna termination must match as much as possible the 50 Ω nominal impedance of the **ANT** port over the operating frequency range, reducing as much as possible the amount of reflected power.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	The radiation efficiency is the ratio of the radiated power to the power delivered to antenna input: the efficiency is a measure of how well an antenna receives or transmits. The radiation efficiency of the antenna connected to the **ANT** port needs to be enough high over the operating frequency range to comply with the Over-The-Air (OTA) radiated performance requirements, as Total Radiated Power (TRP) and the Total Isotropic Sensitivity (TIS), specified by applicable related certification schemes.
Maximum gain	According to radiation exposure limits	The power gain of an antenna is the radiation efficiency multiplied by the directivity: the gain describes how much power is transmitted in the direction of peak radiation to that of an isotropic source. The maximum gain of the antenna connected to **ANT** port must not exceed the herein stated value to comply with regulatory agencies radiation exposure limits. For additional info see section 4.
Input power	> 24 dBm (> 0.25 W)	The antenna connected to the **ANT** port must support with adequate margin the maximum power transmitted by the modules.

Table 6: Summary of cellular antenna RF interface requirements

1.7.2 GNSS antenna RF interface (ANT_GNSS)

☞ The GNSS antenna RF interface is not supported by SARA-R500S and SARA-R510S modules.

☞ For additional information regarding the GNSS system, see the SARA-R5 / SARA-R4 positioning and timing implementation application note [18].

SARA-R510M8S modules provide an RF interface for connecting the external GNSS antenna. The **ANT_GNSS** pin represents the RF input reception of GNSS RF signals.

The **ANT_GNSS** pin has a nominal characteristic impedance of 50 Ω and must be connected to the Rx GNSS antenna through a 50 Ω transmission line to allow proper RF reception. As shown in Figure 4, the GNSS RF interface is designed with an internal DC block, and is suitable for both active and/or passive GNSS antennas due to the built-in SAW filter followed by an additional LNA in front of the integrated high performing u-blox M8 concurrent position engine.

1.7.2.1 GNSS antenna RF interface requirements

Table 7 summarizes the requirements for the GNSS antenna RF interface. See section 2.4.3 for suggestions to correctly design antennas circuits compliant with these requirements.

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of the **ANT_GNSS** port.
Frequency range	BeiDou 1561 MHz GPS / SBAS / QZSS / Galileo 1575 MHz GLONASS 1602 MHz	The required frequency range of the antenna connected to **ANT_GNSS** port depends on the selected GNSS constellations.
Return loss	S_{11} < -10 dB (VSWR < 2:1) recommended S_{11} < -6 dB (VSWR < 3:1) acceptable	The return loss or the S_{11}, as the VSWR, refers to the amount of reflected power, measuring how well the antenna RF connection matches the 50 Ω characteristic impedance of the **ANT_GNSS** port. The impedance of the antenna termination must match as much as possible the 50 Ω nominal impedance of the **ANT_GNSS** port over the operating frequency range, reducing as much as possible the amount of reflected power.
Gain (passive antenna)	> 4 dBic	The antenna gain defines how efficient the antenna is at receiving the signal. It is important providing good antenna visibility to the sky, using antennas with good radiation pattern in the sky direction, according to related antenna placement.
Gain (active antenna)	17 dB minimum, 30 dB maximum	The antenna gain defines how efficient the antenna is at receiving the signal. It is directly related to the overall C/No.
Noise figure (active antenna)	< 2 dB	Since GNSS signals are very weak, any amount of noise degrades all the sensitivity figures of the receiver: active antennas with LNA with a low noise figure are recommended.
Axial ratio	< 3 dB recommended	GNSS signals are circularly-polarized. The purity of the antenna circular polarization is stated in terms of axial ratio (AR), defined as the ratio of the vertical electric field to the horizontal electric field on polarization ellipse at zenith.

Table 7: Summary of GNSS antenna RF interface requirements

1.7.3 Cellular antenna detection interface (ANT_DET)

The antenna detection is based on ADC measurement. The **ANT_DET** pin is an analog to digital converter (ADC) provided to sense the antenna presence.

The antenna detection function provided by **ANT_DET** pin is an optional feature that can be implemented if the application requires it. The antenna detection is forced by the +UANTR AT command. See the SARA-R5 series AT commands manual [2] for more details on this feature.

The **ANT_DET** pin generates a DC current (for detailed characteristics see the SARA-R5 series data sheet [1]) and measures the resulting DC voltage, thus determining the resistance from the antenna connector provided on the application board to GND. So, the requirements to achieve antenna detection functionality are the following:

- an RF antenna assembly with a built-in resistor (diagnostic circuit) must be used
- an antenna detection circuit must be implemented on the application board

See section 2.4.5 for antenna detection circuit on application board and diagnostic circuit on antenna assembly design-in guidelines.

1.8 SIM interface

1.8.1 SIM card interface

SARA-R5 series modules provide on the **VSIM**, **SIM_IO**, **SIM_CLK** and **SIM_RST** pins a high-speed SIM/ME interface including automatic detection and configuration of the voltage required by the connected SIM card or chip.

Both 1.8 V and 3 V SIM types are supported. Activation and deactivation with automatic voltage switch from 1.8 V to 3 V are implemented, according to ISO-IEC 7816-3 specifications. The **VSIM** supply output provides internal short circuit protection to limit start-up current and protects the SIM to short circuits.

1.8.2 SIM card detection interface (GPIO5)

The **GPIO5** pin can be configured as an external interrupt to detect the SIM card mechanical / physical presence. The pin can be configured as input with an internal active pull-down enabled, and it can sense SIM card presence only if cleanly connected to the mechanical switch of a SIM card holder as described in section 2.5:

- Low logic level at **GPIO5** input pin is recognized as SIM card not present
- High logic level at **GPIO5** input pin is recognized as SIM card present

The SIM card detection function provided by **GPIO5** pin is an optional feature that can be implemented or not according to the application requirements. For more details about “SIM card detection” feature, see the SARA-R5 series AT commands manual [2], +UGPIOC, +CIND and +CMER AT commands.

If the “SIM card detection” feature is enabled in the application by the dedicated +UGPIOC AT command, then it is recommended to also enable the additional “SIM card hot insertion/removal” feature by the dedicated +UDCONF=50 AT command, in order to enable / disable the SIM interface upon detection of the external SIM card physical insertion / removal. For more details about the “SIM card hot insertion/removal” feature, see the u-blox AT commands manual [2], +UDCONF=50 AT command.

1.9 Data communication interfaces

SARA-R5 series modules provide the following serial communication interfaces:

- UART interfaces, available for communications with host application processor. See section 1.9.1.
- USB 2.0 compliant interface, available for diagnostic only. See section 1.9.2.
- SPI interfaces, available for communications with external SPI devices and for diagnostic. See section 1.9.3.
- SDIO interface, available for communications with external SDIO devices. See section 1.9.4.
- I2C interface, available for communications with external I2C devices. See section 1.9.5.

1.9.1 UART interfaces

1.9.1.1 UART features

SARA-R5 series modules include 1.8 V unbalanced asynchronous serial interfaces (UART) for communications with external host application processor.

UART can be configured by dedicated AT command (see the SARA-R5 series AT commands manual [2], +USIO AT command) in the following variants:

- **Variant 0** (default configuration), consisting in a single UART interface on **RXD**, **TXD**, **CTS**, **RTS**, **DTR**, **RI** pins, supporting:
  - AT commands
  - data communication
  - multiplexer protocol functionality (see 1.9.1.4)
  - FW update by means of FOAT
  - FW update by means of the u-blox EasyFlash tool (see the firmware update application note [21])

  The following lines are provided:
  - data lines (**RXD** as output, **TXD** as input)
  - hardware flow control lines (**CTS** as output, **RTS** as input)
  - modem status and control lines (**DTR** as input, **RI** as output)
- **Variant 1**, consisting in a single UART interface on **RXD**, **TXD**, **CTS**, **RTS**, **DTR**, **DSR**, **DCD**, **RI** pins, supporting:
  - AT commands
  - data communication
  - multiplexer protocol functionality (see 1.9.1.4)
  - FW update by means of FOAT
  - FW update by means of the u-blox EasyFlash tool (see the firmware update application note [21])

  The following lines are provided:
  - data lines (**RXD** as output, **TXD** as input)
  - hardware flow control lines (**CTS** as output, **RTS** as input)
  - modem status and control lines (**DTR** as input, **DSR** as output, **DCD** as output, **RI** as output)

- **Variants 2, 3 and 4**, consisting in two UART interfaces (first primary UART on **RXD**, **TXD**, **CTS**, **RTS** pins, and second auxiliary UART on **DCD**, **DTR**, **RI**, **DSR** pins) plus ring indication and DTR functions:
  - First primary UART interface supports:
    - AT commands
    - data communication
    - multiplexer protocol functionality (see 1.9.1.4)
    - FW update by means of FOAT
    - FW update by means of the u-blox EasyFlash tool (see the firmware update application note [21])

    The following lines are provided:
    - data lines (**RXD** as output, **TXD** as input)
    - hardware flow control lines (**CTS** as output, **RTS** as input)
  - Second auxiliary UART interface supports:
    - AT commands (variant 2 only)
    - data communication (variant 2 only)
    - FW update by means of FOAT (variant 2 only)
    - diagnostic trace log (variant 3 only)
    - GNSS tunneling (variant 4 only)

    The following lines are provided:
    - data lines (**DCD** as data output, **DTR** as data input)
    - hardware flow control lines (**RI** as flow control output, **DSR** as flow control input)
  - Ring indication function over the GPIO pin configured for this purpose (see section 1.12)

☞ When +USIO variant 4 is set, second auxiliary UART interface does not support flow control and status of its CTS line (**RI** pin) can be ignored.

UART general features, valid for all variants, are:

- Serial port with RS-232 functionality conforming to the ITU-T V.24 recommendation [5], with CMOS compatible levels (0 V for low data bit or ON state, and 1.8 V for high data bit or OFF state)
- Hardware flow control (default value) or none flow control are supported
- UART power saving indication available on the hardware flow control output, if hardware flow control is enabled: the line is driven to the OFF state when the module is not prepared to accept data by the UART interface
- One-shot autobauding is supported and it is enabled by default: automatic baud rate detection is performed only once, at module start up. After the detection, the module works at the fixed baud rate (the detected one) and the baud rate can be changed via AT command
- The default frame format is 8N1 (8 data bits, no parity, 1 stop bit)

SARA-R5 series modules are designed to operate as cellular modems, i.e. as the data circuit-terminating equipment (DCE) according to the ITU-T V.24 recommendation [5]. A host application processor connected to the module UART interface represents the data terminal equipment (DTE).

☞ UART signal names of the cellular modules conform to the ITU-T V.24 recommendation [5]: e.g. **TXD** line represents data transmitted by the DTE (host processor output) and received by the DCE (module input).

SARA-R5 series modules' UART interface is by default configured for AT commands: the module waits for AT command instructions and interprets all the characters received as commands to execute. All the functionalities supported by SARA-R5 series modules can be in general set and configured by AT commands:

- AT commands according to 3GPP TS 27.007 [6], 3GPP TS 27.005 [7], 3GPP TS 27.010 [8]
- u-blox AT commands (see the SARA-R5 series AT commands manual [2])

The UART interfaces settings can be suitably configured by AT commands (for more details, see the SARA-R5 series AT commands manual [2]).

Figure 17 describes the 8N1 frame format.

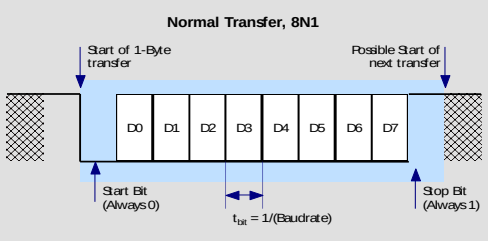

Figure 17: Description of UART default frame format (8N1 = 8 data bits, no parity, 1 stop bit), with fixed baud rate

1.9.1.2 UART signals behavior

At the end of the module boot sequence (see Figure 12, Figure 13, Figure 14), the module is by default in active mode, and the UART interface is initialized and enabled as AT commands interface.

The configuration and behavior of the UART signals after the boot sequence are described below:

- The module data output lines (**RXD** only if USIO variant 0 or 1 is set; **RXD** and **DCD** if USIO variant 2, 3 or 4 is set) are set by default to the OFF state (high level) at UART initialization. The module holds these lines in the OFF state until the module transmits some data.
- The module data input lines (**TXD** only if USIO variant 0 or 1 is set; **TXD** and **DTR** if USIO variant 2, 3 or 4 is set) are assumed to be controlled by the external host once UART is initialized. The data input lines have an internal active pull-up enabled.

1.9.1.3 UART and power saving

The power saving configuration is controlled by the AT+UPSV command (for the complete description, see the SARA-R5 series AT commands manual [2]). When power saving is enabled, the module automatically enters idle mode or deep-sleep mode whenever possible, and otherwise the active mode is maintained by the module (see section 1.4 for definition and description of module operating modes referred to in this section). The AT+UPSV command configures both the module power saving and the UART behavior in relation to the power saving.

Four different power saving configurations can be set by the AT+UPSV command:

- AT+UPSV=0, power saving disabled: module forced on active mode and UART interface enabled (default)
- AT+UPSV=1, power saving enabled: UART is cyclically enabled and module enters idle mode or deep-sleep mode automatically whenever possible
- AT+UPSV=2, power saving enabled and controlled by the UART **RTS** input line (not supported if HW flow control is enabled)
- AT+UPSV=3, power saving enabled and controlled by the UART **DTR** input line (not supported if +USIO variant 2, 3 or 4 is set)
- AT+UPSV=4, power saving enabled and behavior equal to AT+UPSV=1

The different power saving configurations that can be set by the +UPSV AT command are described in detail in the following subsections. Table 8 summarizes the UART interface communication process in the different power saving configurations, in relation with HW flow control settings and **RTS** and **DTR** input lines status. For more details on the +UPSV AT command description, see the SARA-R5 series AT commands manual [2].

AT+UPSV	HW flow control	RTS line	DTR line	Communication during idle mode and wake-up
0	Enabled (AT&K3)	ON	ON or OFF	Data sent by the DTE are correctly received by the module. Data sent by the module are correctly received by the DTE.
0	Enabled (AT&K3)	OFF	ON or OFF	Data sent by the DTE are correctly received by the module. Data sent by the module is buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. **RTS** line will be ON).
0	Disabled (AT&K0)	ON or OFF	ON or OFF	Data sent by the DTE are correctly received by the module. Data sent by the module are correctly received by the DTE if it is ready to receive data, otherwise data are lost.
1 or 4	Enabled (AT&K3)	ON	ON or OFF	Data sent by the DTE should be buffered by the DTE and will be correctly received by the module when active mode is entered. Data sent by the module are correctly received by the DTE.
1 or 4	Enabled (AT&K3)	OFF	ON or OFF	Data sent by the DTE should be buffered by the DTE and will be correctly received by the module when active mode is entered. Data sent by the module are buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. **RTS** line will be ON).
1 or 4	Disabled (AT&K0)	ON or OFF	ON or OFF	The first character sent by the DTE is lost, but after ~15 ms the UART and the module are waked up: recognition of subsequent characters is guaranteed after the complete UART / module wake-up. Data sent by the module are correctly received by the DTE if it is ready to receive data, otherwise data are lost.
2	Enabled (AT&K3)	ON or OFF	ON or OFF	Not applicable: HW flow control cannot be enabled with AT+UPSV=2.
2	Disabled (AT&K0)	ON	ON or OFF	Data sent by the DTE are correctly received by the module. Data sent by the module are correctly received by the DTE if it is ready to receive data, otherwise data are lost.
2	Disabled (AT&K0)	OFF	ON or OFF	Data sent by the DTE are lost. Data sent by the module are correctly received by the DTE if it is ready to receive data, otherwise data are lost.
3	Enabled (AT&K3)	ON	ON	Data sent by the DTE are correctly received by the module. Data sent by the module are correctly received by the DTE.
3	Enabled (AT&K3)	ON	OFF	Data sent by the DTE are lost. Data sent by the module are correctly received by the DTE.
3	Enabled (AT&K3)	OFF	ON	Data sent by the DTE are correctly received by the module. Data sent by the module are buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. **RTS** line will be ON).
3	Enabled (AT&K3)	OFF	OFF	Data sent by the DTE are lost. Data sent by the module are buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. **RTS** line will be ON).
3	Disabled (AT&K0)	ON or OFF	ON	Data sent by the DTE are correctly received by the module. Data sent by the module are correctly received by the DTE if it is ready to receive data, otherwise data are lost.
3	Disabled (AT&K0)	ON or OFF	OFF	Data sent by the DTE are lost. Data sent by the module are correctly received by the DTE if it is ready to receive data, otherwise data are lost.

Table 8: UART and power-saving summary

AT+UPSV=0: power saving disabled, fixed active mode

The module does not enter idle mode and the UART interface is enabled (data can be sent and received): the **CTS** line is always held in the ON state after UART initialization. This is the default configuration.

AT+UPSV=1 or AT+UPSV=4: power saving enabled

When the AT+UPSV=1 command is issued by the DTE, the UART is disabled after the timeout set by the second parameter of the +UPSV AT command (for more details, see the SARA-R5 series AT commands manual [2]).

Afterwards, the UART is periodically enabled to receive or send data and, if data has not been received or sent over the UART, the interface is automatically disabled whenever possible according to the timeout configured by the second parameter of the +UPSV AT command.

The module automatically enters the idle mode whenever possible but it wakes up to active mode according to the UART periodic wake-up so that the module cyclically enters the idle mode and the active mode. Additionally, the module wakes up to active mode according to any required activity related to the network or any other required activity related to the functions / interfaces of the module.

The module automatically enters the deep-sleep mode, according to the PSM / eDRX[7] settings, and according to the concurrent activities executed by the module (e.g. GNSS activities); when the module is in deep-sleep mode, UART is not functional.

The UART is enabled, and the module does not enter idle mode, in the following cases:

- During the periodic UART wake-up to receive or send data
- If the module needs to transmit some data over the UART (e.g. URC)
- During a PSD data call with external context activation
- If a character is sent by the DTE with HW flow control disabled, the first character sent causes the system wake-up due to the “wake-up via data reception” feature described in the following subsection, and the UART will be then kept enabled after the last data received according to the timeout set by the second parameter of the AT+UPSV=1 command

The module, when not in deep-sleep mode, periodically wakes up from idle mode to active mode to monitor the paging channel of the current base station (paging block reception), according to DRX and eDRX specifications, and according to +CEDRXS / +CEDRXRDP AT commands setting. The time period between two paging receptions is defined by the current base station (i.e. by the network); the eDRX parameters can be set by the module but are then negotiated with the current base station (i.e. by the network).

When the module is not registered with a network, the UART is enabled for ~30 ms, and then, if data has not been received or sent, the UART is disabled for ~31 s, and afterwards the interface is enabled again.

The module active mode duration depends on:

- Network parameters, related to the time interval for the paging block reception
- Duration of UART enable time in absence of data reception (~30 ms)
- The time period from the last data received at the serial port during the active mode: the module does not enter idle mode until a timeout expires. The second parameter of the +UPSV AT command configures this timeout (see the SARA-R5 series AT commands manual [2]).
  The active mode duration can be extended indefinitely since every subsequent character, received during the active mode, resets and restarts the timer.

[7] eDRX deep-sleep mode is not supported by “00B” product versions

The hardware flow control output (**CTS** line) indicates when the UART interface is enabled (data can be sent and received over the UART), if HW flow control is enabled, as illustrated in Figure 18.

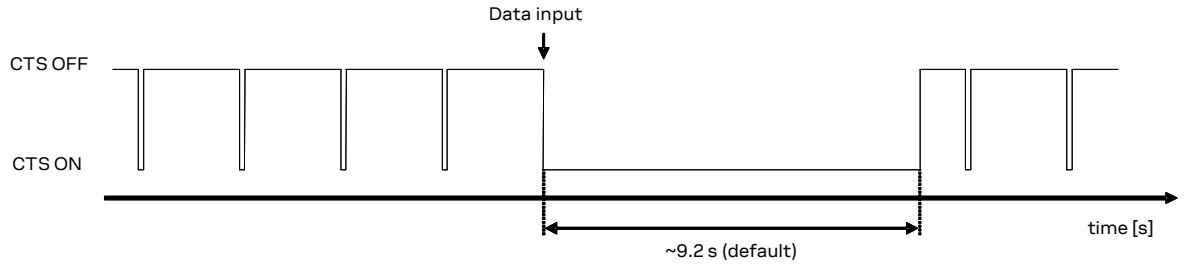

Figure 18: CTS behavior with power saving enabled (AT+UPSV=1) and HW flow control enabled: the CTS output line indicates when the UART interface of the module is enabled (CTS = ON = low level) or disabled (CTS = OFF = high level)

AT+UPSV=2: power saving enabled and controlled by the RTS line

☞ This configuration can only be enabled with the module hardware flow control disabled by AT&K0 command.

The UART interface is immediately disabled after the DTE sets the **RTS** line to OFF.

Then, the module automatically enters idle mode whenever possible according to any required activity related to the network or any other required activity related to the functions / interfaces of the module.

The module automatically enters the deep-sleep mode, according to the PSM / eDRX[8] settings, and according to the concurrent activities executed by the module (e.g. GNSS activities); when the module is in deep-sleep mode, UART is not functional.

The UART is disabled as long as the **RTS** line is held to OFF, but the UART is enabled in the following cases:

- If the module needs to transmit some data over the UART (e.g. URC)
- During a PSD data call with external context activation

When an OFF-to-ON transition occurs on the **RTS** input line, the UART is re-enabled and the module, if it was in idle mode, switches from idle to active mode after ~15 ms: this is the UART and module "wake-up time".

If the **RTS** line is set to ON by the DTE, then the module is not allowed to enter the idle mode or deep-sleep mode and the UART is kept enabled until the **RTS** line is set to OFF.

AT+UPSV=3: power saving enabled and controlled by the DTR line

☞ This configuration can only be enabled with the +USIO variant set to 0 or 1 (single UART interface).

The UART interface is immediately disabled after the DTE sets the **DTR** line to OFF.

Then, the module automatically enters idle mode whenever possible according to any required activity related to the network or any other required activity related to the functions / interfaces of the module.

The module automatically enters the deep-sleep mode, according to the PSM / eDRX[8] settings, and according to the concurrent activities executed by the module (e.g. GNSS activities); when the module is in deep-sleep mode, UART is not functional.

[8] eDRX deep-sleep mode is not supported by "00B" product versions

The UART is disabled as long as the **DTR** line is held to OFF, but the UART is enabled in case the module needs to transmit some data over the UART (e.g. URC).

When an OFF-to-ON transition occurs on the **DTR** input line, the UART is re-enabled and the module, if it was in idle mode, switches from idle to active mode after ~15 ms: this is the UART and module "wake-up time".

If the **DTR** line is set to ON by the DTE, then the module is not allowed to enter the idle mode or deep-sleep mode and the UART is kept enabled until the **DTR** line is set to OFF.

When the AT+UPSV=3 configuration is enabled, the **DTR** input line can still be used by the DTE to control the module behavior according to AT&D command configuration (see the SARA-R5 series AT commands manual [2]).

☞ The **CTS** output line indicates the UART power saving state as illustrated in Figure 18, if HW flow control is enabled with AT+UPSV=3.

Wake-up via data reception

The UART wake-up via data reception consists of a special configuration during idle mode of the module **TXD** input line that causes the system wake-up when an OFF-to-ON transition occurs on the **TXD** input line. In particular, the UART is enabled and the module switches from the idle mode to active mode within ~15 ms from the first character received: this is the system "wake-up time".

As a consequence, the first character sent by the DTE when the UART is disabled (i.e. the wake-up character) is not a valid communication character even if the wake-up via data reception configuration is active, because it cannot be recognized, and the recognition of the subsequent characters is guaranteed only after the complete system wake-up (i.e. after ~15 ms).

The UART wake-up via data reception configuration is active in the following case:

- AT+UPSV=1 or AT+UPSV=4 is set with hardware flow control disabled

The UART wake-up via data reception configuration is not active on the **TXD** input, and therefore all the data sent by the DTE is lost, in the following cases:

- AT+UPSV=2 is set and the **RTS** line is set OFF
- AT+UPSV=3 is set and the **DTR** line is set OFF

Figure 19 and Figure 20 show examples of common scenarios and timing constraints:

- AT+UPSV=1 power saving configuration is active and the timeout from last data received to idle mode start is set to 2000 GSM frames (AT+UPSV=1,2000)
- Hardware flow control is disabled

Figure 19 shows the case where the module UART is disabled and only a wake-up is forced. In this scenario the only character sent by the DTE is the wake-up character; as a consequence, the DCE module UART is disabled when the timeout from last data received expires (2000 GSM frames without data reception, as the default case).

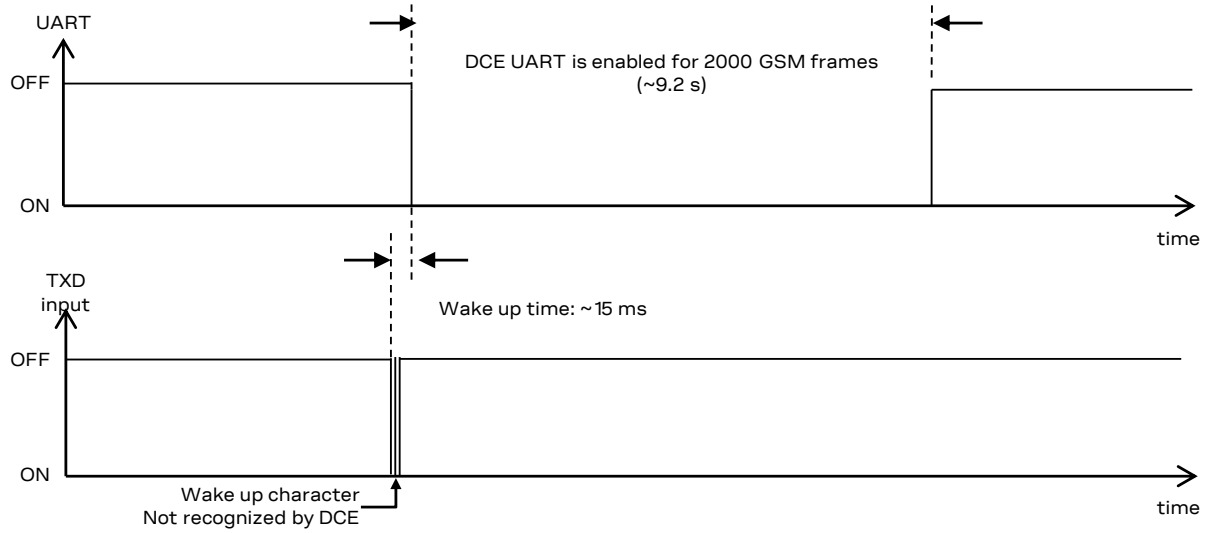

Figure 19: Wake-up via data reception without further communication

Figure 20 shows the case where in addition to the wake-up character further (valid) characters are sent. The wake-up character wakes up the module UART. The other characters must be sent after the “wake-up time” of ~15 ms. If this condition is satisfied, the module (DCE) recognizes characters. The module will disable the UART after 2000 GSM frames from the latest data reception.

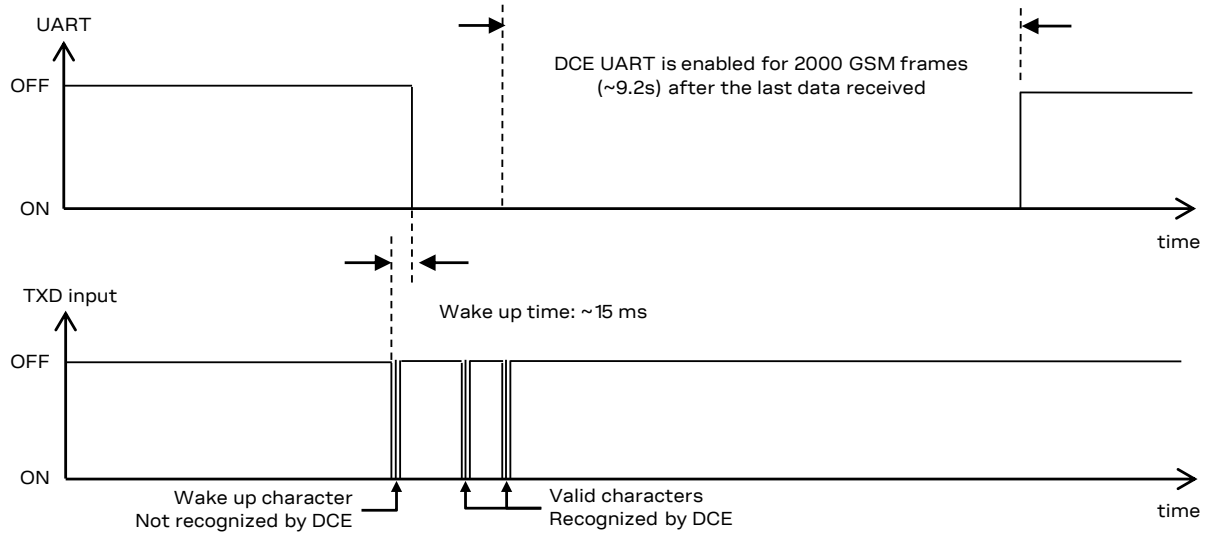

Figure 20: Wake-up via data reception with further communication

☞ The “wake-up via data reception” feature cannot be disabled.

1.9.1.4 UART multiplexer protocol

SARA-R5 series modules include multiplexer functionality as per 3GPP TS 27.010 [8], on the UART physical link. This is a data link protocol which uses HDLC-like framing and operates between the module (DCE) and the application processor (DTE) and allows a number of simultaneous sessions over the used physical link (UART).

When USIO variant 0 or 1 is set, the following virtual channels are defined:

- Channel 0: control channel
- Channel 1 – 3: AT commands / data communication
- Channel 4: GNSS tunneling

When USIO variant 2 is set, AT commands and data communication are available on second auxiliary UART, and the following virtual channels are defined on main primary UART:

- Channel 0: control channel
- Channel 1 – 2: AT commands / data communication
- Channel 3: GNSS tunneling

When USIO variant 3 is set, diagnostic trace log is available on second auxiliary UART, and the following virtual channels are defined on main primary UART:

- Channel 0: control channel
- Channel 1 – 3: AT commands / data communication
- Channel 4: GNSS tunneling

When USIO variant 4 is set, GNSS tunneling is available on second auxiliary UART, and the following virtual channels are defined on main primary UART:

- Channel 0: control channel
- Channel 1 – 3: AT commands / data communication

For more details, see the mux implementation application note [9].

1.9.2 USB interface

SARA-R5 series modules include a high-speed USB 2.0 compliant interface with a maximum 480 Mbit/s data rate according to the Universal Serial Bus Revision 2.0 specification [4]. The module itself acts as a USB device and can be connected to any USB host equipped with compatible drivers.

The USB interface is available for diagnostic purposes only.

The **USB_D+** / **USB_D-** lines carry the USB data / signaling, while the **VUSB_DET** input pin represents the input to enable the USB interface by applying an external valid USB VBUS voltage (5 V typical).

1.9.3 SPI interface

☞ The SPI interface is not supported by the “00B” and “01B” product versions of SARA-R5 series modules, except for diagnostic purposes.

SARA-R5 series modules include 1.8 V Serial Peripheral Interfaces available for communications with external SPI local devices, or for diagnostic purposes with the module acting as SPI host.

1.9.4 SDIO interface

☞ The SDIO interface is not supported by the “00B” and “01B” product versions of SARA-R5 series modules.

SARA-R5 series modules include a 1.8 V 4-bit Secure Digital Input Output interface over the **SDIO_D0**, **SDIO_D1**, **SDIO_D2**, **SDIO_D3**, **SDIO_CLK** and **SDIO_CMD** pins, with the module acting as an SDIO host, available for communications with compatible external SDIO devices, and for diagnostic purposes.

1.9.5 I2C interface

☞ Communication with an external GNSS receiver is not supported by SARA-R510M8S modules.

SARA-R5 series modules include a 1.8 V I2C-bus compatible interface over the **SDA** and **SCL** pins, available to communicate with an external u-blox GNSS receiver and with external I2C devices as for example an audio codec: the SARA-R5 series module acts as an I2C host that can communicate with I2C local devices in accordance with the I2C bus specifications [10].

The same 1.8 V I2C-bus compatible interface is internally connected to the u-blox M8 GNSS chipset integrated in SARA-R510M8S modules, as illustrated in Figure 4.

The **SDA** and **SCL** pins have internal active pull-up, so there is no need of additional pull-up resistors on the external application board.

1.10 Audio

☞ Audio is not supported by “00B” and “01B” product versions of SARA-R5 series modules.

SARA-R5 series modules include a 1.8 V I2S digital audio interface over the **I2S_TXD**, **I2S_RXD**, **I2S_CLK** and **I2S_WA** pins for transferring digital audio data with an external compatible digital audio device.

1.11 ADC

☞ ADC is not supported by “00B” product versions of SARA-R5 series modules.

SARA-R5 series modules include an Analog-to-Digital Converter input pin, **ADC**, configurable via a dedicated AT command (for further details, see the SARA-R5 series AT commands manual [2]).

1.12 General purpose input / output (GPIO)

SARA-R5 series modules include pins which can be configured as general purpose input/output or to provide custom functions via u-blox AT commands (for more details see the SARA-R5 series AT commands manual [2], +UGPIOC, +UGPIOR, +UGPIOW, +UTEST AT commands), as summarized in Table 9.

Function	Description	Default GPIO	Configurable GPIOs
General purpose output	Output to set the high or the low digital level	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6
General purpose input	Input to sense high or low digital level	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6
Network status indication	Output indicating cellular network status: registered, data transmission, no service	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6
External GNSS supply enable [9]	Output to enable/disable the supply of an external u-blox GNSS receiver connected to the cellular module by the I2C interface	-	GPIO2 [9]
External GNSS data ready [9]	Input to sense when an external u-blox GNSS receiver connected to the module is ready for sending data over the I2C interface	-	GPIO3 [9]
SIM card detection	Input for SIM card physical presence detection, to optionally enable / disable SIM interface upon detection of external SIM card physical insertion / removal	-	GPIO5
Module status indication	Output indicating module status: power-off or deep-sleep mode versus idle, active or connected mode	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6
Module operating mode indication	Output indicating module operating mode: power-off, deep-sleep or idle mode versus active or connected mode	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6
Ring indicator	Output providing events indicator	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6
Last gasp	Input to trigger last gasp notification	-	GPIO1, GPIO2, GPIO3[10], GPIO4, GPIO6
Time pulse output	Output providing accurate time reference, as a sequence with configurable[11] PPS or as single time pulse, based on the GNSS system or the LTE system (CellTime™)	-	GPIO6
Time stamp of external interrupt input	Input triggering via interrupt the generation of an URC time stamp over AT serial interface	-	EXT_INT
Faster and safe power-off	Input to trigger a faster and safe shutdown of the module (as triggered by AT+CFUN=10 command)	-	GPIO1, GPIO2, GPIO3[10], GPIO4, GPIO6
External GNSS time pulse [9]	Input to receive an accurate time reference, as a sequence with configurable[11] PPS from an external GNSS system	-	SDIO_CMD [9]
External GNSS time stamp of external interrupt [9]	Output triggering via interrupt the generation of an URC time stamp from an external GNSS system	-	GPIO4 [9]
Pin disabled	Tri-state with an internal active pull-down enabled	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, EXT_INT, SDIO_CMD	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, EXT_INT, SDIO_CMD
Antenna dynamic tuning	Output for real time control of an antenna tuning IC according to the LTE band used by the module	-	I2S_TXD, I2S_WA

Table 9: SARA-R5 series modules GPIO custom functions configuration

[9] SARA-R500S and SARA-R510S modules only
[10] SARA-R500S, SARA-R510S and SARA-R510M8S-00B modules only
[11] Configurability is not supported by “00B” product versions; the sequence is fixed to 1 PPS

1.13 GNSS peripheral output

☞ The GNSS peripheral output pins are not supported by the SARA-R500S, SARA-R510S, and SARA-R510M8S-00B product versions.

☞ For additional information regarding the GNSS system, see the SARA-R5 / SARA-R4 positioning and timing implementation application note [18].

SARA-R510M8S modules provide the following 1.8 V peripheral output pins directly connected to the internal u-blox M8 GNSS chipset (as is illustrated in Figure 3):

- The ANT_ON output pin, over the **I2S_RXD** pin, can provide optional control for switching off power to an external active GNSS antenna or an external separate LNA. This facility is provided to help minimize power consumption in power save mode operation.
- The GEOFENCE output pin, over the **I2S_CLK** pin, can provide optional indication of the geofencing status and can be used, for example, to wake up a host on activation.

1.14 Reserved pin (RSVD)

SARA-R5 series modules have a pin reserved for future use, marked as **RSVD**. This pin is to be left unconnected on the application board.

2 Design-in

2.1 Overview

For an optimal integration of the SARA-R5 series modules in the final application board, follow the design guidelines stated in this section.

Every application circuit must be suitably designed to guarantee the correct functionality of the relative interface, but a number of points require particular attention during the design of the application device.

The following list provides a rank of importance in the application design, starting from the highest relevance:

1. Module antennas connection: **ANT**, **ANT_GNSS** [12] and **ANT_DET** pins.
   Antenna circuit directly affects the RF compliance of the device integrating a SARA-R5 series module with applicable certification schemes. Follow the suggestions provided in the relative section 2.4 for schematic and layout design.

2. Module supply: **VCC** and **GND** pins.
   The supply circuit affects the RF compliance of the device integrating a SARA-R5 series module with the applicable required certification schemes as well as the antenna circuits design. Very carefully follow the suggestions provided in the relative section 2.2.1 for schematic and layout design.

3. SIM interface: **VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST** pins.
   Accurate design is required to guarantee SIM card functionality reducing the risk of RF coupling. Carefully follow the suggestions provided in relative section 2.5 for schematic and layout design.

4. System functions: **PWR_ON** and **RESET_N** pins.
   Accurate design is required to guarantee that the voltage level is well defined during operation. Carefully follow the suggestions provided in relative section 2.3 for schematic and layout design.

5. Other digital interfaces: UART, USB, SPI, SDIO, I2C, I2S, ADC, GPIOs and GNSS PIOs.
   Accurate design is required to guarantee correct functionality and reduce the risk of digital data frequency harmonics coupling. Follow the suggestions provided in sections 2.6, 2.7, 2.8, 2.9 and 2.10 for schematic and layout design.

6. Other supplies: **V_INT** generic digital interfaces supply.
   Accurate design is required to guarantee correct functionality. Follow the suggestions provided in the corresponding section 2.2.2 for schematic and layout design.

☞ It is recommended to follow the specific design guidelines provided by each manufacturer of any external part selected for the application board integrating the u-blox cellular modules.

[12] Not supported by SARA-R500S and SARA-R510S modules

2.2 Supply interfaces

2.2.1 Module supply (VCC)

2.2.1.1 General guidelines for VCC supply circuit selection and design

All the available **VCC** pins have to be connected to the external supply minimizing the power loss due to series resistance.

GND pins are internally connected. Application design shall connect all the available pads to solid ground on the application board, since a good (low impedance) connection to external ground can minimize power loss and improve RF and thermal performance.

SARA-R5 series modules must be sourced through the **VCC** pins with a suitable DC power supply that should comply with the module **VCC** requirements summarized in Table 5.

The appropriate DC power supply can be selected according to the application requirements (see Figure 21) between the different possible supply sources types, which most common ones are the following:

- Switching regulator
- Low Drop-Out (LDO) linear regulator
- Rechargeable Lithium-ion (Li-Ion) or Lithium-ion polymer (Li-Pol) battery
- Primary (disposable) battery

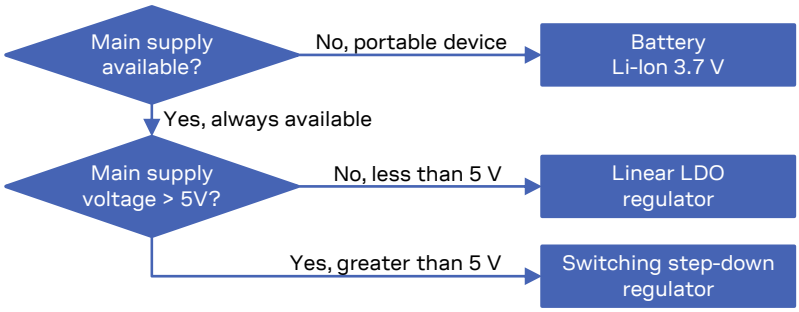

Figure 21: VCC supply concept selection

The switching step-down regulator is the typical choice when primary supply source has a nominal voltage much higher (e.g. greater than 5 V) than the operating supply voltage of SARA-R5 series. The use of switching step-down provides the best power efficiency for the overall application and minimizes current drawn from the main supply source. See section 2.2.1.2 for design-in.

The use of an LDO linear regulator becomes convenient for a primary supply with a relatively low voltage (e.g. less or equal than 5 V). In this case, the typical 90% efficiency of the switching regulator diminishes the benefit of voltage step-down and no true advantage is gained in input current savings. On the opposite side, linear regulators are not recommended for high voltage step-down as they dissipate a considerable amount of energy in thermal power. See section 2.2.1.3 for design-in.

If SARA-R5 series modules are deployed in a mobile unit where no permanent primary supply source is available, then a battery will be required to provide **VCC**. A standard 3-cell Li-Ion or Li-Pol battery pack directly connected to **VCC** is the usual choice for battery-powered devices. During charging, batteries with Ni-MH chemistry typically reach a maximum voltage that is above the maximum rating for **VCC**, and should therefore be avoided. See sections 2.2.1.4, 2.2.1.5, 2.2.1.6 and 2.2.1.7 for specific design-in.

Keep in mind that the use of rechargeable batteries requires the implementation of a suitable charger circuit, which is not included in the modules. The charger circuit needs to be designed to prevent over-voltage on **VCC** pins, and it should be selected according to the application requirements. A DC-DC switching charger is the typical choice when the charging source has a high nominal voltage (e.g. ~12 V), whereas a linear charger is the typical choice when the charging source has a relatively low nominal voltage (~5 V). If both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time as possible supply source, then a suitable charger / regulator with integrated power path management function can be selected to supply the module while simultaneously and independently charging the battery. See sections 2.2.1.6 and 2.2.1.7 for specific design-in.

An appropriate primary (not rechargeable) battery can be selected taking into account the maximum current specified in the SARA-R5 series data sheet [1] during connected mode, considering that primary cells might have weak power capability. See section 2.2.1.5 for specific design-in.

The usage of more than one DC supply at the same time should be carefully evaluated: depending on the supply source characteristics, different DC supply systems can result as mutually exclusive.

The selected regulator or battery must be able to support with adequate margin the highest averaged current consumption value specified in the SARA-R5 series data sheet [1].

The following sections highlight some design aspects for each of the supplies listed above providing application circuit design-in compliant with the module **VCC** requirements summarized in Table 5.

2.2.1.2 Guidelines for VCC supply circuit design using a switching regulator

The use of a switching regulator is suggested when the difference from the available supply rail source to the **VCC** value is high, since switching regulators provide good efficiency transforming a 12 V or greater voltage supply to the typical 3.8 V value of the **VCC** supply.

The characteristics of the switching regulator connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 5:

- **Power capability**: the switching regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering to **VCC** pins the maximum current consumption occurring during transmissions at the maximum power, as specified in the SARA-R5 series data sheet [1].
- **Low output ripple**: the switching regulator together with its output circuit must be capable of providing a clean (low noise) **VCC** voltage profile.
- **PWM mode operation**: it is preferable to select regulators with Pulse Width Modulation (PWM) mode. While in connected mode, the Pulse Frequency Modulation (PFM) mode and PFM/PWM modes transitions must be avoided to reduce noise on **VCC** voltage profile. Switching regulators can be used that are able to switch between low ripple PWM mode and high ripple PFM mode, provided that the mode transition occurs when the module changes status from the active mode to connected mode. It is permissible to use a regulator that switches from the PWM mode to the burst or PFM mode at an appropriate current threshold.

Figure 22 and the components listed in Table 10 show an example of a power supply circuit for SARA-R5 series modules. In this example, the module **VCC** is supplied by a step-down switching regulator capable of delivering the maximum peak / pulse current specified for the LTE use-case, with low output ripple and with fixed switching frequency in PWM mode operation greater than 1 MHz.

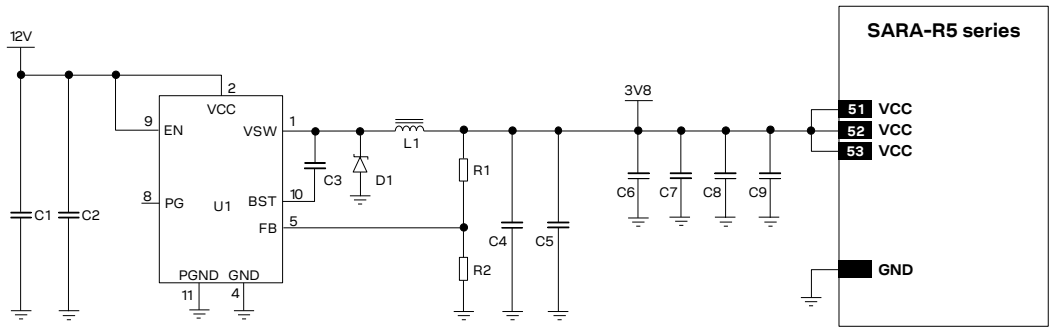

Figure 22: Example of VCC supply circuit for SARA-R5 series modules, using a step-down regulator

Reference	Description	Part number – Manufacturer
C1	10 µF capacitor ceramic X7R 50 V	Generic manufacturer
C2	10 nF capacitor ceramic X7R 16 V	Generic manufacturer
C3	22 nF capacitor ceramic X7R 16 V	Generic manufacturer
C4	22 µF capacitor ceramic X5R 25 V	Generic manufacturer
C5	22 µF capacitor ceramic X5R 25 V	Generic manufacturer
C6	100 nF capacitor ceramic X7R 16 V	GCM155R71C104KA55 – Murata
C7	10 nF capacitor ceramic X7R 16 V	GRT155R71C103KE01 – Murata
C8	68 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1E680JA01 – Murata
C9	15 pF capacitor ceramic C0G 0402 5% 50 V	GJM1555C1H150JB01 – Murata
D1	Schottky diode 30 V 2 A	MBR230LSFT1G – ON Semiconductor
L1	4.7 µH inductor 20% 2 A	SLF7045T-4R7M2R0-PF – TDK
R1	470 kΩ resistor 0.1 W	Generic manufacturer
R2	150 kΩ resistor 0.1 W	Generic manufacturer
U1	Step-down regulator 1 A 1 MHz	TS30041 – Semtech

Table 10: Components for the VCC supply circuit for SARA-R5 series modules, using a step-down regulator

☞ See the section 2.2.1.9, and in particular Figure 28 / Table 15, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.3 Guidelines for VCC supply circuit design using linear regulator

The use of a linear regulator is suggested when the difference from the available supply rail source and the **VCC** value is low: linear regulators provide high efficiency when transforming a 5 V supply to a voltage value within the module **VCC** normal operating range.

The characteristics of the Low Drop-Out (LDO) linear regulator connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 5:

- **Power capabilities**: the LDO linear regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering to **VCC** pins the maximum current consumption occurring during a transmission at the maximum Tx power, as specified in the SARA-R5 series data sheet [1].
- **Power dissipation**: the power handling capability of the LDO linear regulator must be checked to limit its junction temperature to the rated range (i.e. check the voltage drop from the maximum input voltage to the minimum output voltage to evaluate the power dissipation of the regulator).

Figure 23 and the components listed in Table 11 show an example of a power supply circuit for SARA-R5 series modules, where the module **VCC** is supplied by an LDO linear regulator capable of delivering maximum peak / pulse current specified for LTE use-case, with suitable power handling capability.

It is recommended to configure the LDO linear regulator to generate a voltage supply value slightly below the maximum limit of the module **VCC** normal operating range (e.g. ~4.1 V for the **VCC**, as in the circuits described in Figure 23 and Table 11). This reduces the power on the linear regulator and improves the thermal design of the circuit.

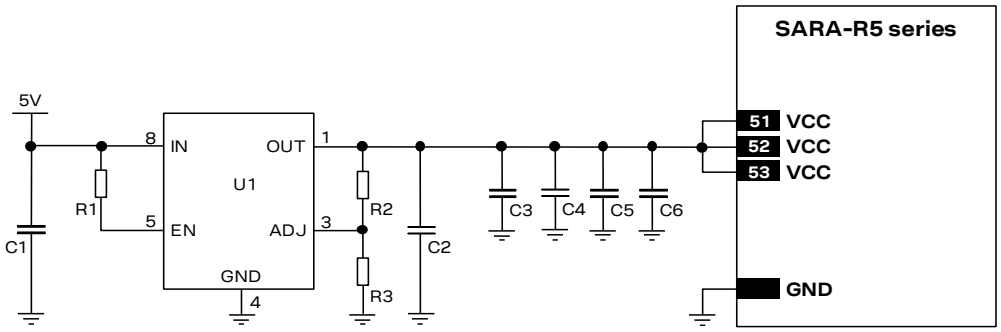

Figure 23: Example of VCC supply circuit for SARA-R5 series modules, using an LDO linear regulator

Reference	Description	Part number – Manufacturer
C1	1 µF capacitor ceramic X5R 6.3 V	Generic manufacturer
C2	22 µF capacitor ceramic X5R 25 V	Generic manufacturer
C3	100 nF capacitor ceramic X7R 16 V	GCM155R71C104KA55 – Murata
C4	10 nF capacitor ceramic X7R 16 V	GRT155R71C103KE01 – Murata
C5	68 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1E680JA01 – Murata
C6	15 pF capacitor ceramic C0G 0402 5% 50 V	GJM1555C1H150JB01 – Murata
R1	47 kΩ resistor 0.1 W	Generic manufacturer
R2	41 kΩ resistor 0.1 W	Generic manufacturer
R3	10 kΩ resistor 0.1 W	Generic manufacturer
U1	LDO linear regulator 1.0 A	AP7361C – Diodes Incorporated

Table 11: Components for VCC supply circuit for SARA-R5 series modules, using an LDO linear regulator

☞ See the section 2.2.1.9, and in particular Figure 28 / Table 15, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.4 Guidelines for VCC supply circuit design using a rechargeable battery

Rechargeable Li-Ion or Li-Pol batteries connected to the **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 5:

- **Maximum pulse and DC discharge current**: the rechargeable Li-Ion battery with its related output circuit connected to the **VCC** pins must be capable of delivering the maximum current occurring during a transmission at maximum Tx power, as specified in SARA-R5 series data sheet [1]. The maximum discharge current is not always reported in the data sheets of batteries, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- **DC series resistance**: the rechargeable Li-Ion battery with its output circuit must be capable of avoiding a VCC voltage drop below the operating range summarized in Table 5 during transmission.

2.2.1.5 Guidelines for VCC supply circuit design using a primary battery

The characteristics of a primary (non-rechargeable) battery connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 5:

- **Maximum pulse and DC discharge current**: the non-rechargeable battery with its related output circuit connected to the **VCC** pins must be capable of delivering the maximum current consumption occurring during a transmission at maximum Tx power, as specified in SARA-R5 series data sheet [1]. The maximum discharge current is not always reported in the data sheets of batteries, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- **DC series resistance**: the non-rechargeable battery with its output circuit must be capable of avoiding a VCC voltage drop below the operating range summarized in Table 5 during transmission.

2.2.1.6 Guidelines for external battery charging circuit

SARA-R5 series modules do not have an on-board charging circuit. Figure 24 provides an example of a battery charger design, suitable for applications that are Li-Ion (or Li-Pol) battery powered.

In the application circuit, a rechargeable Li-Ion (or Li-Pol) battery cell, that features the correct pulse and DC discharge current capabilities and the appropriate DC series resistance, is directly connected to the **VCC** supply input of the module. Battery charging is completely managed by the battery charger IC, which from a USB power source (5.0 V typ.), linearly charges the battery in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current.
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor.
- **Constant voltage**: when the battery voltage reaches the regulated output voltage, the battery charger IC starts to reduce the current until the charge termination is done. The charging process ends when the charging current reaches the value configured by an external resistor or when the charging timer reaches the factory set value.

Using a battery pack with an internal NTC resistor, the battery charger IC can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

The battery charger IC, as linear charger, is more suitable for applications where the charging source has a relatively low nominal voltage (~5 V), so that a switching charger is suggested for applications where the charging source has a relatively high nominal voltage (e.g. ~12 V, see section 2.2.1.7 for the specific design-in).

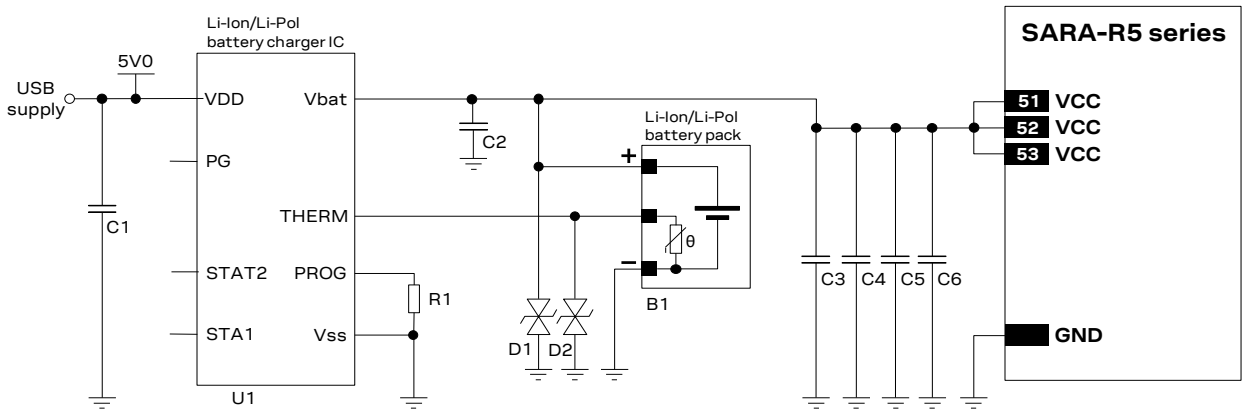

Figure 24: Li-Ion (or Li-Pol) battery charging application circuit

Reference	Description	Part number – Manufacturer
B1	Li-Ion (or Li-Pol) battery pack with 470 Ω NTC	Generic manufacturer
C1, C2	1 µF capacitor ceramic X7R 16 V	Generic manufacturer
C3	15 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H150JB01 – Murata
C4	68 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H680JA16 – Murata
C5	10 nF capacitor ceramic X7R 0402 10% 16 V	GRT155R71C103KE01 – Murata
C6	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
D1, D2	Low capacitance ESD protection	CG0402MLE-18G – Bourns
R1	10 kΩ resistor 0.1 W	Generic manufacturer
U1	Single cell Li-Ion (or Li-Pol) battery charger IC	MCP73833 – Microchip

Table 12: Suggested components for the Li-Ion (or Li-Pol) battery charging application circuit

☞ See the section 2.2.1.9, and in particular Figure 28 / Table 15, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.7 Guidelines for external charging and power path management circuit

Application devices where both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time as a possible supply source, should implement a suitable charger / regulator with integrated power path management function to supply the module and the whole device while simultaneously and independently charging the battery.

Figure 25 reports a simplified block diagram circuit showing the working principle of a charger / regulator with integrated power path management function. This component allows the system to be powered by a permanent primary supply source (e.g. ~12 V) using the integrated regulator, which simultaneously and independently recharges the battery (e.g. 3.7 V Li-Pol) that represents the back-up supply source of the system. The power path management feature permits the battery to supplement the system current requirements when the primary supply source is not available or cannot deliver the peak system currents.

A power management IC should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 5:

- High efficiency internal step-down converter, with characteristics as indicated in section 2.2.1.2
- Low internal resistance in the active path Vout – Vbat, typically lower than 50 mΩ
- High efficiency switch mode charger with separate power path control

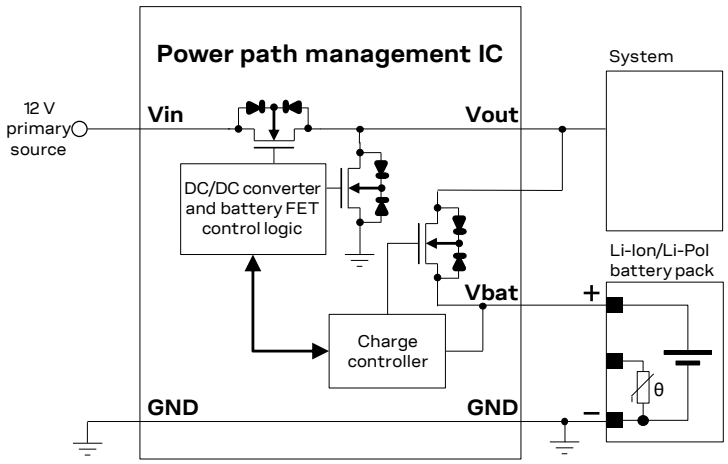

Figure 25: Charger / regulator with integrated power path management circuit block diagram

Figure 26 and the parts listed in Table 13 provide an application circuit example where the MPS MP2617H switching charger / regulator with integrated power path management function provides the supply to the cellular module. At the same time it also concurrently and autonomously charges a suitable Li-Ion (or Li-Pol) battery with the correct pulse and DC discharge current capabilities and the appropriate DC series resistance according to the rechargeable battery recommendations described in section 2.2.1.4.

The MP2617H IC constantly monitors the battery voltage and selects whether to use the external main primary supply / charging source or the battery as supply source for the module, and starts a charging phase accordingly.

The MP2617H IC normally provides a supply voltage to the module regulated from the external main primary source allowing immediate system operation even under missing or deeply discharged battery: the integrated switching step-down regulator is capable to provide up to 3 A output current with low output ripple and fixed 1.6 MHz switching frequency in PWM mode operation. The module load is satisfied in priority, then the integrated switching charger will take the remaining current to charge the battery.

Additionally, the power path control allows an internal connection from battery to the module with a low series internal ON resistance (40 mΩ typical), in order to supplement additional power to the module when the current demand increases over the external main primary source or when this external source is removed.

Battery charging is managed in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current, set to 10% of the fast-charge current
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor to a value suitable for the application
- **Constant voltage**: when the battery voltage reaches the regulated output voltage (4.2 V), the current is progressively reduced until the charge termination is done. The charging process ends when the charging current reaches the 10% of the fast-charge current or when the charging timer reaches the value configured by an external capacitor

Using a battery pack with an internal NTC resistor, the MP2617H can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

Several parameters as the charging current, the charging timings, the input current limit, the input voltage limit, the system output voltage can be easily set according to the specific application requirements, as the actual electrical characteristics of the battery and the external supply / charging source: suitable resistors or capacitors must be accordingly connected to the related pins of the IC.

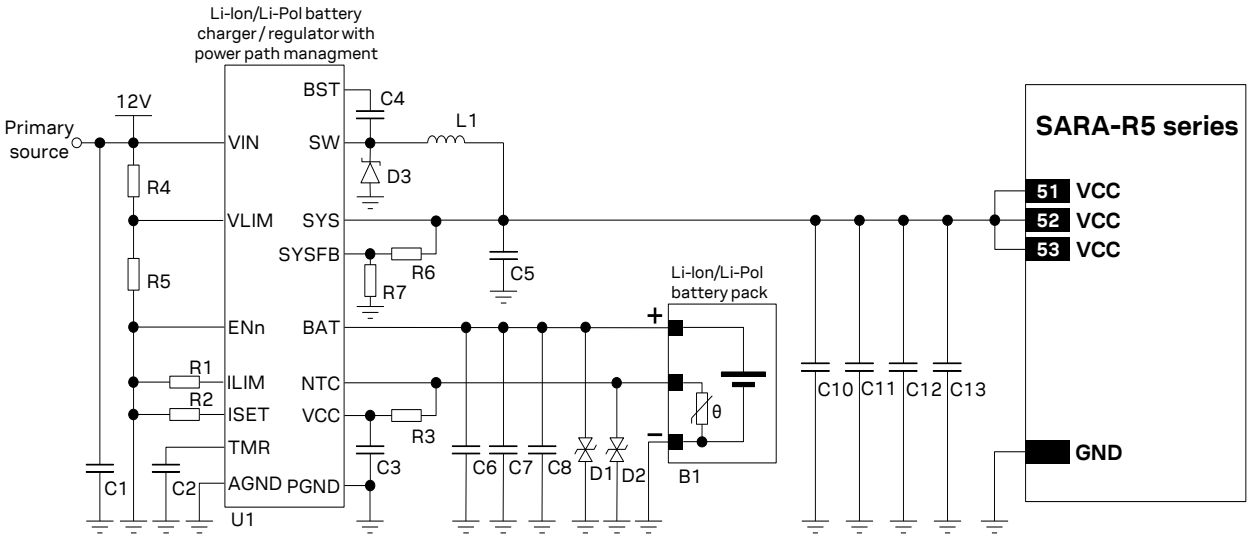

Figure 26: Li-Ion (or Li-Pol) battery charging and power path management application circuit

Reference	Description	Part number – Manufacturer
B1	Li-Ion (or Li-Pol) battery pack with 10 kΩ NTC	Various manufacturer
C1, C5, C6	22 µF capacitor ceramic X5R 0603 10% 25 V	GRM188R60J226MEA0 – Murata
C2, C4, C10	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
C3	1 µF capacitor ceramic X7R 0603 10% 25 V	GCM188R71E105KA64 – Murata
C7, C12	68 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H680JA16 – Murata
C8, C13	15 pF capacitor ceramic C0G 0402 5% 25 V	GJM1555C1H150JB01 – Murata
C11	10 nF capacitor ceramic X7R 0402 10% 16 V	GRT155R71C103KE01 – Murata
D1, D2	Low capacitance ESD protection	CG0402MLE-18G – Bourns
D3	Schottky diode 40 V 3 A	MBRA340T3G – ON Semiconductor
R1, R3, R5, R7	10 kΩ resistor 0402 1% 1/16 W	Generic manufacturer
R2	1.05 kΩ resistor 0402 1% 0.1 W	Generic manufacturer
R4	22 kΩ resistor 0402 1% 1/16 W	Generic manufacturer
R6	26.5 kΩ resistor 0402 1% 1/16 W	Generic manufacturer
L1	2.2 µH inductor 7.4 A 13 mΩ 20%	SRN8040-2R2Y – Bourns
U1	Li-Ion/Li-Pol battery DC-DC charger / regulator with integrated power path management function	MP2617H – Monolithic Power Systems (MPS)

Table 13: Suggested components for battery charging and power path management application circuit

☞ See the section 2.2.1.9, and in particular Figure 28 / Table 15, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.8 Guidelines for removing VCC supply

Removing the **VCC** power can be useful to minimize the current consumption when the SARA-R500S and SARA-R510M8S modules are switched off. The application processor can disconnect the **VCC** supply source from the module and zero out the module's current.

The **VCC** supply source can be removed using an appropriate low-leakage load switch or p-channel MOSFET controlled by the application processor as shown in Figure 27, using an external switch with:

- Very low leakage current (for example, less than 60 µA), to minimize the current consumption
- Very low $R_{DS(ON)}$ series resistance (for example, less than 50 mΩ), to minimize voltage drops
- Adequate maximum drain current (see the SARA-R5 series data sheet [1] for module current consumption figures)

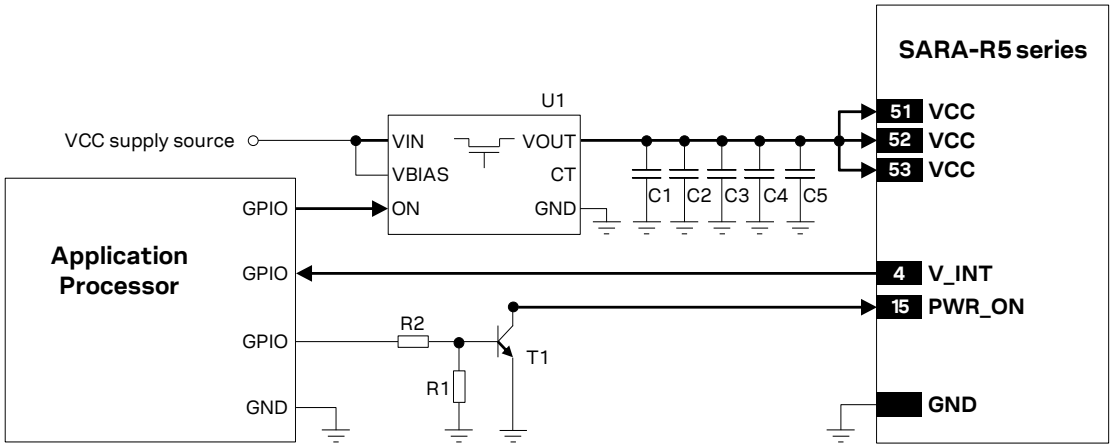

Figure 27: Example of application circuit for VCC supply removal

Reference	Description	Part number – Manufacturer
C1	10 µF capacitor ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 – Murata
C2	10 nF capacitor ceramic X7R 0402 10% 16 V	GRT155R71C103KE01 – Murata
C3	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
C4	68 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H680JA16 – Murata
C5	15 pF capacitor ceramic C0G 0402 5% 25 V	GJM1555C1H150JB01 – Murata
R1, R3	47 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R2	10 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
T1	NPN BJT transistor	BC847 – Infineon
U1	Ultra-low resistance load switch	TPS22967 – Texas Instruments

Table 14: Components for VCC supply removal application circuit

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply during SARA-R5 series normal operations: the **VCC** supply can be removed only after **V_INT** goes low, indicating that the module has entered deep-sleep mode or power-off mode.

☞ In case of applications where an abrupt power removal cannot be avoided, it is recommended to set the **RESET_N** input line at the low logic level as soon as the power failure in the supply source is detected, so that the under-voltage shutdown may be executed more safely since ~405 ms after the falling edge at the **RESET_N** input line.

☞ See the section 2.2.1.9, and in particular Figure 28 / Table 15, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.9 Additional guidelines for VCC supply circuit design

To reduce voltage drops, use a low impedance power source. The series resistance of the supply lines (connected to the modules' **VCC** and **GND** pins) on the application board and battery pack should also be considered and minimized: cabling and routing must be as short as possible to minimize losses.

Three pins are allocated to **VCC** supply connection. Several pins are designated for **GND** connection. It is recommended to correctly connect all of them to supply the module minimizing series resistance.

To reduce voltage ripple and noise, improving RF performance especially if the application device integrates an internal antenna, place the following bypass capacitors near the **VCC** pins:

- 68 pF capacitor with self-resonant frequency in the 700/800/900 MHz range (e.g. Murata GRM1555C1H680J), to filter EMI in the low cellular frequency bands
- 15 pF capacitor with self-resonant frequency in the 1700/1800/1900 MHz range (as Murata GRM1555C1H150J), to filter EMI in the high cellular frequency bands
- 10 nF capacitor (e.g. Murata GRM155R71C103K), to filter digital logic noise from clocks and data
- 100 nF capacitor (e.g. Murata GRM155R61C104K), to filter digital logic noise from clocks and data

An additional capacitor is recommended to avoid undershoot and overshoot at the start and at the end of RF transmission:

- 10 µF capacitor, or greater capacitor, with low ESR (e.g. Murata GRM188R60J106ME47)

An additional series ferrite bead may be provided for additional RF noise filtering, in particular if the application device integrates an internal antenna:

- Ferrite bead specifically designed for EMI / noise suppression in the GHz frequency band (e.g. the Murata BLM18EG221SN1), placed as close as possible to the **VCC** input pins of the module, implementing the circuit described in Figure 28, to filter out EMI in all the cellular bands

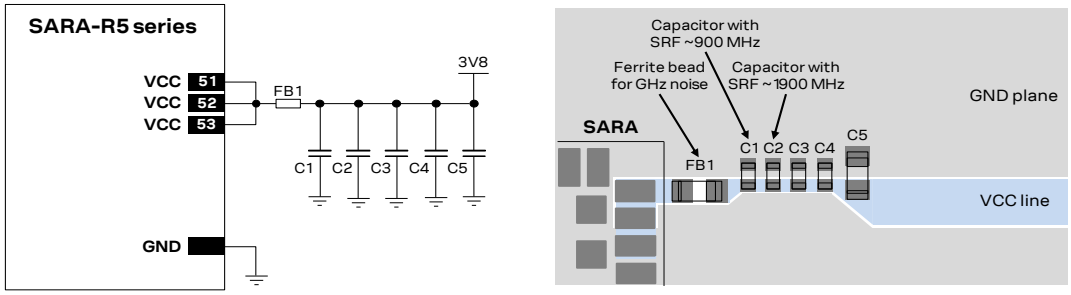

Figure 28: Suggested design to reduce ripple / noise on VCC, in particular suitable when using an integrated antenna

Reference	Description	Part number – Manufacturer
C1	68 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H680JA16 – Murata
C2	15 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H150JB01 – Murata
C3	10 nF capacitor ceramic X7R 0402 10% 16 V	GRT155R71C103KE01 – Murata
C4	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
C5	10 µF capacitor ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 – Murata
FB1	Chip Ferrite bead EMI filter for GHz band noise 220 Ω at 100 MHz, 260 Ω at 1 GHz, 2000 mA	BLM18EG221SN1 – Murata

Table 15: Suggested components to reduce ripple / noise on VCC

☞ The necessity of each part depends on the specific design, but it may be in particular suitable to provide all the parts described in Figure 28 / Table 15 if the application device integrates an internal antenna.

☞ ESD sensitivity rating of the **VCC** supply pins is 1 kV (HBM according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if accessible battery connector is directly connected to the supply pins. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible point.

2.2.1.10 Guidelines for VCC supply layout design

Good connection of the module **VCC** pins with DC supply source is required for correct RF performance. Guidelines are summarized in the following list:

- All the available **VCC** pins must be connected to the DC source.
- The series resistance along the **VCC** path must be as minimum as possible.
- Any series component with Equivalent Series Resistance (ESR) greater than few milliohms must be avoided.
- **VCC** connection must be routed through a PCB area separated from RF lines / parts, sensitive analog signals and sensitive functional units: it is good practice to interpose at least one layer of PCB ground between the **VCC** track and other signal routing.
- **VCC** connection must be routed as far as possible from the antenna, in particular if embedded in the application device: see Figure 29.
- Coupling between **VCC** and digital lines must be avoided.
- The tank bypass capacitor for current spikes smoothing described in section 2.2.1.9 should be placed close to the **VCC** pins. If the main DC source is a switching DC-DC converter, place the large capacitor close to the DC-DC output and minimize **VCC** track length. Otherwise consider using separate capacitors for DC-DC converter and module.
- The bypass capacitors in the pF range described in Figure 28 and Table 15 should be placed as close as possible to the **VCC** pins, where the **VCC** line narrows close to the module input pins, improving the RF noise rejection in the band centered on the self-resonant frequency of the pF capacitors. This is in particular suitable if the application device integrates an internal antenna.
- Since **VCC** input provides the supply to RF power amplifiers, voltage ripple at high frequency may result in unwanted spurious modulation of transmitter RF signal. This is more likely to happen with switching DC-DC converters, in which case it is better to select the highest operating frequency for the switcher and add a large L-C filter before connecting to the SARA-R5 series modules in the worst case.
- Shielding of switching DC-DC converter circuit, or at least the use of shielded inductors for the switching DC-DC converter, may be considered since all switching power supplies may potentially generate interfering signals as a result of high-frequency high-power switching.
- If **VCC** is protected by transient voltage suppressor to ensure that the voltage maximum ratings are not exceeded, place the protecting device along the path from the DC source toward the module, preferably closer to the DC source (otherwise protection function may be compromised).

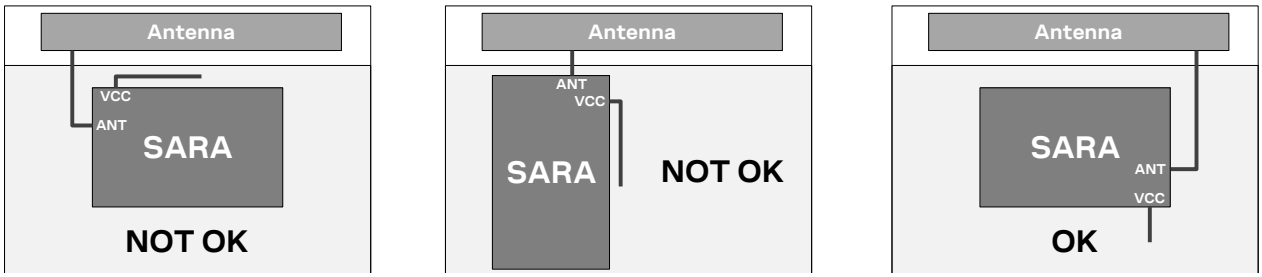

Figure 29: VCC line routing guideline for designs integrating an embedded antenna

2.2.1.11 Guidelines for grounding layout design

Good connection of the module **GND** pins with application PCB solid ground layer is required for correct RF performance. It significantly reduces EMC issues and provides a thermal heat sink for the module.

- Connect each **GND** pin with application board solid GND layer. It is strongly recommended that each **GND** pad surrounding **VCC** pins have one or more dedicated via down to the application board solid ground layer.
- The **VCC** supply current flows back to main DC source through GND as ground current: provide adequate return path with suitable uninterrupted ground plane to main DC source.
- It is recommended to implement one layer of the application PCB as GND plane as wide as possible.
- If the application board is a multilayer PCB, then all the layers should be filled with GND plane as much as possible and each GND area should be connected together with complete via stack down to the main ground layer of the board. Use as many vias as possible to connect the ground planes.
- Provide a dense line of vias at the edges of each GND area, in particular along RF and high-speed lines.
- If the whole application device is composed by more than one PCB, then it is required to provide a good and solid ground connection between the GND areas of all the different PCBs.
- Good grounding of **GND** pads also ensures thermal heat sink. This is critical during connection, when the real network commands the module to transmit at maximum power: correct grounding helps prevent module overheating.

2.2.2 Generic digital interfaces supply output (V_INT)

2.2.2.1 Guidelines for V_INT circuit design

SARA-R5 series modules provide the **V_INT** generic digital interfaces 1.8 V supply output, which can be mainly used to:

- Indicate when the module is switched on and it is not in the deep-sleep mode or power-off mode
- Supply external devices, as voltage translators, instead of using an external discrete regulator (e.g. see 2.6.1)
- Pull-up SIM detection signal (see section 2.5 for more details)

☞ Do not apply loads which might exceed the maximum available current from **V_INT** supply (see SARA-R5 series data sheet [1]) as this can cause malfunctions in internal circuitry.

☞ **V_INT** can only be used as an output: do not connect any external supply source on **V_INT**.

☞ ESD sensitivity rating of the **V_INT** supply pin is 1 kV (HBM according to JESD22-A114). Higher protection level could be required if the line is externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG) close to accessible point.

☞ It is recommended to monitor the **V_INT** pin to sense the end of the internal switch-off sequence of SARA-R5 series modules: **VCC** supply can be removed only after **V_INT** goes low.

☞ It is recommended to provide direct access to the **V_INT** pin on the application board by means of an accessible test point directly connected to the **V_INT** pin.

2.2.2.2 Guidelines for V_INT layout design

V_INT digital interfaces supply output is generated by an integrated switching step-down converter, used internally to supply the digital interfaces. Because of this, it can be a source of noise: avoid coupling with sensitive signals.

2.3 System functions interfaces

2.3.1 Module power-on (PWR_ON)

2.3.1.1 Guidelines for PWR_ON circuit design

SARA-R5 series **PWR_ON** input is equipped with an internal active pull-up resistor; an external pull-up resistor is not required and should not be provided.

If connecting the **PWR_ON** input to a push button, the pin will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection should be provided close to the accessible point, as described in Figure 30 and Table 16.

ESD sensitivity rating of the **PWR_ON** pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to **PWR_ON** pin, and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to the accessible point.

An open drain or open collector output is suitable to drive the **PWR_ON** input from an application processor, as described in Figure 30.

PWR_ON input pin should not be driven high by an external device, as it may cause start up issues.

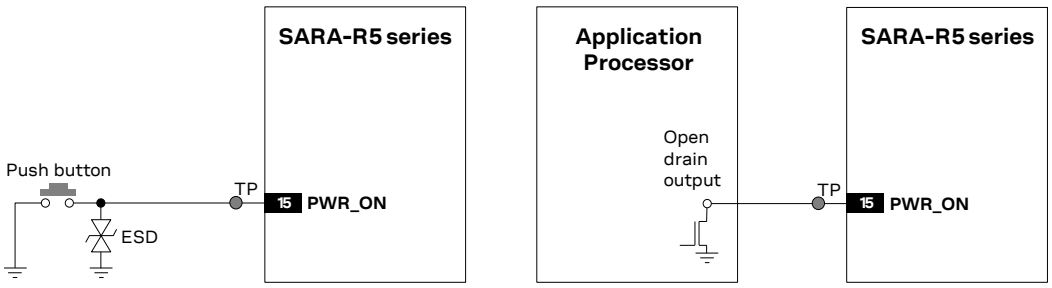

Figure 30: PWR_ON application circuits using a push button and an open drain output of an application processor

Reference	Description	Part number – Manufacturer
ESD	Varistor for ESD protection	B72590T8140S160 – TDK

Table 16: Example ESD protection component for the PWR_ON application circuit

It is recommended to provide direct access to the **PWR_ON** pin on the application board by means of an accessible test point directly connected to the **PWR_ON** pin.

2.3.1.2 Guidelines for PWR_ON layout design

The power-on circuit (**PWR_ON**) requires careful layout due to the pin function (see sections 1.6.1 and 1.6.2). It is required to ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious power-on request.

2.3.2 Module reset (RESET_N)

2.3.2.1 Guidelines for RESET_N circuit design

SARA-R5 series **RESET_N** is equipped with an internal active pull-up; an external pull-up resistor is not required and should not be provided.

If connecting the **RESET_N** input to a push button, the pin will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection device (e.g. the EPCOS CA05P4S14THSG varistor) should be provided close to accessible point on the line connected to this pin, as described in Figure 31 and Table 17.

ESD sensitivity rating of the **RESET_N** pin is 1 kV (HBM according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to the **RESET_N** pin, and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible point.

An open drain output or open collector output is suitable to drive the **RESET_N** input from an application processor, as described in Figure 31.

RESET_N input pin should not be driven high by an external device, as it may cause start up issues.

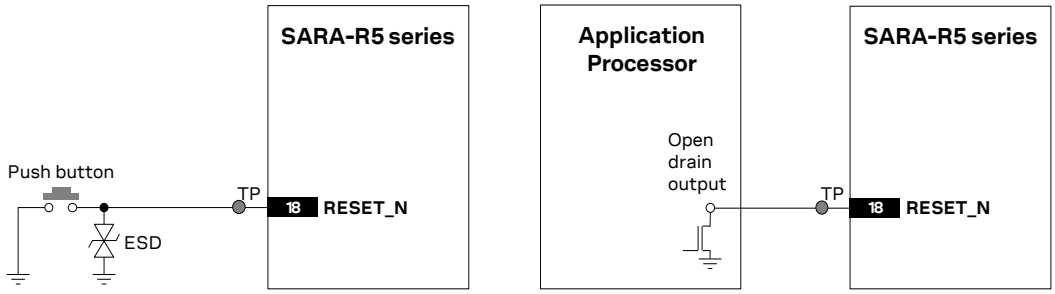

Figure 31: RESET_N application circuits using a push button and an open drain output of an application processor

Reference	Description	Part number – Manufacturer
ESD	Varistor for ESD protection	B72590T8140S160 – TDK

Table 17: Example of ESD protection component for the RESET_N application circuits

If the external reset function is not required by the customer application, the **RESET_N** input pin can be left unconnected to external components, but it is recommended providing direct access on the application board by means of an accessible test point directly connected to the **RESET_N** input pin.

2.3.2.2 Guidelines for RESET_N layout design

The **RESET_N** circuit require careful layout due to the pin function (see section 1.6.3). Ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious reset request. It is recommended to keep the connection line to **RESET_N** pin as short as possible.

2.4 Antenna interfaces

SARA-R5 series modules provide a cellular RF interface for connecting the external cellular antenna: the **ANT** pin represents the cellular RF input/output for cellular signals transmission and reception.

SARA-R510M8S modules provide also a GNSS RF interface for connecting the external GNSS antenna: the **ANT_GNSS** pin represents the GNSS RF input for GNSS signals reception.

The **ANT** and **ANT_GNSS** pins have a nominal characteristic impedance of 50 Ω and must be connected to the related physical antenna through a 50 Ω transmission line to allow clean transmission / reception of RF signals.

2.4.1 General guidelines for antenna interfaces

2.4.1.1 Guidelines for ANT and ANT_GNSS pins RF connection design

☞ The GNSS antenna RF interface is not supported by SARA-R500S and SARA-R510S modules.

A clean transition between the **ANT** and **ANT_GNSS** pads and the application board PCB must be provided, implementing the following design-in guidelines for the layout of the application PCB close to the **ANT** and **ANT_GNSS** pads:

- On a multilayer board, the whole layer stack below the RF connections should be free of digital lines
- Increase GND keep-out (i.e. clearance, a void area) around the **ANT** and **ANT_GNSS** pads, on the top layer of the application PCB, to at least 250 µm up to adjacent pads metal definition and up to 400 µm on the area below the module, to reduce parasitic capacitance to ground, as described in the left picture in Figure 32
- Add GND keep-out (i.e. clearance, a void area) on the buried metal layer below the **ANT** and **ANT_GNSS** pads if the top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground, as described in the right picture in Figure 32

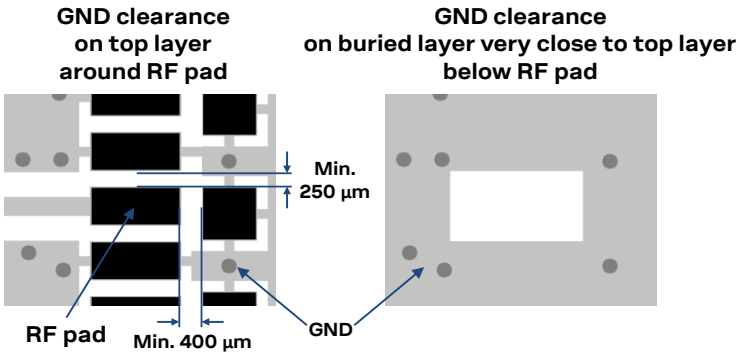

Figure 32: GND keep-out area on top layer around RF pad and on very close buried layer below RF pad (ANT / ANT_GNSS)

☞ See section 2.4.2.3 for the description of the antenna trace design implemented on the u-blox host printed circuit board used for conformity assessment of SARA-R5 series surface-mounted modules for regulatory type approvals such as FCC United States, ISED Canada, RED Europe, etc.

2.4.1.2 Guidelines for RF transmission lines design

☞ The GNSS antenna RF interface is not supported by SARA-R500S and SARA-R510S modules.

Any RF transmission line, such as the ones from the **ANT** and **ANT_GNSS** pads up to the related antenna connector or up to the related internal antenna pad, must be designed so that the characteristic impedance is as close as possible to 50 Ω.

RF transmission lines can be designed as a micro strip (consists of a conducting strip separated from a ground plane by a dielectric material) or a strip line (consists of a flat strip of metal which is sandwiched between two parallel ground planes within a dielectric material). The micro strip, implemented as a coplanar waveguide, is the most common configuration for printed circuit board.

Figure 33 and Figure 34 provide two examples of suitable 50 Ω coplanar waveguide designs. The first example of RF transmission line can be implemented in case of 4-layer PCB stack-up herein described, and the second example of RF transmission line can be implemented in case of 2-layer PCB stack-up herein described.

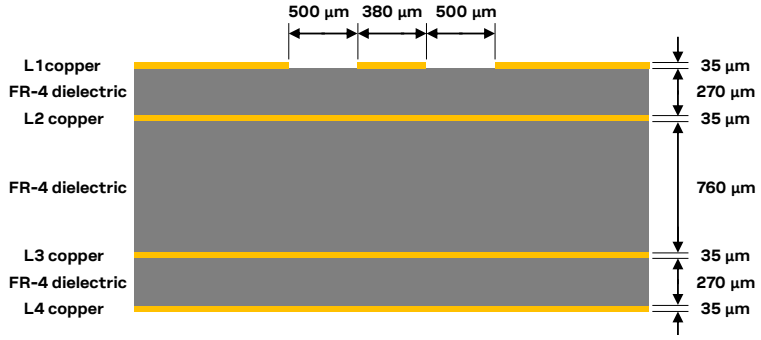

Figure 33: Example of 50 Ω coplanar waveguide transmission line design for the described 4-layer board layup

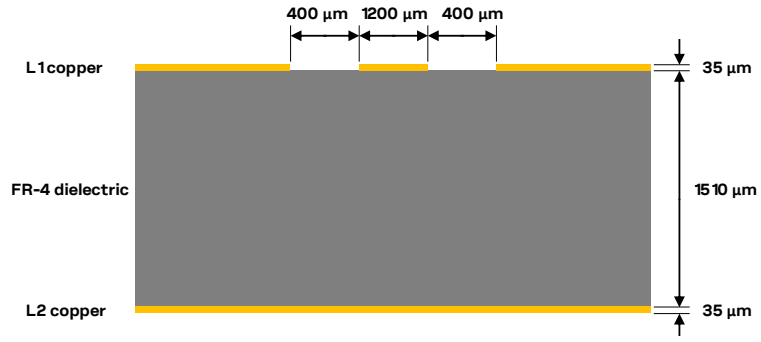

Figure 34: Example of 50 Ω coplanar waveguide transmission line design for the described 2-layer board layup

If the two examples do not match the application PCB stack-up, then the 50 Ω characteristic impedance calculation can be made using the HFSS commercial finite element method solver for electromagnetic structures from Ansys Corporation, or using freeware tools like Avago / Broadcom AppCAD (https://www.broadcom.com/appcad) taking care of the approximation formulas used by the tools for the impedance computation.

To achieve a 50 Ω characteristic impedance, the transmission line width must be chosen due to:

- the thickness of the transmission line itself (e.g. 35 µm in the example of Figure 33 and Figure 34)
- the thickness of the dielectric material between the top layer (where the line is routed) and the inner closer layer implementing the ground plane (e.g. 270 µm in Figure 33, 1510 µm in Figure 34)
- the dielectric constant of the dielectric material (e.g. dielectric constant of the FR-4 dielectric material in Figure 33 and Figure 34)
- the gap from the transmission line to the adjacent ground plane on the same layer of the transmission line (e.g. 500 µm in Figure 33, 400 µm in Figure 34)

If the distance between the transmission line and the adjacent GND area (on the same layer) does not exceed 5 times the width of the line, use the “Coplanar Waveguide” model for the 50 Ω calculation.

Additionally to the 50 Ω impedance, the following guidelines are recommended for transmission lines:

- Minimize the transmission line length: the insertion loss should be minimized as much as possible, in the order of a few tenths of a dB,
- Add GND keep-out (i.e. clearance, a void area) on buried metal layers below any pad of component present on the RF transmission lines, if top-layer to buried layer dielectric thickness is below 200 μm, to reduce parasitic capacitance to ground,
- The transmission lines width and spacing to GND must be uniform and routed as smoothly as possible: avoid abrupt changes of width and spacing to GND,
- Add GND stitching vias around transmission lines, as described in Figure 35,
- Ensure solid metal connection of the adjacent metal layer on the PCB stack-up to main ground layer, providing enough vias on the adjacent metal layer, as described in Figure 35,
- Route RF transmission lines far from any noise source (as switching supplies and digital lines) and from any sensitive circuit (as USB),
- Avoid stubs on the transmission lines,
- Avoid signal routing in parallel to transmission lines or crossing the transmission lines on buried metal layer,
- Do not route microstrip lines below discrete component or other mechanics placed on top layer

Two examples of a suitable RF circuit design for **ANT** pin are illustrated in Figure 35, where the cellular antenna detection circuit is not implemented (if the cellular antenna detection function is required by the application, follow the guidelines for circuit and layout implementation detailed in section 2.4.5):

- In the first example shown on the left, the **ANT** pin is directly connected to an SMA connector by means of a suitable 50 Ω transmission line, designed with the appropriate layout.
- In the second example shown on the right, the **ANT** pin is connected to an SMA connector by means of a suitable 50 Ω transmission line, designed with the appropriate layout, with an additional high pass filter to improve the ESD immunity at the antenna port. (The filter consists of a suitable series capacitor and shunt inductor, for example the Murata GRM1555C1H150JB01 15 pF capacitor and the Murata LQG15HN39NJ02 39 nH inductor with SRF ~1 GHz.).

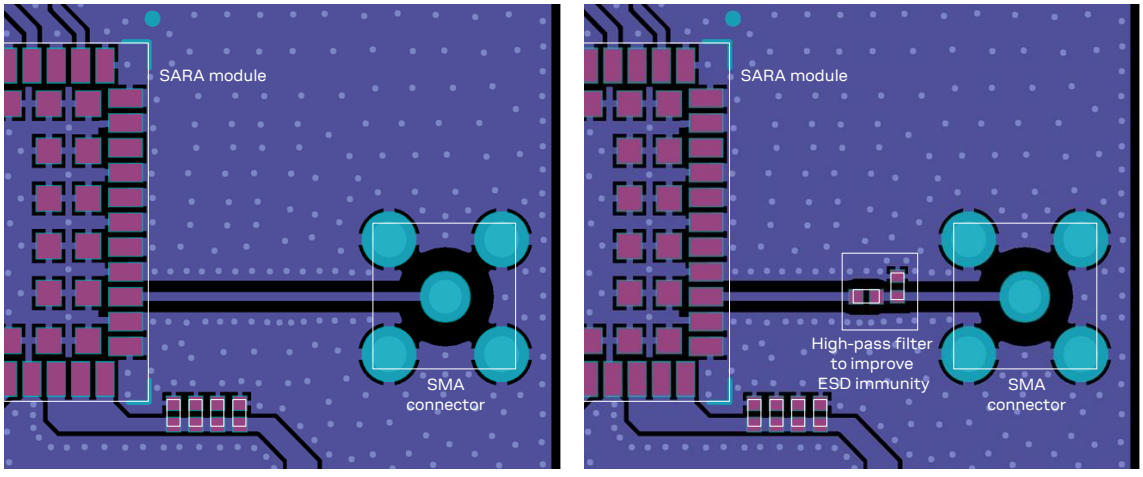

Figure 35: Example of circuit and layout for ANT RF circuits on the application board

☞ See section 2.4.2.3 for the description of the antenna trace design implemented on the u-blox host printed circuit board used for conformity assessment of SARA-R5 series surface-mounted modules for regulatory type approvals such as FCC United States, ISED Canada, RED Europe, etc.

2.4.1.3 Guidelines for RF termination design

☞ The GNSS antenna RF interface is not supported by SARA-R500S and SARA-R510S modules.

The RF termination must provide a characteristic impedance of 50 Ω as well as the RF transmission line up to the RF termination, to match the characteristic impedance of **ANT** and **ANT_GNSS** ports.

However, real antennas do not have a perfect 50 Ω load on all the supported frequency bands. So to reduce as much as possible any performance degradation due to antenna mismatching, the RF termination must provide optimal return loss (or VSWR) figures over all the operating frequencies, as summarized in Table 6 and Table 7.

If an external antenna is used, the antenna connector represents the RF termination on the PCB:

- Use a suitable 50 Ω connector providing a clean PCB-to-RF-cable transition.
- Strictly follow the connector manufacturer's recommended layout, for example:
  - SMA Pin-Through-Hole connectors require a GND keep-out (i.e. clearance, a void area) on all the layers around the central pin up to the annular pads of the four GND posts, as illustrated in Figure 35 or in Figure 41.
  - U.FL surface mounted connectors require no conductive traces (i.e. clearance, a void area) in the area below the connector between the GND land pads, as illustrated in Figure 36.

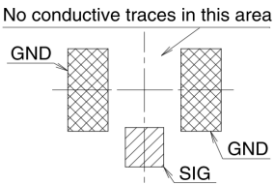

Figure 36: U.FL surface mounted connector mounting pattern layout

- Cut out the GND layer under the RF connector and close to any buried vias, to remove stray capacitance and thus keep the RF line at 50 Ω, e.g. the active pad of U.FL connector needs to have a GND keep-out (i.e. clearance, a void area) at least on the first inner layer to reduce parasitic capacitance to ground.

If an integrated antenna is used, the integrated antenna represents the RF terminations. The following guidelines should be followed:

- Use an antenna designed by an antenna manufacturer providing the best possible return loss.
- Provide a ground plane large enough according to the relative integrated antenna requirements. The ground plane of the application PCB can be reduced down to a minimum size that must be similar to one quarter of wavelength of the minimum frequency that needs to be radiated. As numerical example,
  Frequency = 617 MHz → Wavelength ≅ 48 cm → Minimum GND plane size ≅ 12 cm
- It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including the PCB layout and matching circuitry.
- Further to the custom PCB and product restrictions, the antenna may require a tuning to comply with all the applicable required certification schemes. It is recommended to consult the antenna manufacturer for antenna matching design-in guidelines relative to the custom application.

Additionally, these recommendations regarding the antenna system placement must be followed:

- Do not place the antennas within a closed metal case.
- Do not place the cellular antenna in close vicinity to the end user since the emitted radiation in human tissue is restricted by regulatory requirements.
- Place the antennas as far as possible from VCC supply line and related parts (see also Figure 29), from high speed digital lines (as USB) and from any possible noise source.

- Place the antenna far from sensitive analog systems or employ countermeasures to reduce EMC or EMI issues.
- Be aware of interaction between co-located RF systems since the LTE transmitted power may interact or disturb the performance of companion systems (see also section 2.4.4).

☞ See section 2.4.2.3 for the description of the antenna trace design implemented on the u-blox host printed circuit board used for conformity assessment of SARA-R5 series surface-mounted modules for regulatory type approvals such as FCC United States, ISED Canada, RED Europe, etc.

2.4.2 Cellular antenna RF interface (ANT)

2.4.2.1 Guidelines for antenna selection and design

The antenna is the most critical component to be evaluated. Designers must take care of the antenna from all perspective at the very start of the design phase when the physical dimensions of the application board are under analysis/decision, since the cellular compliance of the device integrating SARA-R5 series modules with all the applicable required certification schemes depends on antenna's radiating performance.

Cellular antennas are typically available as:

- External antennas (e.g. linear monopole):
  - External antennas basically do not imply physical restriction to the design of the PCB where the SARA-R5 series module is mounted.
  - The radiation performance mainly depends on the antennas. It is required to select antennas with optimal radiating performance in the operating bands.
  - RF cables should be carefully selected to have minimum insertion losses. Additional insertion loss will be introduced by low quality or long cable. Large insertion loss reduces both transmit and receive radiation performance.
  - A high quality 50 Ω RF connector provides a clean PCB-to-RF-cable transition. It is recommended to strictly follow the layout and cable termination guidelines provided by the connector manufacturer.
- Integrated antennas (e.g. PCB antennas such as patches or ceramic SMT elements):
  - Internal integrated antennas imply physical restriction to the design of the PCB: Integrated antenna excites RF currents on its counterpoise, typically the PCB ground plane of the device that becomes part of the antenna: its dimension defines the minimum frequency that can be radiated. Therefore, the ground plane can be reduced down to a minimum size that should be similar to the quarter of the wavelength of the minimum frequency that needs to be radiated, given that the orientation of the ground plane relative to the antenna element must be considered. As numerical example, the physical restriction to the PCB design can be considered as following:

    Frequency = 617 MHz → Wavelength ≅ 48 cm → Minimum GND plane size ≅ 12 cm
  - Radiation performance depends on the whole PCB and antenna system design, including product mechanical design and usage. Antennas should be selected with optimal radiating performance in the operating bands according to the mechanical specifications of the PCB and the whole product.
  - It is recommended to select a custom antenna designed by an antennas' manufacturer if the required ground plane dimensions are very small (e.g. less than 6.5 cm long and 4 cm wide). The antenna design process should begin at the start of the whole product design process.
  - It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.

- Further to the custom PCB and product restrictions, antennas may require tuning to obtain the required performance for compliance with all the applicable required certification schemes. It is recommended to consult the antenna manufacturer for the design-in guidelines for antenna matching relative to the custom application.

In both of cases, selecting external or internal antennas, these recommendations should be observed:

- Select an antenna providing optimal return loss / VSWR / efficiency figure over all the operating cellular frequencies.
- Select an antenna providing the worst possible return loss / VSWR / efficiency figure in the GNSS frequency band, to optimize the RF coexistence between the cellular and the GNSS systems (see section 2.4.4 for further details and guidelines regarding Cellular / GNSS RF coexistence).
- Select an antenna providing appropriate gain figure (i.e. combined directivity and efficiency figure) so that the RF radiation intensity do not exceed the regulatory limits specified in some countries: refer to the FCC United States notice reported in section 4.2.2, the ISED Canada notice reported in section 4.3.1, the RED Europe notice reported in section 4.4.

2.4.2.2 Examples of cellular antennas

Table 18 lists some examples of possible internal on-board surface-mount cellular antennas.

Manufacturer	Part number	Product name	Description
Taoglas	PA.760.A	WarriorX	Wideband cellular SMD antenna 600..6000 MHz 40.0 x 5.0 x 6.0 mm
Taoglas	PCS.26.A	Havok	Cellular SMD antenna 617..960 MHz, 1710..2690 MHz 54.6 x 13.0 x 3.0 mm
Taoglas	PCS.66.A	Reach	Wideband cellular SMD antenna 600..6000 MHz 32.0 x 25.0 x 1.6 mm
Taoglas	PCS.68.A	Reach	Low-profile, wideband cellular SMD antenna 600..6000 MHz 42.0 x 10.0 x 1.5 mm
Antenova	SR4L002	Lucida	Cellular SMD antenna 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 35.0 x 8.5 x 3.2 mm
AVX / Ethertronics	1004795 / 1004796		Cellular SMD antenna 617..960 MHz, 1710..2200 MHz, 2490..2700 MHz 36.0 x 9.0 x 3.2 mm
AVX / Ethertronics	P822601 / P822602		Cellular SMD antenna 698..960 MHz, 1710..2170 MHz, 2490..2700 MHz 50.0 x 8.0 x 3.2 mm
AVX / Ethertronics	1002436		Cellular vertical mount antenna 698..960 MHz, 1710..2700 MHz 50.6 x 19.6 x 1.6 mm
Fractus	NN03-310	TRIO mXTEND™	Cellular SMD antenna 698..8000 MHz 30.0 x 3.0 x 1.0 mm
PulseLarsen Antennas	W3796	Domino	Cellular SMD antenna 698..960 MHz, 1427..1661 MHz, 1695..2200 MHz, 2300..2700 MHz 42.0 x 10.0 x 3.0 mm
Molex	1462000001		Cellular SMD antenna 698..960 MHz, 1700..2700 MHz 40.0 x 5.0 x 5.0 mm

Manufacturer	Part number	Product name	Description
Cirocomm	DSAN0001		Ceramic LTE SMD antenna 698..960 MHz, 1710..2170 MHz 40.0 x 6.0 x 5.0 mm
Amotech	AMMAL004 / AMMAL008	Chip	Cellular SMD Antenna 699..960 MHz, 1710..2690 MHz 35.0 x 9.0 x 3.2 mm
Amotech	AMMAL021 / AMMAL022	Chip	Cellular SMD Antenna 617..960 MHz, 1710..6000 MHz 39.0 x 9.0 x 3.2 mm

Table 18: Examples of internal surface-mount cellular antennas

Table 19 lists some examples of possible internal off-board PCB-type cellular antennas with cable and connector.

Manufacturer	Part number	Product name	Description
PulseLarsen Antennas	W3929B0100		LTE FPC antenna with coax feed 617..960 MHz, 1710..2690 MHz, 3400..3900 MHz 115.8 x 30.4 mm
Taoglas	FXUB64	Cyclone	LTE wideband flex antenna 617..960 MHz, 1710..2690 MHz 130.0 x 30.0 mm
Taoglas	FXUB63		Cellular PCB antenna with cable and U.FL 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2690 MHz 96.0 x 21.0 mm
Taoglas	FXUB66	Maximus	Wideband flexible antenna 600..6000 MHz 120.4 x 50.4 x 0.2 mm
Laird Tech.	EFF692SA3S	Revie Flex	Flexible LTE antenna 689..875 MHz, 1710..2500 MHz 90.0 x 20.0 mm
Antenova	SRFL026	Mitis	Cellular antenna on flexible PCB with cable and U.FL 689..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2500..2690 MHz 110.0 x 20.0 mm
AVX / Ethertronics	1002289		Cellular antenna on flexible PCB with cable and U.FL 698..960 MHz, 1710..2700 MHz 140.0 x 75.0 mm
EAD	FSQS35241-UF-10	SQ7	Cellular PCB antenna with cable and U.FL 690..960 MHz, 1710..2170 MHz, 2500..2700 MHz 110.0 x 21.0 mm
Amotech	AMMAL024	FPCB+cable	LTE FPCB antenna with coaxial cable and connector 617..5000 MHz 120.0 x 30.0 mm
Amotech	AMMAL030U200	FPCB+cable	LTE FPCB antenna with coaxial cable and connector 699..960 MHz, 1427..3800 MHz 43.0 x 43.0 mm

Table 19: Examples of internal cellular antennas with cable and connector

Table 20 lists some examples of possible external cellular antennas.

Manufacturer	Part number	Product name	Description
Taoglas	GSA.8842.A		Wideband LTE I-Bar adhesive antenna with cable and SMA(M) 617..960 MHz, 1710..2700 MHz, 4900..5850 MHz 176.5 x 59.2 x 13.6 mm
Taoglas	TG.55.8113		LTE terminal mount monopole antenna with 90° hinged SMA(M) 600..6000 MHz 172.0 x 23.9 x 13 mm
Taoglas	TG.35.8113	Apex II	Wideband LTE dipole terminal antenna hinged SMA(M) 600..6000 MHz 224 x 57.6 x 13 mm
Taoglas	GSA.8835	Phoenix	5G/4G Adhesive Mount Antenna, IP67-rated enclosure 600..6000 MHz 105 x 30 x 7.9 mm
AVX / Ethertronics	1003657		LTE / Cellular antenna with RG178 coax cable and MMCX connector 698..960 MHz, 1710..2700 MHz 104 x 22 x 4.2 mm
AVX / Ethertronics	1004112		Broadband External LTE / Cellular Antenna 698..960 MHz, 1710..2700 MHz 218.2 x 27.2 x 13.8 mm
AVX / Ethertronics	X1005246		Adhesive-mount LTE external antenna 698..960 MHz, 1710..2170 MHz, 2300..2690 MHz, 1710..2700 MHz 105.1 x 30.1 x 6.7 mm
Laird Tech.	TRA6927M3PW-001		Cellular screw-mount antenna with N-type(F) 698..960 MHz, 1710..2170 MHz, 2300..2700 MHz 83.8 x Ø 36.5 mm
Laird Tech.	CMS69273		Cellular ceiling-mount antenna with cable and N-type(F) 698..960 MHz, 1575.42 MHz, 1710..2700 MHz 86 x Ø 199 mm
Laird Tech.	OC69271-FNM		Cellular pole-mount antenna with N-type(M) 698..960 MHz, 1710..2690 MHz 248 x Ø 24.5 mm
PulseLarsen Antennas	SPDA24617/3900		Multiband swivel dipole antenna with SMA(M) 617..960 MHz, 1400..2700 MHz, 3200..3900 MHz 223.24 x 56.13 x 10.97 mm
Amotech	ACA556022-S0-A1		Low-profile, screw-type LTE/Sub6G antenna, Waterproof IP67 699..960 MHz, 1427..3800 MHz 55.0 x 60.0 x 22.0 mm
Amotech	ACA556022-S0-A2		Low-profile, adhesive-type LTE/Sub6G antenna, Waterproof IP67 699..960 MHz, 1427..3800 MHz 55.0 x 60.0 x 22.0 mm
Amotech	ACAD6623-S0-A1		Low-profile, roof-mount LTE/Sub6G antenna, Waterproof IP67 699..960 MHz, 1427..3800 MHz 23.0 x Ø 60.0 mm

Table 20: Examples of external cellular antennas

2.4.2.3 Antenna trace design used for SARA-R5 series modules' type approvals

The conformity assessment of u-blox SARA-R5 series LGA surface-mounted modules for regulatory type approvals such as FCC United States, ISED Canada, RED Europe, etc. has been carried out with the SARA-R5 series modules mounted on a u-blox host printed circuit board with a 50 Ω grounded coplanar waveguide designed on it, herein referenced as "antenna trace design", implementing the connection of the **ANT** LGA pad of the module, consisting in the cellular RF input/output of the module, up to a dedicated 50 Ω SMA female connector, consisting in the cellular RF input/output of the host printed circuit board for external antenna and/or RF cable access.

☞ Manufacturers of mobile or fixed devices incorporating SARA-R5 series modules are authorized to use the FCC United States Grants and ISED Canada Certificates of SARA-R5 series modules for their own final host products if, as per FCC KDB 996369, the antenna trace design implemented on the host PCB is electrically equivalent to the antenna trace design implemented on the u-blox host PCB used for regulatory type approvals of SARA-R5 series modules, described in this section.

☞ In case of antenna trace design change, an FCC Class II Permissive Change and/or ISED Class IV Permissive Change application is required to be filed by the grantee, or the host manufacturer can take responsibility through the change in FCC ID and/or the ISES Multiple Listing (new application) procedure followed by an FCC C2PC and/or ISED C4PC application.

The antenna trace design is implemented on the u-blox host PCB as illustrated in Figure 37, using the parts listed in Table 21, with the support of the additional optional antenna detection capability. Guidelines to design a proper equivalent optional antenna detection circuit on a host printed circuit board are available in section 2.4.5.

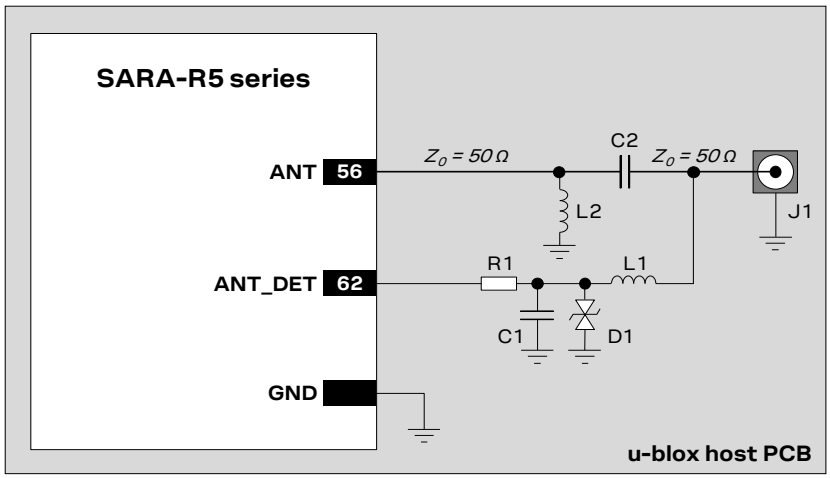

Figure 37: Antenna trace design implemented on the u-blox host PCB, with additional antenna detection circuit

Reference	Description	Part number – Manufacturer
C1	27 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H270JA16 – Murata
C2	33 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H330JA16 – Murata
D1	Very low capacitance ESD protection	PESD0402-140 – Tyco Electronics
L1	68 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 – Murata
R1	10 kΩ resistor 0402 1% 0.063 W	Generic manufacturer
J1	SMA connector 50 Ω through hole jack	SMA6251A1-3GT50G-50 – Amphenol
L2	39 nH multilayer inductor 0402 (SRF ~1 GHz)	Not Installed

Table 21: Parts in use on the u-blox host PCB for the antenna trace design, with additional antenna detection circuit

The u-blox host printed circuit board has a structure of 4 copper layers with 35 µm thickness (1 oz/ft^2) each, using FR4 dielectric substrate material with 4.3 typical permittivity at 1 GHz, and 0.013 typical loss tangent at 1 GHz.

The top layer layout of the u-blox host PCB designed to accommodate the **ANT** pad of SARA-R5 series module is described in Figure 38: the left side illustrates top layer copper mask and top layer solder resist mask, with top layer to bottom layer vias; the right side illustrates the PCB stack-up structure. Considering that the thickness of the dielectric material from the top layer to the buried layer is larger than 200 µm, no GND keep-out is implemented on the buried metal layer area below the **ANT** pad. Guidelines to design an equivalent proper connection for the **ANT** pad on a host printed circuit board are available in section 2.4.1.1.

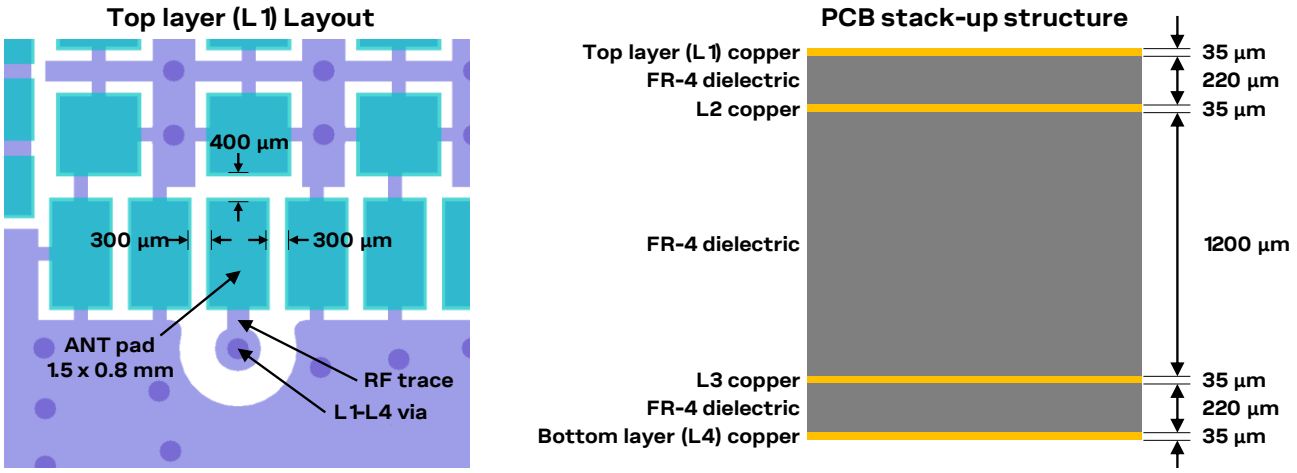

Figure 38: Top layer layout and stack-up structure of the u-blox host PCB for the ANT pad of the module

As illustrated on the left side of Figure 38, the antenna RF trace is routed from the RF pad on the top layer (L1) to the bottom layer (L4) through a dedicated via. After the via, the antenna RF trace, as 50 Ω transmission line, is connected to the antenna detection circuit described in Figure 37 and Table 21, with the layout illustrated on the left side of Figure 39. Guidelines to design a proper equivalent (optional) antenna detection circuit on a host printed circuit board are available in section 2.4.5.

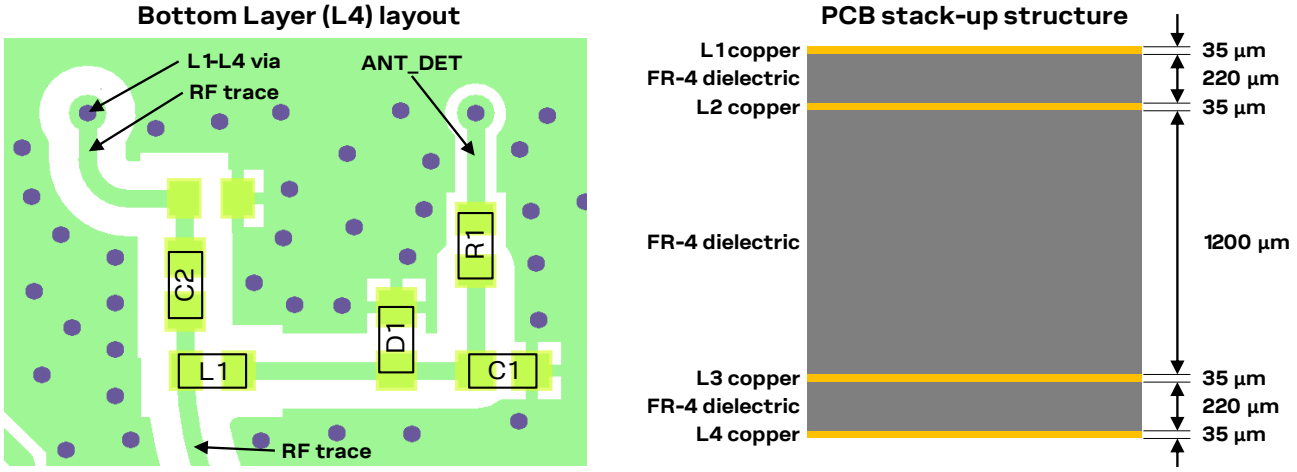

Figure 39: Bottom layer layout and stack-up structure of the u-blox host PCB for the antenna detection circuit

After the antenna detection circuit with the layout illustrated on the left side of Figure 39, the antenna RF trace is designed as a 50 Ω grounded coplanar waveguide on the bottom layer of the u-blox host printed circuit board, with total length ~29 mm, with layout and thickness, width, gap (signal to ground) characteristics illustrated in Figure 40. Guidelines to design a proper equivalent 50 Ω transmission line on a host printed circuit board are available in section 2.4.1.2.

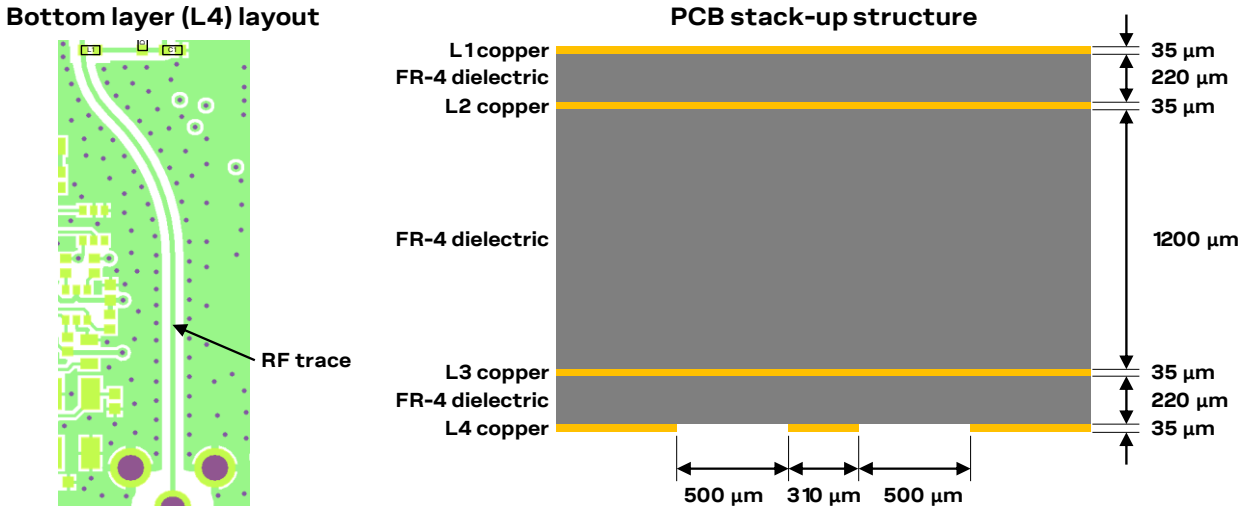

Figure 40: 50 Ω grounded coplanar waveguide transmission line designed on the u-blox host PCB bottom layer

The 50 Ω grounded coplanar waveguide routed on the bottom layer is terminated on a dedicated 50 Ω SMA female connector mounted on the top layer, consisting in the cellular RF input/output of the host PCB for external antenna and/or RF coaxial cable access, with board layout illustrated in Figure 41. Guidelines to design a proper equivalent 50 Ω termination on a host printed circuit board are available in section 2.4.1.3, with antenna selection and design guidelines available in section 2.4.2.1.

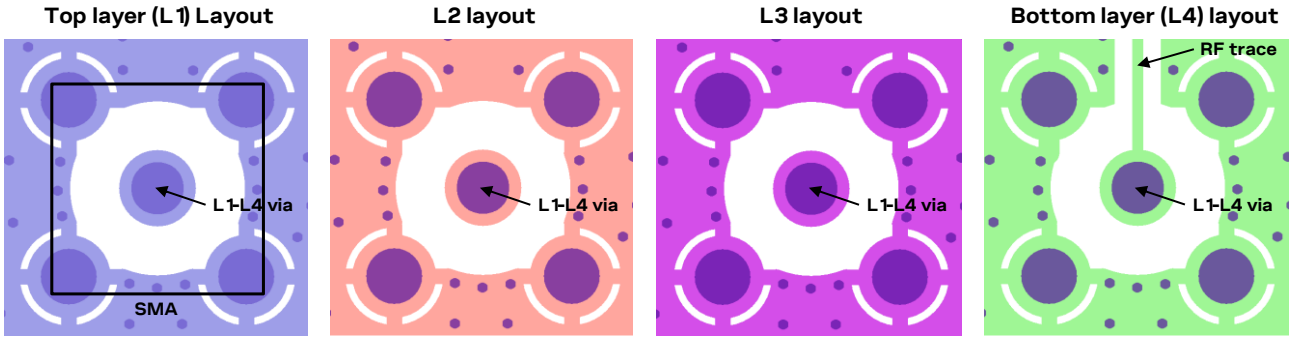

Figure 41: 50 Ω SMA female connector layout on the u-blox host PCB

The 50 Ω characteristic impedance of the antenna trace design on a host printed circuit board can be verified using a Vector Network Analyzer, as done on the u-blox host PCB, with calibrated RF coaxial cable soldered at the pad corresponding to RF input/output of the module and with the transmission line terminated to a 50 Ω load at the 50 Ω SMA female connector.

Compliance of the design with regulatory rules and specifications defined by the FCC, ISED, RED, etc. can be verified using a radio communication tester (callbox) as the Rohde & Schwarz CMW500, or any equivalent equipment for multi-technology signaling conformance tests.

2.4.3 GNSS antenna RF interface (ANT_GNSS)

☞ The GNSS antenna RF interface is not supported by SARA-R500S and SARA-R510S modules.

☞ The GNSS peripheral ANT_ON output pin is not supported by SARA-R510M8S-00B modules.

☞ For additional information and guidelines regarding the GNSS design, see the SARA-R5 / SARA-R4 positioning and timing implementation application note [18].

The antenna and its placement are critical system factors for accurate GNSS reception. Use of a ground plane will minimize the effects of ground reflections and enhance the antenna efficiency. A good allowance for ground plane size is typically in the area of 50 x 50 to 70 x 70 mm^2. The smaller the electrical size of the plane, the narrower the reachable bandwidth and the lower the radiation efficiency. Exercise care with rover vehicles that emit RF energy from motors etc. as interference may extend into the GNSS band and couple into the GNSS antenna suppressing the wanted signal. For more details about GNSS antennas see also the u-blox GNSS antennas application note [19].

Since SARA-R510M8S modules already include an internal SAW filter followed by an additional LNA before the u-blox M8 GNSS chipset (as illustrated in Figure 4), they are optimized to work with passive or active antennas without requiring additional external circuitry.

2.4.3.1 Guidelines for applications with a passive antenna

If a GNSS passive antenna with high gain and good sky view is used, together with a short 50 Ω line between antenna and receiver, and no jamming sources affect the GNSS passive antenna, the circuit illustrated in Figure 42 can be used. This provides the minimum BoM cost and minimum board space.

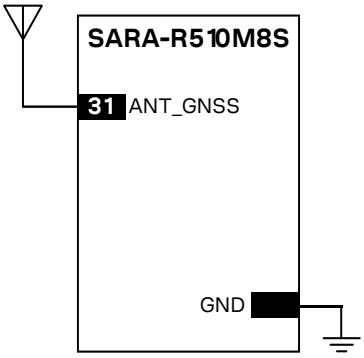

Figure 42: Minimum circuit with GNSS passive antenna

If the connection between the module and antenna incurs additional losses (e.g. antenna placed far away from the module, small ground plane for a patch antenna) or improved jamming immunity is needed due to strong out-of-band jammers close to the GNSS antenna (e.g. the cellular antenna is close to the GNSS antenna), consider adding an external SAW filter (see Table 22 for possible suitable examples) close to the GNSS passive antenna, followed by an external LNA (see Table 23 for possible suitable examples), as illustrated in Figure 43. Note that SARA-R510M8S modules already include an internal SAW filter followed by an LNA before the u-blox M8 GNSS chipset (as illustrated in Figure 4), so that additional external SAW and LNA are not required for most of the applications (see section 2.4.4 for further details and design-in guidelines regarding Cellular / GNSS RF coexistence).

☞ An external LNA with related external SAW filter are only required if the GNSS antenna is far away (more than 10 cm) from the GNSS RF input of the module. In that case, the SAW and the LNA must be placed close to the passive antenna.

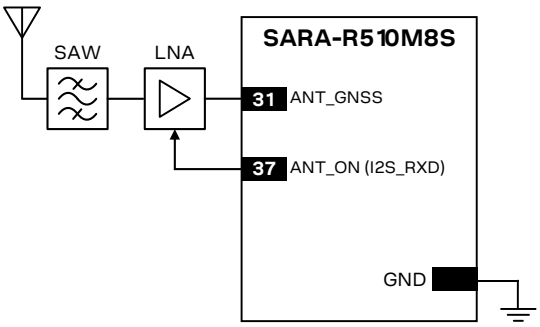

Figure 43: Typical circuit for best performance and improved jamming immunity with GNSS passive antenna

The external LNA can be selected to deliver the performance needed by the application in terms of:

- Noise figure (sensitivity)
- Selectivity and linearity (robustness against jamming)
- Robustness against RF power

Depending on the characteristics of the supply source (DC/DC regulator, linear LDO regulator or other) used to supply the external LNA, make sure some good filtering is in place for the external LNA supply because of the noise on the external LNA supply line can affect the performance of the LNA itself: consider adding a proper series ferrite bead (see Table 24 for possible suitable examples) and a proper decoupling capacitor to ground with self-resonant frequency in the GNSS frequency range (as for example the 27 pF 0402 capacitor Murata GCM1555C1H270JA16) at the input of the external LNA supply line.

It should be noted anyway that the insertion loss of the filter directly affects the system noise figure and hence the system performance. The selected SAW filter has to provide very low loss (no more than 1.5 dB) in the GNSS pass-band, beside providing very large attenuation (more than 40 to 60 dB) in the out-of-band jammers' cellular frequency bands (see Table 22 for possible suitable examples).

SARA-R510M8S already provides an integrated SAW filter and LNA (as illustrated in Figure 4). The addition of such external components should be carefully evaluated, especially in case the application power consumption should be minimized, since the LNA alone requires an additional supply current of typically 5 to 20 mA.

Moreover, the first LNA of the input chain will dominate the receiver noise performance, therefore its noise figure should be less than 2 dB. If the antenna is close to the receiver, then a good passive antenna (see Table 25) can be directly connected to the receiver with a short (a few cm) 50 Ω line. From a noise point of view, this design choice offers comparable performance as an active antenna with a long (~3 to 5m) cable attached to the application board by means of an SMA connector without the increased power consumption and BOM cost. If the goal is to protect the GNSS receiver in a noisy environment then an additional external SAW filter may be required. If a degradation in the C/No of 2 to 3dB (depending on the choice of the filter) is not acceptable for the application, then, to compensate for the filter losses and restore an adequate C/No level, an external LNA with good gain and low Noise Figure (see Table 23) is to be considered.

Table 22 lists examples of SAW filters suitable for the GNSS RF input of SARA-R510M8S modules.

Manufacturer	Part number	Description
Murata	SAFFB1G56AC0F0A	GPS / SBAS / QZSS / GLONASS / Galileo / BeiDou RF band-pass SAW filter with high attenuation in Cellular frequency ranges
Murata	SAFFB1G56AC0F7F	GPS / SBAS / QZSS / GLONASS / Galileo / BeiDou RF band-pass SAW filter with high attenuation in Cellular frequency ranges

Table 22: Examples of GNSS band-pass SAW filters

Table 23 lists examples of LNA suitable for the GNSS RF input of SARA-R510M8S modules.

Manufacturer	Part number	Comments
Maxim	MAX2659ELT+	Low noise figure, up to 10 dBm RF input power
JRC New Japan Radio	NJG1143UA2	Low noise figure, up to 15 dBm RF input power
NXP	BGU8006	Low noise figure, very small package size (WL-CSP)
Infineon	BGA524N6	Low noise figure, small package size

Table 23: Examples of GNSS Low Noise Amplifiers

Table 24 lists examples of ferrite beads suitable for the supply line of an external GNSS LNA.

Manufacturer	Part number	Comments
Murata	BLM15HD102SN1	High impedance at 1.575 GHz
Murata	BLM15HD182SN1	High impedance at 1.575 GHz
TDK	MMZ1005F121E	High impedance at 1.575 GHz
TDK	MMZ1005A121E	High impedance at 1.575 GHz

Table 24: Examples of ferrite beads for the supply line of external GNSS Low Noise Amplifiers

Table 25 lists examples of passive antennas to be used with SARA-R510M8S modules.

Manufacturer	Part number	Product name	Description
Tallysman	TW3400P		Passive antenna GPS / SBAS / QZSS / GLONASS
Tallysman	TW3710P		Passive antenna GPS / SBAS / QZSS / GLONASS / Galileo / BeiDou
Taoglas	CGGBP.35.3.A.02		Ceramic patch antenna GPS / SBAS / QZSS / GLONASS / Galileo / BeiDou
Taoglas	CGGBP.18.4.A.02		Embedded patch antenna GPS / SBAS / QZSS / GLONASS / Galileo / BeiDou
Inpaq	PA1590MF6G		Patch antenna GPS / SBAS / QZSS / GLONASS
Yageo	ANT2525B00BT1516S		Ceramic patch antenna GPS / SBAS / QZSS / GLONASS
Antenova	SR4G008	Sinica	Ultra-low profile patch antenna GPS / SBAS / QZSS / GLONASS / Galileo / BeiDou
Amotech	A18-4T		Ceramic patch antenna GPS / SBAS / QZSS / GLONASS / BeiDou
Amotech	A25-4T		Ceramic patch antenna GPS / SBAS / QZSS / BeiDou

Table 25: Examples of GNSS passive antennas

2.4.3.2 Guidelines for applications with an active antenna

Active antennas offer higher gain and better overall performance compared with passive antennas (without additional external SAW filter and LNA). However, the integrated low-noise amplifier contributes an additional current of typically 5 to 20 mA to the system's power consumption budget.

Active antennas for GNSS applications are usually powered through a DC bias on the RF cable. A simple bias-T, as shown in Figure 44, can be used to add this DC current to the RF signal line. The inductance L is responsible for isolating the RF path from the DC path. It should be selected to offer high impedance (greater than 500 Ω) at L-band frequencies. A series current limiting resistor is required to prevent short circuits destroying the bias-t inductor.

To avoid damaging the bias-T series inductor in the case of a short circuit at the antenna connector, it is recommended to implement a proper over-current protection circuit, which may consist in a series resistor as in the example illustrated in Figure 44. Component values are calculated according to the characteristics of the active antenna and the related supply circuit in use: the value of R_{bias} is calculated such that the maximum current capacity of the inductor L is never exceeded. Moreover R_{bias} and C form a low pass filter to remove high frequency noise from the DC supply. Assuming VCC_ANT=3.3 V, Table 26 reports suggested components for the circuit in Figure 44.

The recommended bias-t inductor (Murata LQW15ANR12J00) has a maximum current capacity of 110 mA. Hence the current is limited to 100 mA by way of a 33 ohm bias resistor. This resistor power rating must be chosen to ensure reliability in the chosen circuit design.

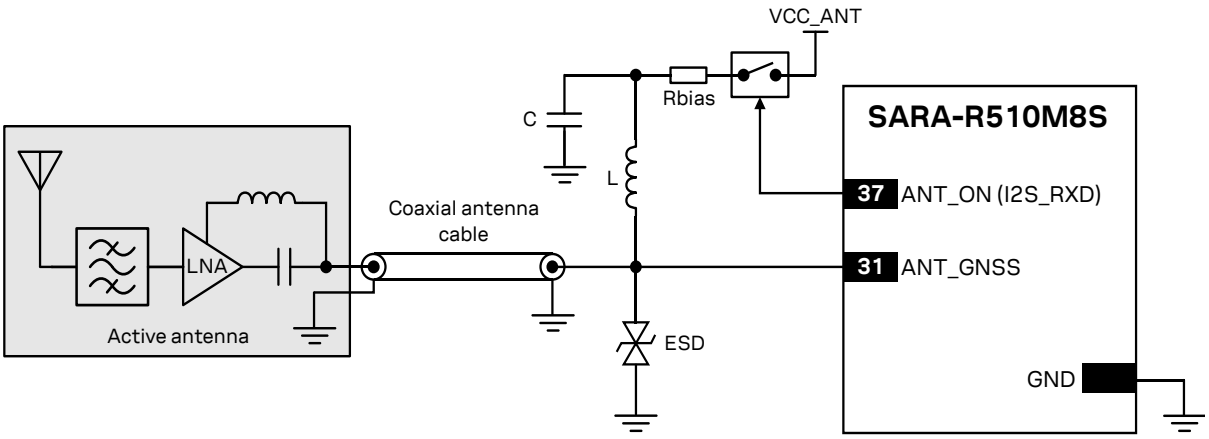

Figure 44: Typical circuit with active antenna connected to GNSS RF interface of SARA-R510M8S, using an external supply

Reference	Description	Part number – Manufacturer
L	120 nH wire-wound RF Inductor 0402 5% 110 mA	LQW15ANR12J00 – Murata
C	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
Rbias	33 ohm resistor 0.5W	Various manufacturers

Table 26: Example component values for active antenna biasing

☞ Refer to the antenna data sheet and/or manufacturer for proper values of the supply voltage VCC_ANT, inductance L and capacitance C.

☞ ESD sensitivity rating of the **ANT_GNSS** RF input pin is 1 kV (HBM according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board. Higher protection level can be achieved by mounting an ultra-low capacitance (i.e. less than 1 pF) ESD protection (see Table 27) close to accessible point.

Table 27 lists examples of ESD protection suitable for the GNSS RF input of SARA-R510M8S.

Manufacturer	Part number	Description
ON Semiconductor	ESD9R3.3ST5G	ESD protection diode with ultra-low capacitance (0.5 pF)
Infineon	ESD5V3U1U-02LS	ESD protection diode with ultra-low capacitance (0.4 pF)
Littelfuse	PESD0402-140	ESD protection diode with ultra-low capacitance (0.25 pF)

Table 27: Examples of ultra-low capacitance ESD protections

Table 28 lists examples of active antennas to be used with SARA-R510M8S modules.

Manufacturer	Part number	Product name	Description
Tallysman	TW3400 – TW3402		Active antenna, 2.5 – 16 V GPS / SBAS / QZSS / GLONASS
Tallysman	TW3710 – TW3712		Active antenna, 2.5 – 16 V GPS / SBAS / QZSS / GLONASS / Galileo / BeiDou
Taoglas	AA.162.301111	Ulysses	Ultra-Low profile miniature antenna, 1.8 – 5.5V GPS / SBAS / QZSS / GLONASS / Galileo
Taoglas	MA310.A.LB.001		Magnet mount antenna, 1.8 – 5.5 V GPS / SBAS / QZSS / GLONASS
Taoglas	ASGGB254.A - ASGGB184.A		Active GNSS surface-mount patch antenna, 1.8 – 5.5 V GPS / SBAS / QZSS / GLONASS / BeiDou / Galileo
Taoglas	AGGBP.SL.25A – AGGBP.SL.18A		Active GNSS surface-mount patch antenna, 1.8 – 5.5 V GPS / SBAS / QZSS / GLONASS / BeiDou / Galileo
Inpaq	B3G02G-S3-01-A		SMA plug active antenna, 3.3 V typical GPS / SBAS / GLONASS
Inpaq	GPSH237N-N3-37-A		Patch circular antenna, 3.0 V typical GPS / SBAS / QZSS
Abracon LLC	APAMP-110		Module RF antenna 5dBic SMA adhesive, 2.5 – 3.5 V GPS / SBAS / QZSS
TE Connectivity	2195768-1		Active antenna, 3.0 V typical GPS / SBAS / QZSS
Amotech	AGA151502-S0		Active antenna, 3.0 V typical GPS / SBAS / QZSS / GLONASS
Amotech	AGA393914-S0-A6		Active antenna, IP66, 5V typical GPS / SBAS / QZSS / GLONASS / BeiDou

Table 28: Examples of GNSS active antennas

2.4.4 Cellular and GNSS RF coexistence

Overview

Desensitization or receiver blocking is a form of electromagnetic interference where a radio receiver is unable to detect a weak signal that it might otherwise be able to receive when there is no interference (see Figure 45). Good blocking performance is particularly important in the scenarios where a number of radios of various forms are used in close proximity to each other.

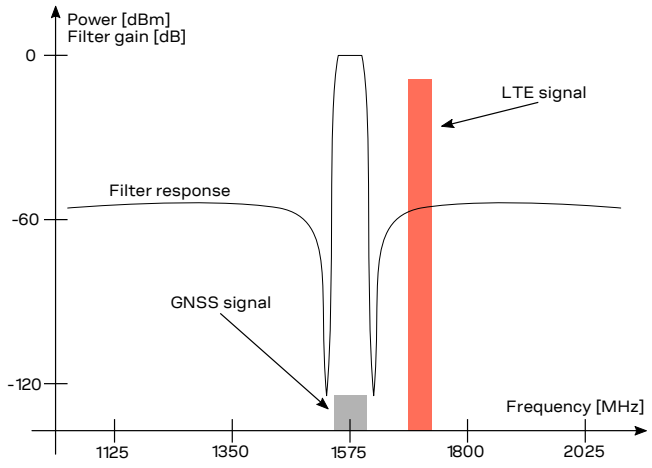

Figure 45: Interference due to transmission in LTE B3, B4 and B66 low channels (1710 MHz) adjacent to GNSS frequency range (1561 to 1605 MHz). Harmonics due to transmission in LTE B13 high channels (787 MHz) may fall into the GNSS bands

Jamming signals may come from in-band and out-band frequency sources. In-band jamming is caused by signals with frequencies falling within the GNSS frequency range, while out-band jamming is caused by very strong signals with frequencies adjacent to the GNSS frequency range so that part of the strong signal power may leak at the input of the GNSS receiver and/or block GNSS reception.

If not properly taken into consideration, in-band and out-band jamming signals may cause a reduction in the carrier-to-noise power density ratio (C/No) of the GNSS satellites.

In-band interference

In-band interference signals are typically caused by harmonics from displays, switching converters, micro-controllers and bus systems. Moreover, considering for example the LTE band 13 high channel transmission frequency (787 MHz) and the GPS operating band (1575.42 MHz ± 1.023 MHz), the second harmonic of the cellular signal is exactly within the GPS operating band. Therefore, depending on the board layout and the transmit power, the highest channel of LTE band 13 is the channel that has the greatest impact on the C/No reduction.

Countermeasures against in-band interference include:

- maintaining a good grounding concept in the design
- ensuring proper shielding of the different RF paths
- ensuring proper impedance matching of RF traces
- placing the GNSS antenna away from noise sources
- add a notch filter along the GNSS RF path, just after the antenna, at the frequency of the jammer (for example, as depicted in Figure 46, a simple notch filter can be reralized by the series connection of a discrete capacitor and inductor)

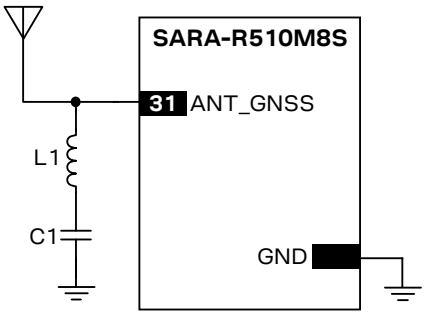

Figure 46: Simple notch filter for improved out-of-band jamming immunity against a single jamming frequency

With reference to Figure 46, a simple notch filter can be realized by the series connection of an inductor and capacitor. Capacitor C1 and inductor L1 values are calculated according to the formula:

$$f = \frac{1}{2\,\pi\,\sqrt{C \cdot L}}$$

For example, a notch filter at ~787 MHz improves the GNSS immunity to LTE band 13 high channel. Suitable component nominal values are C1 = 3.3 pF and L1 = 12 nH, with tolerance less than or equal to 2 % to ensure adequate notch frequency accuracy.

Out-of-band interference

Out-band interference is caused by signal frequencies that are different from the GNSS, the main sources being cellular, Wi-Fi, bluetooth transmitters, etc. For example, the lowest channels in LTE band 3, 4 and 66 can compromise the good reception of the GLONASS satellites. Again, the effect can be explained by comparing the LTE frequencies (low channels transmission frequency is 1710 MHz) with the GLONASS operating band (1602 MHz ± 8 MHz). In this case the LTE signal is outside the useful GNSS band, but, provided that the power received by the GNSS subsystem at 1710 MHz is high enough, blocking and leakage effects may appear reducing once again the C/No.

Countermeasures against out-band interference include:

- maintaining a good grounding concept in the design
- keeping the GNSS and cellular antennas more than the quarter-wavelength (of the minimum Tx frequency) away from each other. If for layout or size reasons this requirement cannot be met, then the antennas should be placed orthogonally to each other and/or on different side of the PCB.
- selecting a cellular antenna providing the worst possible return loss / VSWR / efficiency figure in the GNSS frequency band: the lower is the cellular antenna efficiency between 1575 MHz and 1610 MHz, the higher is the isolation between the cellular and the GNSS systems
- ensuring at least 15 – 20 dB isolation between antennas in the GNSS band by implementing the most suitable placement for the antennas, considering in particular the related radiation diagrams of the antennas: better isolation results from antenna patterns with radiation lobes in different directions considering the GNSS frequency band.
- adding a GNSS pass-band SAW filter along the GNSS RF line, providing very large attenuation in the cellular frequency bands (see Table 22 for possible suitable examples). It has to be noted that, as shown in Figure 3, a SAW filter and an LNA are already integrated in the GNSS RF path of the SARA-R510M8S: the addition of an external filter along the GNSS RF line has to be considered only if the conditions above cannot be met.

Additional countermeasures

In case all the aforementioned countermeasures cannot be implemented, adding a GNSS stop-band SAW filter along the cellular RF line may be considered. The filter shall provide very low attenuation in the cellular frequency bands (see Table 29 for possible suitable examples). It has to be noted that the addition of an external filter along the cellular RF line has to be carefully evaluated, considering that the additional insertion loss of such filter may affect the cellular TRP and/or TIS RF figures.

Table 29 lists examples of GNSS band-stop SAW filters that may be considered for the cellular RF input/output in case enough isolation between the cellular and the GNSS RF systems cannot be provided by proper selection and placement of the antennas beside other proper RF design solutions.

Manufacturer	Part number	Description
Qualcomm	B8636	GPS / SBAS / QZSS / GLONASS / Galileo / BeiDou RF band-stop SAW filter with low attenuation in Cellular frequency ranges
Qualcomm	B8666	GPS / SBAS / QZSS / GLONASS / Galileo / BeiDou RF band-stop SAW filter with low attenuation in Cellular frequency ranges

Table 29: Examples of GNSS band-stop SAW filters

Additional considerations

As far as Tx power is concerned, SARA-R5 series modules maximum output power during LTE transmission is 23 dBm. High-power transmission occurs very infrequently: typical output power values are in the range of -3 to 0 dBm (see Figure 1 in the GSMA official document TS.09 [11]). Therefore, depending on the application, careful PCB layout, antenna selection and placement should be sufficient to ensure accurate GNSS reception.

For an example of vehicle tracking application in a small form factor featuring cellular and short-range connectivity alongside a multi-constellation GNSS receiver, with successful RF coexistence between the systems, refer to the u-blox B36 vehicle tracking blueprint [17]. The distance between the cellular and GNSS antennas for the u-blox B36 blueprint is annotated in Figure 47.

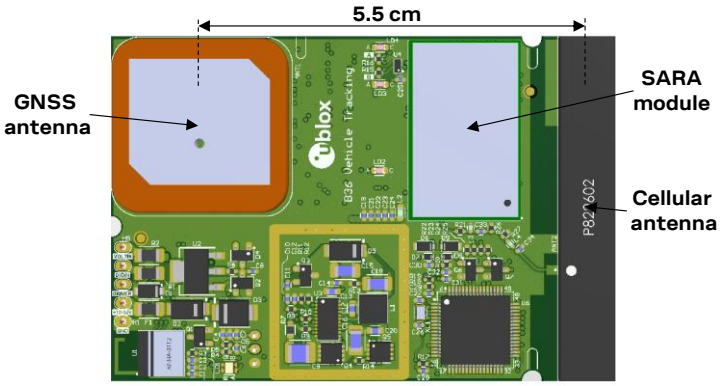

Figure 47: PCB top rendering for the u-blox B36 blueprint with annotated distance between cellular and GNSS antennas

☞ For additional information and guidelines regarding the GNSS design, see the SARA-R5 / SARA-R4 positioning and timing implementation application note [18].

2.4.5 Cellular antenna detection interface (ANT_DET)

2.4.5.1 Guidelines for ANT_DET circuit design

Figure 48 and Table 30 describe the recommended schematic / components for the cellular antenna detection circuit to be provided on the application board and for the diagnostic circuit that must be provided on the antenna's assembly to achieve antenna detection functionality.

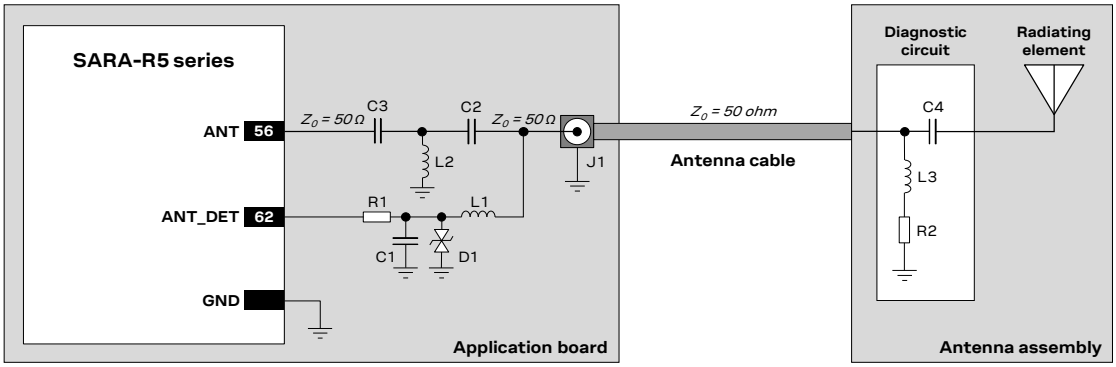

Figure 48: Suggested schematic for antenna detection circuit on application PCB and diagnostic circuit on antenna assembly

Reference	Description	Part number – Manufacturer
C1	27 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H270JA16 – Murata
C2	33 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H330JA16 – Murata
D1	Very low capacitance ESD protection	PESD0402-140 – Tyco Electronics
L1	68 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 – Murata
R1	10 kΩ resistor 0402 1% 0.063 W	Generic manufacturer
J1	SMA connector 50 Ω through hole jack	SMA6251A1-3GT50G-50 – Amphenol
C3	15 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H150J – Murata
L2	39 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HN39NJ02 – Murata
C4	22 pF capacitor Ceramic C0G 0402 5% 25 V	GCM1555C1H270JA16 – Murata
L3	68 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 – Murata
R2	15 kΩ resistor for diagnostics	Generic manufacturer

Table 30: Suggested parts for antenna detection circuit on application PCB and diagnostic circuit on antennas assembly

The antenna detection and diagnostic circuit suggested in Figure 48 and Table 30 are here explained:

- When antenna detection is forced by the +UANTR AT command (see the SARA-R5 series AT commands manual [1]), the **ANT_DET** pin generates a DC current measuring the resistance (R2) from the antenna connector (J1) provided on the application board to GND.
- DC blocking capacitors are needed at the **ANT** pin (C2) and at the antenna radiating element (C4) to decouple the DC current generated by the **ANT_DET** pin.
- Choke inductors with a Self-Resonance Frequency (SRF) in the range of 1 GHz are needed in series at the **ANT_DET** pin (L1) and in series at the diagnostic resistor (L3), to avoid a reduction of the RF performance of the system, improving the RF isolation of the load resistor.
- Resistor on the **ANT_DET** path (R1) is needed for accurate measurements through the +UANTR AT command. It also acts as an ESD protection.
- Additional components (C1 and D1 in Figure 48) are needed at the **ANT_DET** pin as ESD protection.
- Additional high pass filter (C3 and L2 in Figure 48) is provided as ESD immunity improvement
- The **ANT** pin must be connected to the antenna connector by means of a transmission line with nominal characteristics impedance as close as possible to 50 Ω.

The DC impedance at RF port for some antennas may be a DC open (e.g. linear monopole) or a DC short to reference GND (e.g. PIFA antenna). For those antennas, without the diagnostic circuit of Figure 48, the measured DC resistance is always at the limits of the measurement range (respectively open or short), and there is no mean to distinguish between a defect on antenna path with similar characteristics (respectively: removal of linear antenna or RF cable shorted to GND for PIFA antenna).

Furthermore, any other DC signal injected to the RF connection from ANT connector to radiating element will alter the measurement and produce invalid results for antenna detection.

☞ It is recommended to use an antenna with a built-in diagnostic resistor in the range from 5 kΩ to 30 kΩ to assure good antenna detection functionality and avoid a reduction of module RF performance. The choke inductor should exhibit a parallel Self-Resonance Frequency (SRF) in the range of 1 GHz to improve the RF isolation of load resistor.

For example:

Consider an antenna with built-in DC load resistor of 15 kΩ. Using the +UANTR AT command, the module reports the resistance value evaluated from the antenna connector provided on the application board to GND:

- Reported values close to the used diagnostic resistor nominal value (i.e. values from 13 kΩ to 17 kΩ if a 15 kΩ diagnostic resistor is used) indicate that the antenna is correctly connected.
- Values close to the measurement range maximum limit or an open-circuit “over range” report (see the SARA-R5 series AT commands manual [2]) means that the antenna is not connected or the RF cable is broken.
- Reported values below the measurement range minimum limit highlights a short to GND at antenna or along the RF cable.
- Measurement inside the valid measurement range and outside the expected range may indicate an unclean connection, a damaged antenna or incorrect value of the antenna load resistor for diagnostics.
- Reported value could differ from the real resistance value of the diagnostic resistor mounted inside the antenna assembly due to antenna cable length, antenna cable capacity and the used measurement method.

☞ If the antenna detection function is not required by the customer application, the **ANT_DET** pin can be left not connected and the **ANT** pin can be directly connected to the antenna connector by means of a 50 Ω transmission line as described in Figure 35.

2.4.5.2 Guidelines for ANT_DET layout design

Figure 49 describes the recommended layout for the cellular antenna detection circuit to be provided on the application board to achieve antenna detection functionality, implementing the recommended schematic described in the previous Figure 48 and Table 30:

- The **ANT** pin must be connected to the cellular antenna connector by means of a 50 Ω transmission line, implementing the design guidelines described in section 2.4.2 and the recommendations of the SMA connector manufacturer.
- DC blocking capacitor at **ANT** pin (C2) must be placed in series to the 50 Ω RF line.
- The **ANT_DET** pin must be connected to the 50 Ω transmission line by means of a sense line.
- Choke inductor in series at the **ANT_DET** pin (L1) must be placed so that one pad is on the 50 Ω transmission line and the other pad represents the start of the sense line to the **ANT_DET** pin.
- The additional components (R1, C1, D1) on the **ANT_DET** line must be placed as ESD protection
- The additional high pass filter (C3 and L2) on the **ANT** line is placed as ESD immunity improvement

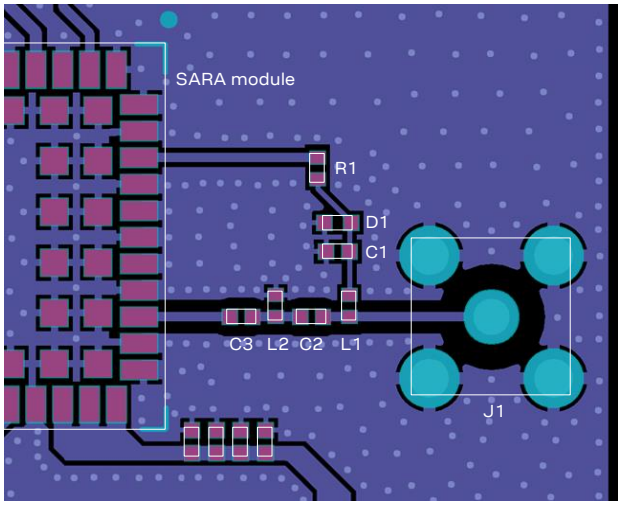

Figure 49: Suggested layout for antenna detection circuit on application board

2.4.6 Cellular antenna dynamic tuning control interface

SARA-R5 series modules support a wide range of frequencies, from 600 MHz to 2200 MHz. To provide more efficient antenna designs over a wide bandwidth, **I2S_TXD** and **I2S_WA** pins can be configured to change their output value in real time according to the operating LTE band in use by the module (see sections 1.12 and 2.9).

These pins, paired with an external antenna tuner IC or RF switch, can be used to:

- tune antenna impedance to reduce power losses due to mismatch
- tune antenna aperture to improve total antenna efficiency
- select the optimal antenna for each operating band

Table 31 reports the antenna dynamic tuning pins setting at the related module operating band.

I2S_TXD	I2S_WA	LTE frequency band in use
0	0	B71 (< 700 MHz)
0	1	B12, B13, B28, B85 (700..800 MHz)
1	0	B5, B8, B18, B19, B20, B26 (800..900 MHz)
1	1	B1, B2, B3, B4, B25, B66 (> 1000 MHz)

Table 31: SARA-R5 series modules antenna dynamic tuning truth table

Figure 50 shows the example application circuits implementing impedance tuning and aperture tuning. The module controls an RF switch which is responsible for selecting the appropriate matching element for the operating band. Table 32 reports suggested components implementing the SP4T RF switch functionality.

In Figure 50(a), tuning the antenna impedance optimizes the power delivered into the antenna by dynamically adjusting the RF impedance seen by **ANT** pin of SARA-R5 series module. By creating a tuned matching network for each operating band, the total radiated power (TRP) and the total isotropic sensitivity (TIS) metrics are improved.

In Figure 50(b), antenna aperture tuning enables higher antenna efficiency over a wide frequency range. The dynamically tunable components are added to the antenna structure itself, thereby modifying the effective electrical length of the radiating element. Thus the resonant frequency of the antenna is shifted into the module's operating frequency band. Aperture tuning optimizes radiation efficiency, insertion loss, isolation, and rejection levels of the antenna.

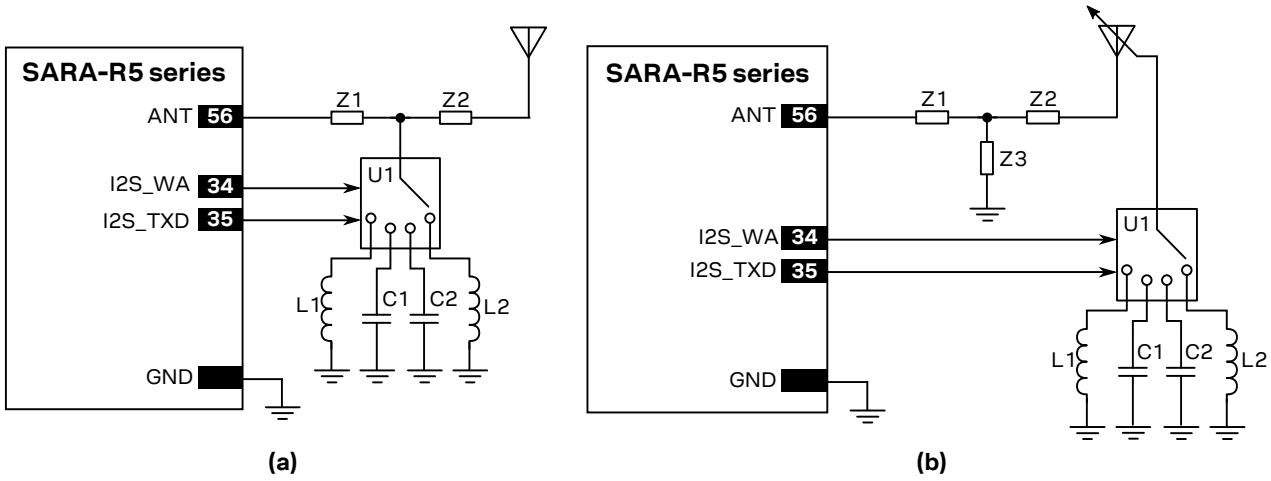

Figure 50: Examples of schematics for cellular antenna dynamic impedance tuning (a) and aperture tuning (b).

☞ Refer to the antenna datasheet and/or manufacturer for proper values of matching components Z1, Z2, Z3, L1, L2, C1, C2. These components should have low losses to avoid degrading the radiating efficiency of the antenna, thereby hindering the positive effects of dynamic tuning.

Manufacturer	Part number	Description
Peregrine Semiconductor	PE42442	30..6000 MHz UltraCMOS SP4T RF switch
Peregrine Semiconductor	PE613050	5..3000 MHz UltraCMOS SP4T RF switch
Peregrine Semiconductor	PE42440	50..3000 MHz UltraCMOS SP4T RF switch
Skyworks Solutions	SKY13626-685LF	400..3800 MHz SP4T high-power RF switch
Skyworks Solutions	SKY13380-350LF	20..3000 MHz SP4T high-power RF switch
AVX / Ethertronics	EC646	100..3000 MHz ultra-small SP4T RF switch
AVX / Ethertronics	EC686-3	100..3000 MHz ultra-low R_{ON} SP4T RF switch
Qorvo	RF1654A	100..2700 MHz SP4T RF switch

Table 32: Examples of RF switches for cellular antenna dynamic tuning

2.5 SIM interface

2.5.1 Guidelines for SIM circuit design

2.5.1.1 Guidelines for SIM cards, SIM connectors and SIM chips selection

The ISO/IEC 7816, the ETSI TS 102 221 and the ETSI TS 102 671 specifications define the physical, electrical and functional characteristics of Universal Integrated Circuit Cards (UICC), which contains the Subscriber Identification Module (SIM) integrated circuit that securely stores all the information needed to identify and authenticate subscribers over the LTE network.

Removable UICC / SIM card contacts mapping is defined by ISO/IEC 7816 and ETSI TS 102 221 as follows:

- Contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Contact C4 = AUX1 (Auxiliary contact) → It must be left not connected
- Contact C5 = GND (Ground) → It must be connected to **GND**
- Contact C6 = VPP/SWP (Other function) → It can be left not connected
- Contact C7 = I/O (Data input/output) → It must be connected to **SIM_IO**
- Contact C8 = AUX2 (Auxiliary contact) → It must be left not connected

A removable SIM card can have 6 contacts (C1, C2, C3, C5, C6, C7) or 8 contacts, also including the auxiliary contacts C4 and C8. Only 5 contacts are required and must be connected to the module SIM interface.

Removable SIM cards are suitable for applications requiring a change of SIM card during the product lifetime.

A SIM card holder can have 6 or 8 positions if a mechanical card presence detector is not provided, or it can have 6+2 or 8+2 positions if two additional pins relative to the normally-open mechanical switch integrated in the SIM connector for the mechanical card presence detection are provided. Select a SIM connector providing 6+2 or 8+2 positions if the optional SIM detection feature is required by the custom application, otherwise a connector without integrated mechanical presence switch can be selected.

Surface-Mounted UICC / SIM chip contact mapping (M2M UICC Form Factor) is defined by the ETSI TS 102 671 as:

- Case pin 8 = UICC contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Case pin 7 = UICC contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Case pin 6 = UICC contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Case pin 5 = UICC contact C4 = AUX1 (Aux. contact) → It must be left not connected
- Case pin 1 = UICC contact C5 = GND (Ground) → It must be connected to **GND**
- Case pin 2 = UICC contact C6 = VPP/SWP (Other) → It can be left not connected
- Case pin 3 = UICC contact C7 = I/O (Data I/O) → It must be connected to **SIM_IO**
- Case pin 4 = UICC contact C8 = AUX2 (Aux. contact) → It must be left not connected

A Surface-Mounted SIM chip has 8 contacts and can also include the auxiliary contacts C4 and C8 for other uses, but only 6 contacts are required and must be connected to the module SIM card interface as described above.

Surface-Mounted SIM chips are suitable for M2M applications where it is not required to change the SIM once installed.

2.5.1.2 Guidelines for single SIM card connection without detection

A removable SIM card placed in a SIM card holder must be connected to the SIM card interface of SARA-R5 series modules as described in Figure 51, where the optional SIM detection feature is not implemented.

Follow these guidelines to connect the module to a SIM connector without SIM presence detection:

- Connect the UICC / SIM contact C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) on SIM supply line, close to the relative pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GCM1555C1H470JA16) on each SIM line, very close to each related pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 – 30 cm from the SIM card holder.
- Provide a very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco PESD0402-140) on each externally accessible SIM line, close to each relative pad of the SIM connector. ESD sensitivity rating of the SIM interface pins is 1 kV (HBM). So that, according to EMC/ESD requirements of the custom application, higher protection level can be required if the lines are externally accessible on the application device.
- Limit capacitance and series resistance on each SIM signal to match the requirements for the SIM interface regarding maximum allowed rise time on the lines.

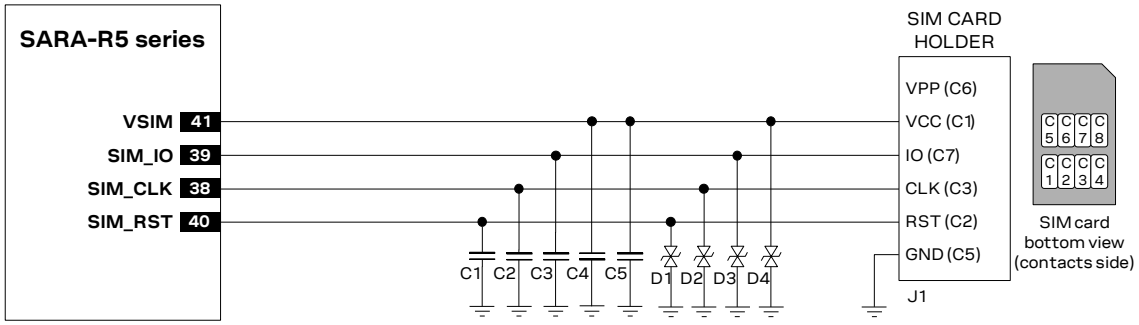

Figure 51: Application circuit for the connection to a single removable SIM card, with SIM detection not implemented

Reference	Description	Part number – Manufacturer
C1, C2, C3, C4	47 pF capacitor ceramic C0G 0402 5% 50 V	GCM1555C1H470JA16 – Murata
C5	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
D1, D2, D3, D4	Very low capacitance ESD protection	PESD0402-140 – Tyco Electronics
J1	SIM card holder, 6 positions, without card presence switch	Generic manufacturer, as C707 10M006 136 2 – Amphenol

Table 33: Example of components for the connection to a single removable SIM card, with SIM detection not implemented

2.5.1.3 Guidelines for single SIM chip connection

A Surface-Mounted SIM chip (M2M UICC form factor) must be connected to the SIM card interface of the SARA-R5 series modules as described in Figure 52.

Follow these guidelines to connect the module to a Surface-Mounted SIM chip without SIM presence detection:

- Connect the UICC / SIM contact C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line close to the relative pad of the SIM chip, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GCM1555C1H470JA16) on each SIM line, to prevent RF coupling especially in case the RF antenna is placed closer than 10 – 30 cm from the SIM lines.
- Limit capacitance and series resistance on each SIM signal to match the requirements for the SIM interface regarding maximum allowed rise time on the lines.

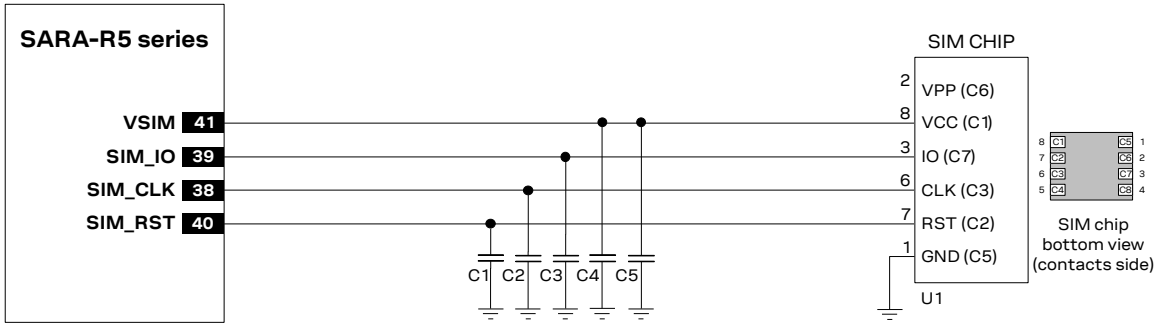

Figure 52: Application circuits for the connection to a single Surface-Mounted SIM chip, with SIM detection not implemented

Reference	Description	Part number – Manufacturer
C1, C2, C3, C4	47 pF capacitor ceramic C0G 0402 5% 50 V	GCM1555C1H470JA16 – Murata
C5	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
U1	SIM chip (M2M UICC form factor)	Generic manufacturer

Table 34: Example of components for the connection to a single SMD SIM chip, with SIM detection not implemented

2.5.1.4 Guidelines for single SIM card connection with detection

An application circuit for the connection to a single removable SIM card placed in a SIM card holder is described in Figure 53, where the optional SIM card detection feature is implemented.

Follow these guidelines connecting the module to a SIM connector implementing SIM presence detection:

- Connect the UICC / SIM contact C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.

- Connect one pin of the normally-open mechanical switch integrated in the SIM connector (as the SW2 pin in Figure 53) to the **GPIO5** input pin, providing a weak pull-down resistor (e.g. 470 kΩ, as R2 in Figure 53).
- Connect the other pin of the normally-open mechanical switch integrated in the SIM connector (SW1 pin in Figure 53) to **V_INT** 1.8 V supply output by means of a strong pull-up resistor (e.g. 1 kΩ, as R1 in Figure 53)
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**), close to the related pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GCM1555C1H470JA16) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), very close to each related pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 – 30 cm from the SIM card holder.
- Provide a low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco Electronics PESD0402-140) on each externally accessible SIM line, close to each related pad of the SIM connector. The ESD sensitivity rating of SIM interface pins is 1 kV (HBM according to JESD22-A114), so that, according to the EMC/ESD requirements of the custom application, higher protection level can be required if the lines are externally accessible.
- Limit capacitance and series resistance on each SIM signal to match the requirements for the SIM interface regarding maximum allowed rise time on the lines.

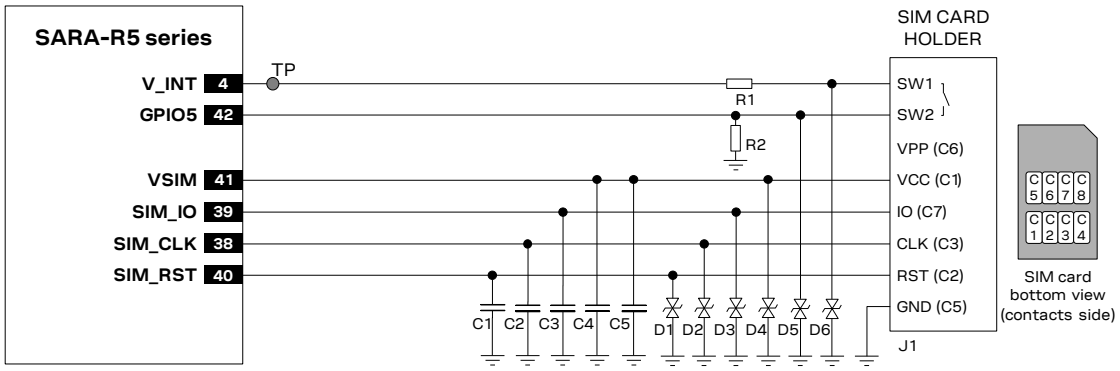

Figure 53: Application circuit for the connection to a single removable SIM card, with SIM detection implemented

Reference	Description	Part number – Manufacturer
C1, C2, C3, C4	47 pF capacitor ceramic C0G 0402 5% 50 V	GCM1555C1H470JA16 – Murata
C5	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
D1 – D6	Very low capacitance ESD protection	PESD0402-140 – Tyco Electronics
R1	1 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R2	470 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
J1	SIM card holder, 6 + 2 positions, with card presence switch	Generic manufacturer, as CCM03-3013LFT R102 – C&K Components

Table 35: Example of components for the connection to a single removable SIM card, with SIM detection implemented

2.5.2 Guidelines for SIM layout design

The layout of the SIM card interface lines (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**) may be critical if the SIM card is placed far away from the SARA-R5 series modules or in close proximity to the cellular antenna (and/or GNSS antenna, for SARA-R510M8S modules): these two cases should be avoided or at least mitigated as described below.

In the first case, the long connection can cause the radiation of some harmonics of the digital data frequency as any other digital interface. It is recommended to keep the traces short and avoid coupling with RF lines or sensitive analog inputs.

In the second case, the same harmonics can be picked up and create self-interference that can reduce the sensitivity of LTE receiver channels (and/or GNSS channels, for SARA-R510M8S modules) whose carrier frequency is coincidental with harmonic frequencies. It is strongly recommended to place the RF bypass capacitors suggested in Figure 51, Figure 52, and Figure 53 near the SIM connector.

In addition, since the SIM card is typically accessed by the end user, it can be subjected to ESD discharges. Add adequate ESD protection as suggested to protect module SIM pins near the SIM connector.

Limit capacitance and series resistance on each SIM signal to match the SIM specifications. The connections should always be kept as short as possible.

Avoid coupling with any sensitive analog circuit, since the SIM signals can cause the radiation of some harmonics of the digital data frequency.

2.6 Data communication interfaces

2.6.1 UART interfaces

2.6.1.1 Guidelines for UART circuit design

Providing 1 UART with the full RS-232 functionality (using the complete V.24 link)

☞ Compatible with USIO variant 1; not compatible with USIO variants 0 / 2 / 3 / 4 (see section 1.9.1.1).

If RS-232 compatible signal levels are needed, two different external voltage translators (e.g. Maxim MAX3237E and Texas Instruments SN74AVC4T774) can be used. The Texas Instruments chips provide the translation from 1.8 V to 3.3 V, while the Maxim chip provides the translation from 3.3 V to RS-232 compatible signal level.

If a 1.8 V application processor (DTE) is used and complete RS-232 functionality is required, then the complete 1.8 V UART of the module (DCE) should be connected to a 1.8 V DTE, as in Figure 54.

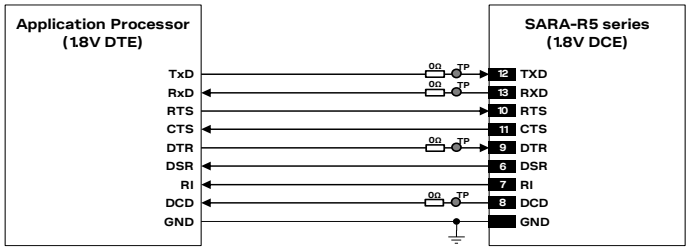

Figure 54: 1 UART interface application circuit with complete V.24 link in DTE/DCE serial communication (1.8 V DTE)

If a 3.0 V application processor (DTE) is used, then it is recommended to connect the 1.8 V UART of the module (DCE) by means of appropriate unidirectional voltage translators using the module V_INT output as 1.8 V supply for the voltage translators on the module side, as described in Figure 55.

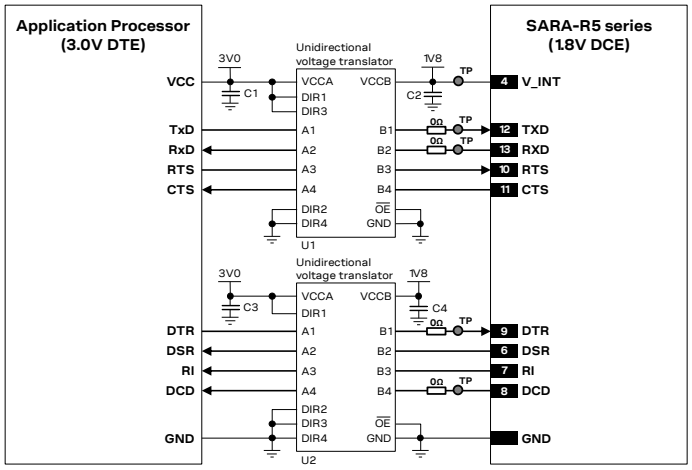

Figure 55: 1 UART interface application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part number – Manufacturer
C1, C2, C3, C4	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
U1, U2	Unidirectional voltage translator	SN74AVC4T774 [13] - Texas Instruments

Table 36: Components for 1 UART application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

☞ Provide accessible test points directly connected to **TXD** and **RXD** pins for FW update purpose and to **DCD** and **DTR** pins for diagnostic purposes.

[13] Voltage translator providing partial power down feature, so the 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing 1 UART with the TXD, RXD, RTS, CTS, DTR and RI lines only

☞ Compatible with USIO variants 0/1; not compatible with USIO variants 2/3/4 (see section 1.9.1.1).

If the functionality of the **DSR** and **DCD** lines is not required, or the lines are not available:

- Leave **DSR** and **DCD** lines of the module unconnected and floating

If RS-232 compatible signal levels are needed, two different external voltage translators (e.g. Maxim MAX3237E and Texas Instruments SN74AVC4T774) can be used. The Texas Instruments chips provide the translation from 1.8 V to 3.3 V, while the Maxim chip provides the translation from 3.3 V to RS-232 compatible signal level.

Figure 56 describes the circuit that should be implemented if a 1.8 V application processor (DTE) is used, given that the DTE will behave correctly regardless of the **DSR** input setting.

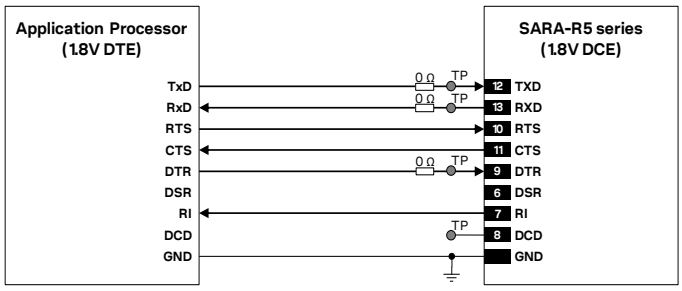

Figure 56: 1 UART interface application circuit with 7-wire link in DTE/DCE serial communication (1.8 V DTE)

If a 3.0 V application processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module V_INT output as 1.8 V supply for the voltage translators on the module side, as described in Figure 57, given that the DTE will behave correctly regardless of the **DSR** input setting.

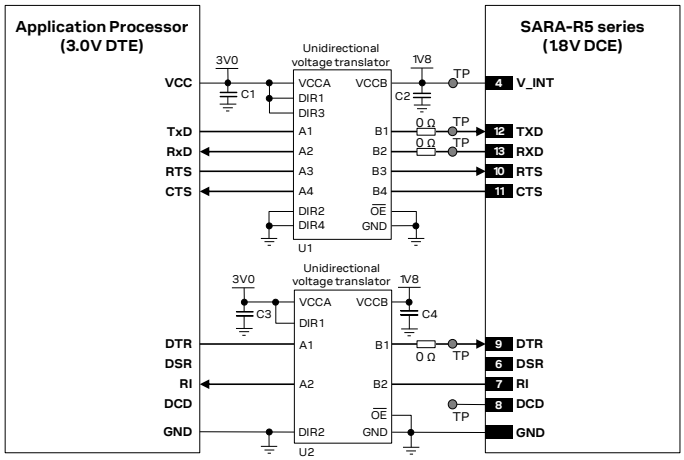

Figure 57: 1 UART interface application circuit with 7-wire link in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part number – Manufacturer
C1, C2, C3, C4	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
U1	Unidirectional voltage translator	SN74AVC4T774 [14] - Texas Instruments
U2	Unidirectional voltage translator	SN74AVC2T245 [14] – Texas Instruments

Table 37: Components for 1 UART application circuit with 7-wire link in DTE/DCE serial communication (3.0 V DTE)

☞ Provide accessible test points directly connected to **TXD** and **RXD** pins for FW update purpose and to **DCD** and **DTR** pins for diagnostic purposes.

[14] Voltage translator providing partial power down feature, so the 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing 1 UART with the TXD, RXD, RTS and CTS lines only

☞ Compatible with USIO variants 0/1/3; not compatible with USIO variants 2/4 (see section 1.9.1.1).

If the functionality of the **DSR**, **DCD**, **RI** and **DTR** lines is not required, or the lines are not available:

- Connect the **DTR** input to GND, as useful to have the greeting text presented over the UART
- Leave **DSR**, **DCD**, and **RI** lines of the module floating

If RS-232 compatible signal levels are needed, the Maxim MAX13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V application processor is used, the circuit should be implemented as described in Figure 58.

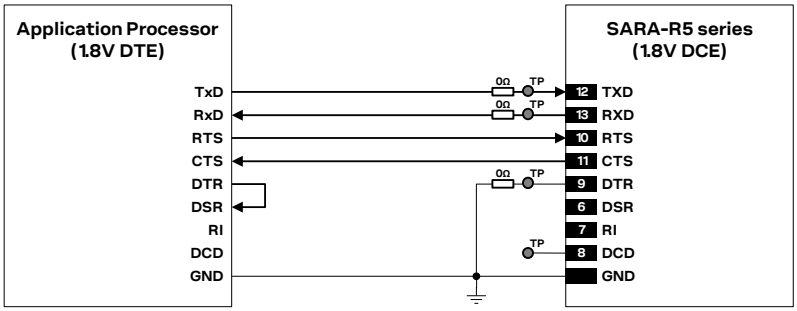

Figure 58: 1 UART interface application circuit with 5-wire link in DTE/DCE serial communication (1.8V DTE)

If a 3.0 V application processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of an appropriate unidirectional voltage translator using the module **V_INT** output as 1.8 V supply for the voltage translator on the module side, as in Figure 59.

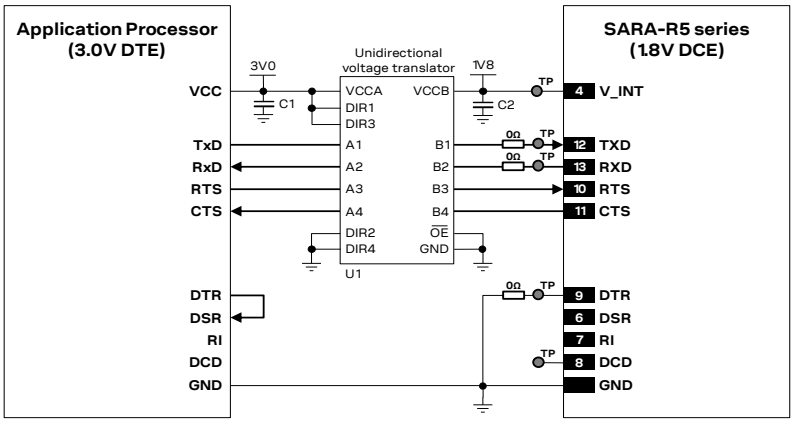

Figure 59: 1 UART interface application circuit with 5-wire link in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part number – Manufacturer
C1, C2	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
U1	Unidirectional voltage translator	SN74AVC4T774 [15] - Texas Instruments

Table 38: Components for 1 UART application circuit with 5-wire link in DTE/DCE serial communication (3.0 V DTE)

☞ Provide accessible test points directly connected to **TXD** and **RXD** pins for FW update purpose and to **DCD** and **DTR** pins for diagnostic purposes.

[15] Voltage translator providing partial power down feature, so the 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing 2 UARTs with the TXD, RXD, RTS and CTS lines only

☞ Compatible with USIO variants 2/3/4; not compatible with USIO variants 0/1 (see section 1.9.1.1).

If RS-232 compatible signal levels are needed, two Maxim MAX13234E voltage level translators can be used. These chips translate voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V application processor is used, the circuit should be implemented as described in Figure 60.

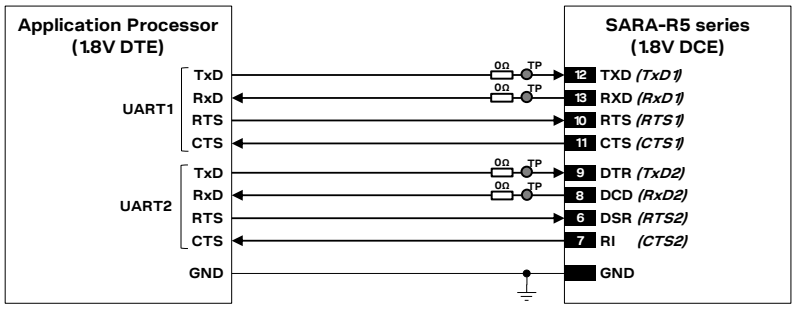

Figure 60: 2 UART interfaces application circuit with 5-wire links in DTE/DCE serial communications (1.8 V DTE)

If a 3.0 V application processor (DTE) is used, then it is recommended to connect the 1.8 V UART interfaces of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as in Figure 61.

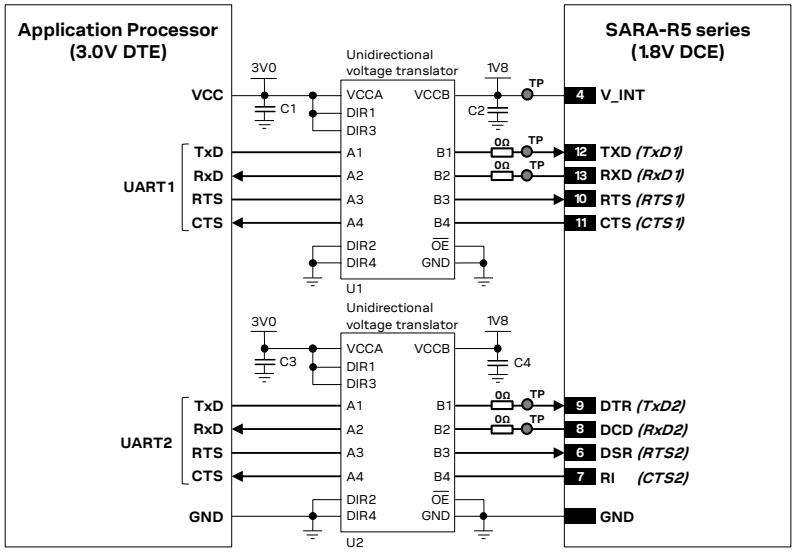

Figure 61: 2 UART interfaces application circuit with 5-wire links in DTE/DCE serial communications (3.0 V DTE)

Reference	Description	Part number – Manufacturer
C1, C2, C3, C4	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
U1, U2	Unidirectional voltage translator	SN74AVC4T774 [16] - Texas Instruments

Table 39: Components for 2 UARTs application circuit with 5-wire links in DTE/DCE serial communications (3.0 V DTE)

☞ Provide accessible test points directly connected to **TXD** and **RXD** pins for FW update purpose and to **DCD** and **DTR** pins for diagnostic purposes.

[16] Voltage translator providing partial power down feature, so the 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing 1 UART with the TXD and RXD lines only

☞ Compatible with USIO variants 0/1/3; not compatible with USIO variants 2/4 (see section 1.9.1.1).

☞ Providing the **TXD** and **RXD** lines only is not recommended if the multiplexer functionality is used in the application: providing also at least the HW flow control (**RTS** and **CTS** lines) is recommended, and it is in particular necessary if the low power mode is enabled by +UPSV AT command.

If the functionality of the **RTS**, **CTS**, **DTR**, **DSR**, **RI** and **DCD** lines is not required in the application, or the lines are not available, then:

- Connect the module **RTS** input line to GND or to the **CTS** output of the module, since the module requires **RTS** active (low electrical level) if HW flow control is enabled (as it is by default)
- Connect the **DTR** input to GND, as useful to have the greeting text presented over the UART
- Leave **DSR**, **RI** and **DCD** lines of the module floating

If RS-232 compatible signal levels are needed, the Maxim MAX13236E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V application processor (DTE) is used, the circuit should be implemented as in Figure 62.

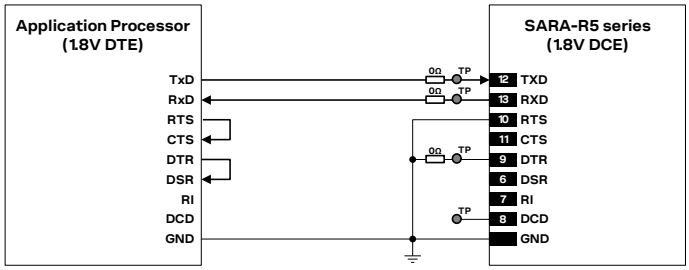

Figure 62: 1 UART interface application circuit with 3-wire link in DTE/DCE serial communication (1.8 V DTE)

If a 3.0 V application processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of an appropriate unidirectional voltage translator using the module **V_INT** output as 1.8 V supply for the voltage translator on the module side, as in Figure 63.

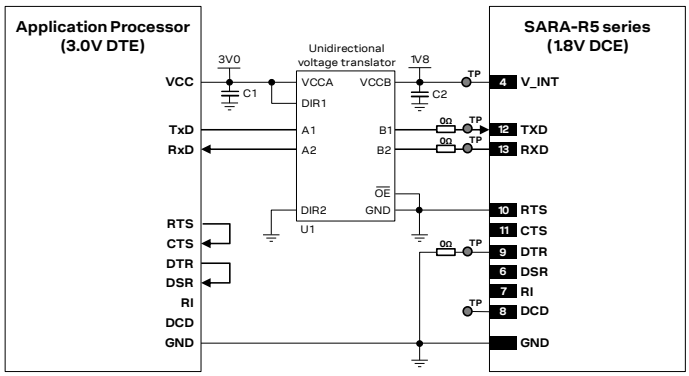

Figure 63: 1 UART interface application circuit with 3-wire link in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part number – Manufacturer
C1, C2	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
U1	Unidirectional voltage translator	SN74AVC2T245 [17] - Texas Instruments

Table 40: Components for 1 UART application circuit with 3-wire link in DTE/DCE serial communication (3.0 V DTE)

☞ Provide accessible test points directly connected to **TXD** and **RXD** pins for FW update purpose and to **DCD** and **DTR** pins for diagnostic purposes.

[17] Voltage translator providing partial power down feature, so the 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing 2 UARTs with the TXD and RXD lines only

☞ Compatible with USIO variants 2/3/4; not compatible with USIO variants 0/1 (see section 1.9.1.1).

☞ Providing the **TXD** and **RXD** lines only is not recommended if the multiplexer functionality is used in the application: providing also at least the HW flow control (**RTS** and **CTS** lines) is recommended, and it is in particular necessary if the low power mode is enabled by +UPSV AT command.

If the functionality of the **RTS**, **CTS**, **DSR** and **RI** lines is not required in the application, or the lines are not available, then:

- Connect the module **RTS** and **DSR** input lines to GND or respectively to the **CTS** and **RI** output of the module, since the module requires **RTS** and **DSR** active (low electrical level) if HW flow control is enabled (as it is by default)

If RS-232 compatible signal levels are needed, the Maxim MAX13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V application processor (DTE) is used, the circuit should be implemented as in Figure 64.

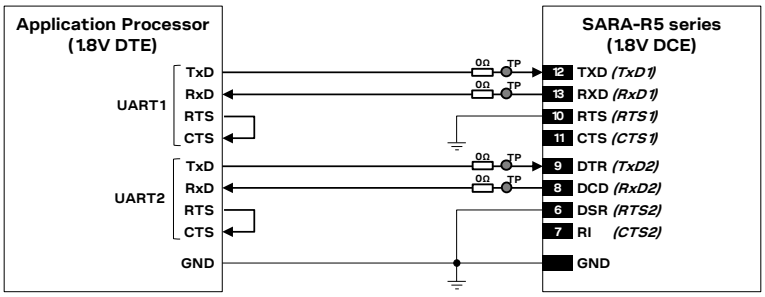

Figure 64: 2 UART interfaces application circuit with 3-wire links in DTE/DCE serial communications (1.8 V DTE)

If a 3.0 V application processor (DTE) is used, then it is recommended to connect the 1.8 V UART interfaces of the module (DCE) by means of an appropriate unidirectional voltage translator using the module **V_INT** output as 1.8 V supply for the voltage translator on the module side, as in Figure 63.

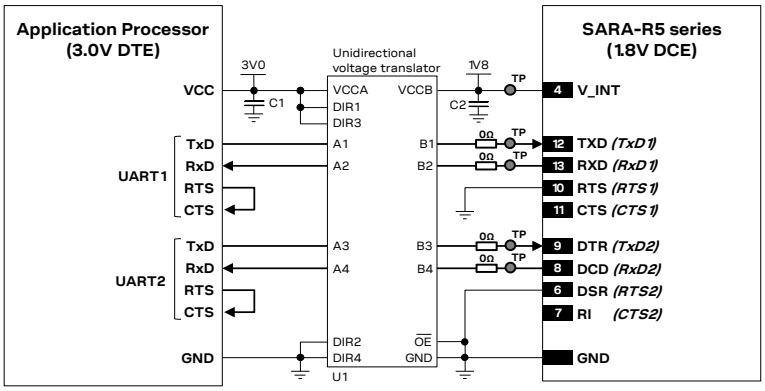

Figure 65: 2 UART interfaces application circuit with 3-wire links in DTE/DCE serial communications (3.0 V DTE)

Reference	Description	Part number – Manufacturer
C1, C2	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
U1	Unidirectional voltage translator	SN74AVC4T774 [18] - Texas Instruments

Table 41: Components for 2 UARTs application circuit with 3-wire links in DTE/DCE serial communications (3.0 V DTE)

☞ Provide accessible test points directly connected to **TXD** and **RXD** pins for FW update purpose and to **DCD** and **DTR** pins for diagnostic purposes.

[18] Voltage translator providing partial power down feature, so the 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Additional considerations

If a 3.0 V application processor (DTE) is used, the voltage scaling from any 3.0 V output of the DTE to the corresponding 1.8 V input of the module (DCE) can be implemented as an alternative low-cost solution, by means of an appropriate voltage divider. Consider the value of the pull-down / pull-up integrated at the input of the module (DCE) for the correct selection of the voltage divider resistance values. Make sure that any DTE signal connected to the module is tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the **V_INT** supply output of the module), to avoid latch-up of circuits and allow a clean boot of the module (see the remark below).

Moreover, the voltage scaling from any 1.8 V output of the cellular module (DCE) to the corresponding 3.0 V input of the application processor (DTE) can be implemented by means of an appropriate low-cost non-inverting buffer with open drain output. The non-inverting buffer should be supplied by the **V_INT** supply output of the cellular module. Consider the value of the pull-up integrated at each input of the DTE (if any) and the baud rate required by the application for the appropriate selection of the resistance value for the external pull-up biased by the application processor supply rail.

- It is highly recommended to provide accessible test points directly connected to the **TXD** and **RXD** pins for FW upgrade purposes and to **DCD** and **DTR** pins for diagnostic purposes, in particular providing a 0 Ω series jumper on each line to detach each pin of the module from the DTE application processor.
- Do not apply voltage to any UART interface pin before the switch-on of the UART supply source (**V_INT**), to avoid latch-up of circuits and allow a clean boot of the module.
- ESD sensitivity rating of the UART interface pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection levels could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible points.

2.6.1.2 Guidelines for UART layout design

The UART serial interface requires the same consideration regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.6.2 USB interface

- The USB interface is available for diagnostic purposes only.

2.6.2.1 Guidelines for USB circuit design

A suitable application circuit can be similar to the one illustrated in Figure 66, where direct external access is provided for diagnostic purposes by means of test points made available on the application board for **VUSB_DET**, **USB_D+** and **USB_D-** lines.

USB pull-up or pull-down resistors and external series resistors on **USB_D+** and **USB_D-** lines as required by the USB 2.0 specification [4] are part of the module USB pins driver and do not need to be externally provided.

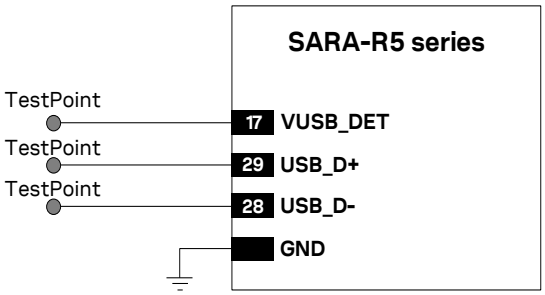

Figure 66: SARA-R5 series modules USB application circuit providing access for diagnostic purposes

- It is highly recommended to provide accessible test points directly connected to the USB interface pins (**VUSB_DET**, **USB_D+**, **USB_D-**) for diagnostic purposes.
- The USB interface pins ESD sensitivity rating is 1 kV (HBM according to JESD22-A114F). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting a very low capacitance (i.e. less or equal to 1 pF) ESD protection (e.g. the Littelfuse PESD0402-140 ESD protection) on the lines connected to these pins, close to accessible points.

2.6.2.2 Guidelines for USB layout design

USB_D+ / **USB_D-** lines should be designed with differential characteristic impedance (Z_0) as close as possible to 90 Ω and with common mode characteristic impedance (Z_{CM}) as close as possible to 30 Ω as defined by the USB 2.0 specification [4], routed as differential pair, with length as short as possible, avoiding any stubs, and avoiding abrupt change of layout.

However, the USB interface is available for diagnostic purposes only, and therefore the layout is not very critical: **USB_D+** / **USB_D-** lines have to be routed as differential pair, with short length, up to the related test points as illustrated in Figure 66.

2.6.3 SPI interfaces

- The SPI interfaces are not supported by the “00B” and “01B” product versions of SARA-R5 series modules, except for diagnostic purposes.
- Accessible test points directly connected to the **SDIO_D0**, **SDIO_D1**, **SDIO_D2** and **SDIO_D3** pins may be provided for diagnostic purposes, alternatively to the highly recommended test points on the USB interface pins.

2.6.4 SDIO interface

- The SDIO interface is not supported by the “00B” and “01B” product versions of SARA-R5 series modules.
- Accessible test points directly connected to the **SDIO_D0**, **SDIO_D1**, **SDIO_D2** and **SDIO_D3** pins may be provided for diagnostic purposes, alternatively to the highly recommended test points on the USB interface pins.

2.6.5 I2C interface

2.6.5.1 Guidelines for I2C circuit design

- Communication with an external GNSS receiver is not supported by SARA-R510M8S modules.

The I2C-bus host interface can be used to communicate with u-blox GNSS receivers and other external I2C-bus local devices as an audio codec.

The **SDA** and **SCL** pins of the module are open drain output as per I2C bus specifications [10], and they have internal pull-up resistors to the **V_INT** 1.8 V supply rail of the module, so there is no need of additional pull-up resistors on the external application board.

☞ Capacitance and series resistance must be limited on the bus to match the I2C specifications (1.0 µs is the max allowed rise time on **SCL** and **SDA** lines): route connections as short as possible.

☞ ESD sensitivity rating of the I2C pins is 1 kV (HBM according to JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible points.

Connection with u-blox 1.8 V GNSS receivers

☞ Communication with an external GNSS receiver is not supported by SARA-R510M8S modules.

Figure 67 shows a circuit example for connecting the cellular module to a u-blox 1.8 V GNSS receiver:

- The **SDA** and **SCL** pins of the cellular module are directly connected to the related pins of the u-blox 1.8 V GNSS receiver. External pull-up resistors are not needed, as they are already integrated in the cellular module.
- The **GPIO2** pin is connected to the active-high enable pin of the voltage regulator that supplies the u-blox 1.8 V GNSS receiver providing the "GNSS supply enable" function (see section 1.12). An additional pull-down resistor is provided to avoid a switch-on of the positioning receiver when the cellular module is switched off or in the reset state.
- The **GPIO3** pin is directly connected to the **TXD1** output pin of the u-blox 1.8 V GNSS receiver providing additional "GNSS data ready" function (see section 1.12), which is suitable for power consumption optimization.
- The **GPIO4** pin is directly connected to the **EXTINT** input pin of the u-blox 1.8 V GNSS receiver, implementing the additional optional "External GNSS time stamp of external interrupt" function (see section 1.12), which is suitable for timing features.
- The **SDIO_CMD** pin is directly connected to the **TIMEPULSE** output pin of the u-blox 1.8 V GNSS receiver, implementing the additional optional "External GNSS time pulse" function (see section 1.12), which is suitable for timing features.

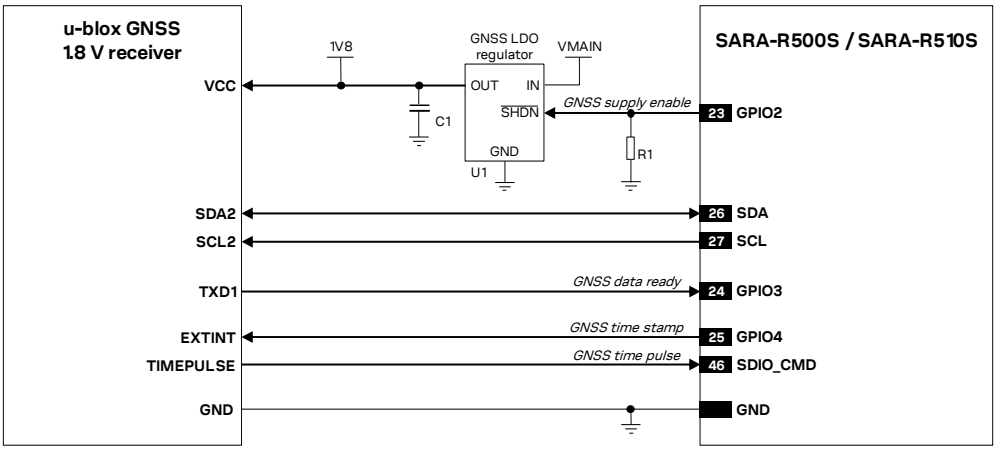

Figure 67: Application circuit for connecting SARA-R500S/SARA-R510S modules to a u-blox 1.8 V GNSS receiver

Reference	Description	Part number – Manufacturer
R1	47 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
U1, C1	Voltage regulator for GNSS receiver and related output bypass capacitor	See GNSS receiver hardware integration manual

Table 42: Components for connecting SARA-R500S/SARA-R510S modules to a u-blox 1.8 V GNSS receiver

☞ For additional guidelines regarding cellular and GNSS RF coexistence, see section 2.4.4.

☞ For additional guidelines regarding the design of applications with u-blox 1.8 V GNSS receivers, see the SARA-R5 / SARA-R4 positioning and timing implementation application note [18] and to the hardware integration manual of the u-blox GNSS receivers.

Connection with u-blox 3.0 V GNSS receivers

☞ Communication with an external GNSS receiver is not supported by SARA-R510M8S modules.

Figure 68 shows a circuit example for connecting the cellular module to a u-blox 3.0 V GNSS receiver:

- As the **SDA** and **SCL** pins of the cellular module are not tolerant up to 3.0 V, the connection to the related I2C pins of the u-blox 3.0 V GNSS receiver must be provided using a suitable I2C-bus bidirectional voltage translator (e.g. TI TCA9406, which additionally provides the partial power down feature so that the GNSS 3.0 V supply can be ramped up before the **V_INT** 1.8 V cellular supply). External pull-up resistors are not needed on the cellular module side, as they are already integrated in the cellular module.
- The **GPIO2** is connected to the active-high enable pin of the voltage regulator that supplies the u-blox 3.0 V GNSS receiver providing the "GNSS supply enable" function (see section 1.12). An additional pull-down resistor is provided to avoid a switch-on of the positioning receiver when the cellular module is switched off or in the reset state.
- The **GPIO3** pin is connected to the **TXD1** pin of the u-blox 3.0 V GNSS receiver providing additional "GNSS data ready" function profitable for power consumption optimization (see section 1.12), using a suitable unidirectional general purpose voltage translator.
- The **GPIO4** pin is connected to the **EXTINT** input pin of the u-blox 3.0 V GNSS receiver, implementing the additional optional "External GNSS time stamp of external interrupt" function for timing features (see section 1.12), using a suitable unidirectional general purpose voltage translator.
- The **SDIO_CMD** pin is connected to the **TIMEPULSE** output pin of the u-blox 3.0 V GNSS receiver, implementing the additional optional "External GNSS time pulse" function for timing features (see section 1.12), using a suitable unidirectional general purpose voltage translator.

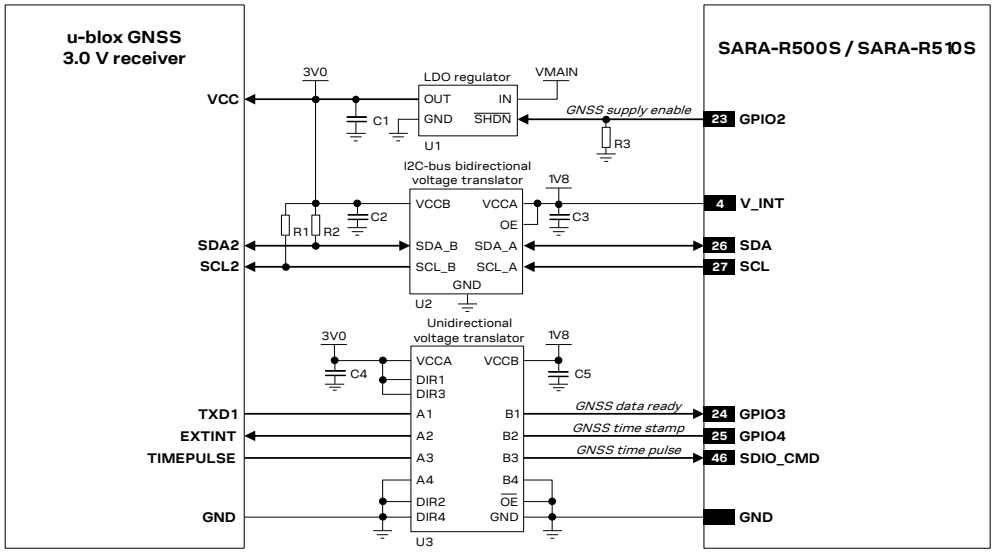

Figure 68: Application circuit for connecting SARA-R500S/SARA-R510S modules to a u-blox 3.0 V GNSS receiver

Reference	Description	Part number – Manufacturer
R1, R2	4.7 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R3	47 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
C2, C3, C4, C5	100 nF capacitor ceramic X5R 0402 10% 10V	GCM155R71C104KA55 – Murata
U1, C1	Voltage regulator for GNSS receiver and related output bypass capacitor	See GNSS receiver hardware integration manual
U2	I2C-bus bidirectional voltage translator	TCA9406DCUR – Texas Instruments
U3	Generic unidirectional voltage translator	SN74AVC4T774 [19] - Texas Instruments

Table 43: Components for connecting SARA-R500S/SARA-R510S modules to a u-blox 3.0 V GNSS receiver

☞ For additional guidelines regarding Cellular and GNSS RF coexistence, see section 2.4.4

☞ For additional guidelines regarding the design of applications with u-blox 3.0 V GNSS receivers, refer to the SARA-R5 / SARA-R4 positioning and timing implementation application note [18] and to the hardware integration manual of the u-blox GNSS receivers.

2.6.5.2 Guidelines for I2C layout design

The I2C serial interface requires the same consideration regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.7 Audio

☞ Audio is not supported by the “00B” and “01B” product versions of SARA-R5 series modules.

2.8 ADC

SARA-R5 series modules include an Analog-to-Digital Converter input pin, **ADC**, configurable via a dedicated AT command (for further details, see the SARA-R5 series AT commands manual [2]).

☞ ADC is not supported by the “00B” product versions of SARA-R5 series modules.

2.8.1 Guidelines for ADC circuit design

As a design example, the **ADC** input pin can be connected to an external voltage divider for voltage measurement purpose as illustrated in Figure 69.

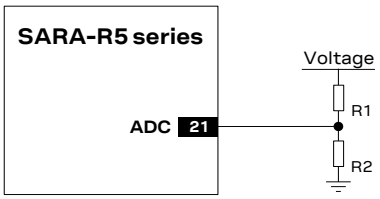

Figure 69: ADC application circuit example

☞ ESD sensitivity rating of the **ADC** pin is 1 kV (Human Body Model according to JESD22-A114). A higher protection level may be required if the lines are externally accessible. This can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible points.

[19] Voltage translator providing partial power down feature, so the 3 V supply can be also ramped up before **V_INT** 1.8 V supply

2.8.2 Guidelines for ADC layout design

The ADC circuit requires careful layout to perform proper measurements. Make sure that no transient noise is coupled on this line, otherwise the measurements might be affected. It is recommended to keep the connection line to **ADC** as short as possible.

2.9 General purpose input / output (GPIO)

2.9.1 Guidelines for GPIO circuit design

A typical usage of SARA-R5 series modules' GPIOs can be the following:

- Network indication provided over **GPIO1** pin (see Figure 70 / Table 44 below)
- Module status / operating mode indication provided by a GPIO pin (see section 1.6.1)
- "External GNSS supply enable" function provided by the **GPIO2** pin [20] (see section 2.6.5)
- "External GNSS data ready" function provided by the **GPIO3** pin [20] (see section 2.6.5)
- "External GNSS time stamp" function provided by the **GPIO4** pin [20] (see section 2.6.5)
- SIM card detection function provided over **GPIO5** pin (see Figure 53 / Table 35 in section 2.5)
- Time pulse function provided over **GPIO6** pin (see section Figure 70 / Table 44 below)
- Time stamp of external interrupt function provided over **EXT_INT** pin (see Figure 73)
- "External GNSS time pulse" function provided by the **SDIO_CMD** pin [20] (see section 2.6.5)
- Antenna dynamic tuning function provided over **I2S_TXD** and **I2S_WA** pins (see section 2.4.6)

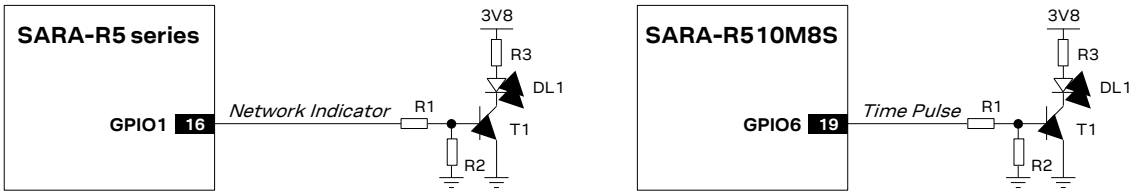

Figure 70: Application circuit for network indication provided over GPIO1

Reference	Description	Part number – Manufacturer
R1	10 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R2	47 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R3	820 Ω resistor 0402 5% 0.1 W	Generic manufacturer
DL1	LED red SMT 0603	LTST-C190KRKT – Lite-on Technology Corporation
T1	NPN BJT transistor	BC847 – Infineon

Table 44: Components for network indication application circuit

☞ Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO of SARA-R5 series modules.

☞ Do not apply voltage to any GPIO of the module before the switch-on of the GPIOs supply (**V_INT**), to avoid latch-up of circuits and allow a clean module boot.

☞ ESD sensitivity rating of the GPIO pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible points.

☞ If the GPIO pins are not used, they can be left unconnected on the application board.

2.9.2 Guidelines for general purpose input/output layout design

The general purpose input / output pins are generally not critical for layout.

[20] Not supported by SARA-R510M8S modules

2.10 GNSS peripheral output

☞ The GNSS peripheral output pins are not supported by the SARA-R500S, SARA-R510S and SARA-R510M8S-00B product versions.

☞ For additional information regarding the GNSS system, see the SARA-R5 / SARA-R4 positioning and timing implementation application note [18].

2.10.1 Guidelines for GNSS peripheral output circuit design

SARA-R510M8S modules provide the following 1.8 V peripheral output pins directly connected to the internal u-blox M8 GNSS chipset (as is illustrated in Figure 3):

- The ANT_ON output pin, over the **I2S_RXD** pin, can provide optional control for switching off power to an external active GNSS antenna or an external separate LNA (see Figure 44 and Figure 43).
- The GEOFENCE output pin, over the **I2S_CLK** pin, can provide optional indication of the geofencing status: the line can be connected to a digital input pin of the application processor (see Figure 71).

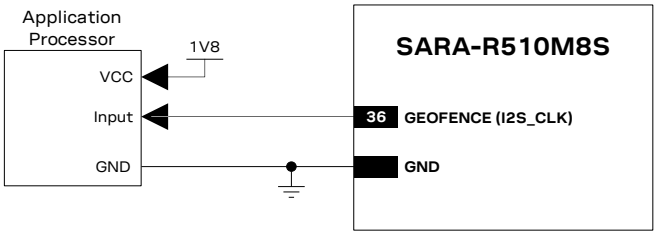

Figure 71: Application circuit for GNSS peripheral GEOFENCE output pin

2.10.2 Guidelines for GNSS peripheral output layout design

The GNSS peripheral output pins are generally not critical for layout.

2.11 Reserved pin (RSVD)

SARA-R5 series modules have a pin reserved for future use, marked as **RSVD**. This pin is to be left unconnected on the application board.

2.12 Module placement

An optimized placement allows minimum RF lines' length and closer path from DC source for **VCC**.

Make sure that the module, analog parts and RF circuits are clearly separated from any possible source of radiated energy. In particular, digital circuits can radiate digital frequency harmonics, which can produce electro-magnetic interference that affects the module, analog parts and RF circuits' performance. Implement suitable countermeasures to avoid any possible electro-magnetic compatibility issue.

Make sure that the module is placed in order to keep the antenna (or antennas, for SARA-R510M8S) as far as possible from VCC supply line and related parts (refer to Figure 29), from high-speed digital lines (as USB) and from any possible noise source.

Provide enough clearance between the module and any external part: clearance of at least 0.4 mm per side is recommended to let suitable mounting of the parts.

☞ The heat dissipation during continuous transmission at maximum power can raise the temperature of the application baseboard below the SARA-R5 series modules: avoid placing temperature sensitive devices close to the module.

2.13 Module footprint and paste mask

Figure 72 and Table 45 describe the suggested footprint (i.e. copper mask) and paste mask layout for SARA modules: the proposed land pattern layout reflects the modules' pins layout, while the proposed stencil apertures layout is slightly different (see the F'', H'', I'', J'', O'' parameters compared to the F', H', I', J', O' ones).

The Non Solder-resist Mask Defined (NSMD) pad type is recommended over the Solder-resist Mask Defined (SMD) pad type, as it implements the solder resist mask opening 50 µm larger per side than the corresponding copper pad.

The recommended thickness of the stencil for the soldering paste is 150 µm, according to application production process requirements.

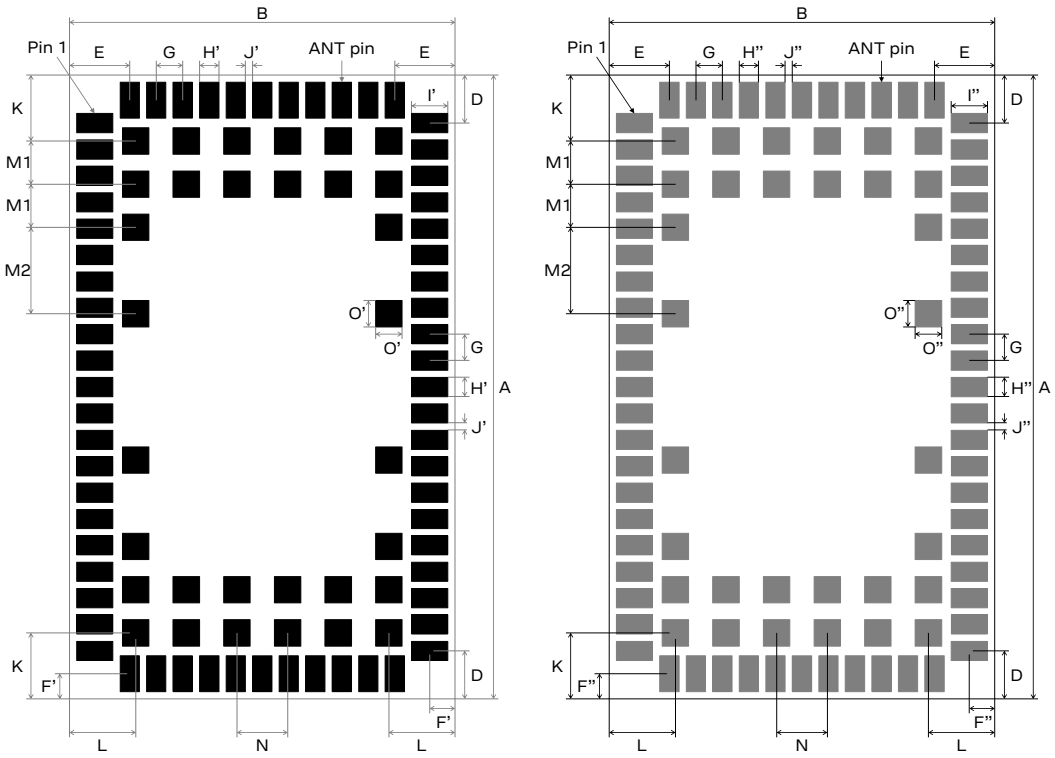

Figure 72: SARA-R5 series modules suggested footprint and paste mask (application board top view)

Parameter	Value	Parameter	Value	Parameter	Value
A	26.0 mm	G	1.10 mm	K	2.75 mm
B	16.0 mm	H'	0.80 mm	L	2.75 mm
C	3.00 mm	H''	0.75 mm	M1	1.80 mm
D	2.00 mm	I'	1.50 mm	M2	3.60 mm
E	2.50 mm	I''	1.55 mm	N	2.10 mm
F'	1.05 mm	J'	0.30 mm	O'	1.10 mm
F''	1.00 mm	J''	0.35 mm	O''	1.05 mm

Table 45: SARA-R5 series modules suggested footprint and paste mask dimensions

☞ These are recommendations only and not specifications. The exact copper, solder and paste mask geometries, distances, stencil thicknesses and solder paste volumes must be adapted to the specific production processes (e.g. soldering etc.) implemented.

2.14 Schematic for SARA-R5 series module integration

Figure 73 is an example of a schematic diagram where a SARA-R5 series module “00B” product version is integrated into an application board using most of the available interfaces and functions of the module.

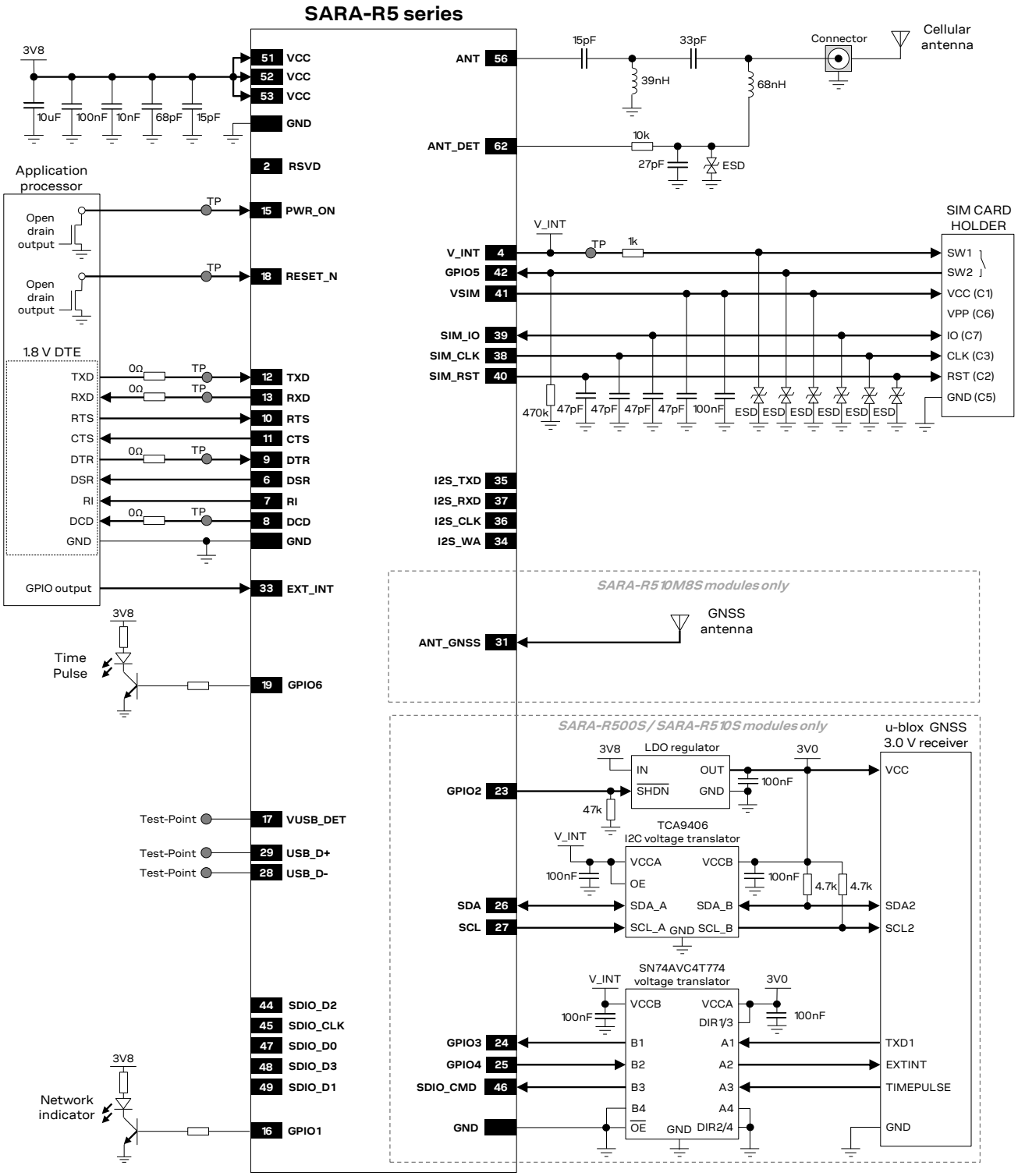

Figure 73: Example of schematic diagram to integrate a SARA-R5 series module “00B” product version using most of the available interfaces

Figure 74 is an example of a schematic diagram where a SARA-R5 series module "01B" product version is integrated into an application board using most of the available interfaces and functions of the module.

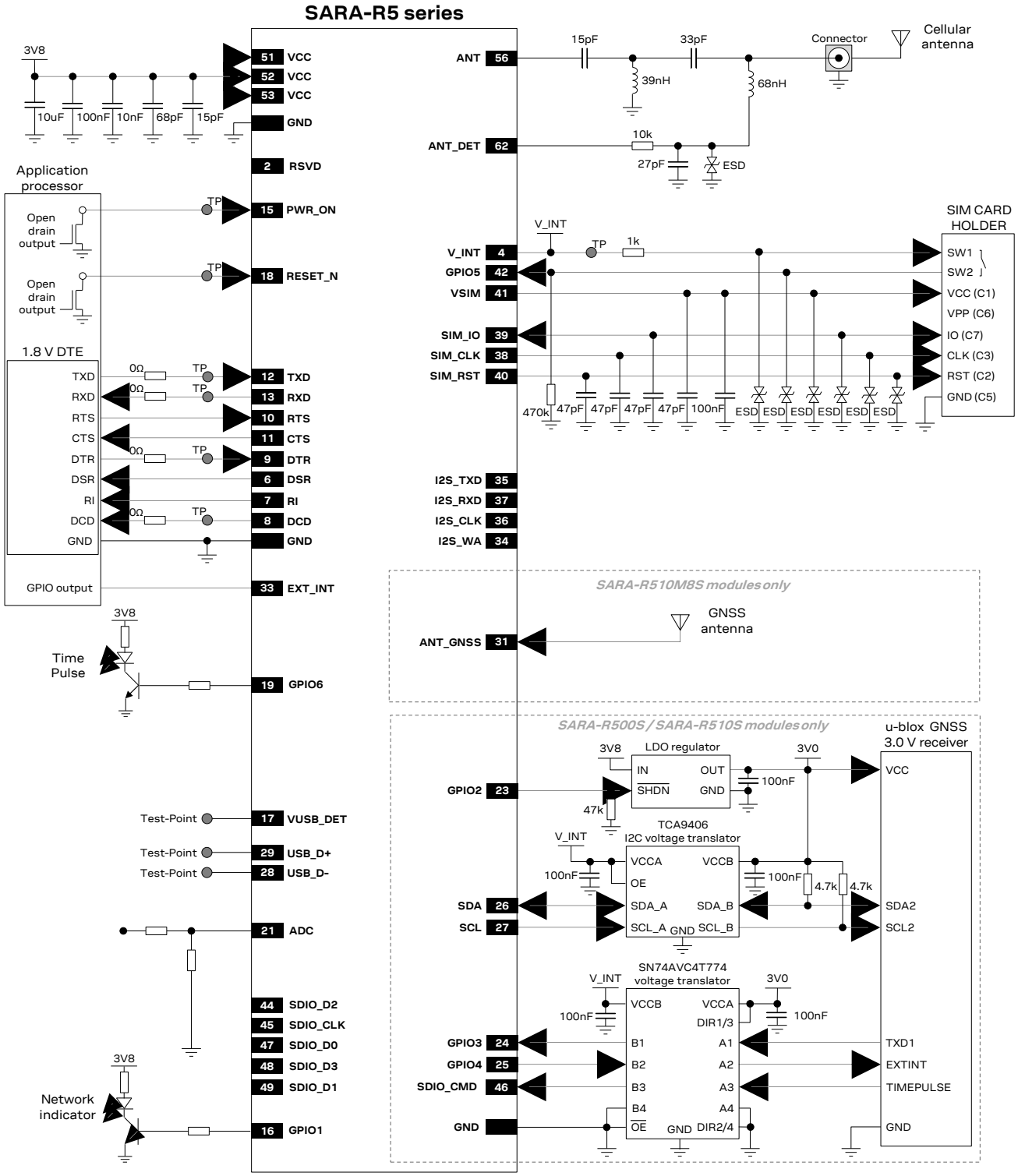

Figure 74: Example of schematic diagram to integrate a SARA-R5 series module "01B" product version using most of the available interfaces

2.15 Design-in checklist

This section provides a design-in checklist.

2.15.1 Schematic checklist

The following are the most important points for a simple schematic check:

- ☑ DC supply must provide a nominal voltage at **VCC** pin within the operating range limits.
- ☑ DC supply must be capable of supporting the highest peak / pulse current consumption values and the maximum averaged current consumption values in connected mode, as specified in the SARA-R5 series data sheet [1].
- ☑ **VCC** voltage supply should be clean, with very low ripple/noise: provide the suggested bypass capacitors, in particular if the application device integrates an internal antenna.
- ☑ Do not apply loads which might exceed the limit for maximum available current from **V_INT** supply.
- ☑ Check that voltage level of any connected pin does not exceed the relative operating range.
- ☑ Provide accessible test points directly connected to the **V_INT**, **PWR_ON** and **RESET_N** pins of the SARA-R5 series modules for diagnostic purposes.
- ☑ Capacitance and series resistance must be limited on each SIM signal to match the SIM specifications.
- ☑ Insert the suggested pF capacitors on each SIM signal and low capacitance ESD protections if accessible.
- ☑ Check UART signals direction, considering the modules' signal names follow the ITU-T V.24 recommendation [5].
- ☑ Provide accessible test points directly connected to the **TXD** and **RXD** pins of the SARA-R5 series modules for FW update purpose and to the **DCD** and **DTR** pins for diagnostic purposes, in particular providing a 0 Ω series jumper on each line to detach each pin of the module from the DTE application processor.
- ☑ Provide accessible test points directly connected to the **VUSB_DET**, **USB_D+** and **USB_D-** pins of the SARA-R5 series modules for diagnostic purposes.
- ☑ Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO when those are used to drive LEDs.
- ☑ Provide adequate precautions for EMC / ESD immunity as required on the application board.
- ☑ Do not apply voltage to any generic digital interface pin of SARA-R5 series modules before the switch-on of the generic digital interface supply source (**V_INT**).
- ☑ All unused pins can be left unconnected.

2.15.2 Layout checklist

The following are the most important points for a simple layout check:

- ☑ Check 50 Ω nominal characteristic impedance of the RF transmission line connected to the **ANT** port (cellular antenna RF interface).
- ☑ Check cellular antenna trace design for regulatory compliance perspective (see section 4.2.3 for FCC United States, section 4.3.2 for ISED Canada, and related section 2.4.2.3).
- ☑ For SARA-R510M8S, check 50 Ω nominal characteristic impedance of the RF transmission line connected to the **ANT_GNSS** port (GNSS antenna RF interface).
- ☑ Ensure no coupling occurs between the RF interfaces and noisy or sensitive signals (like SIM signals and high-speed digital lines).
- ☑ Optimize placement for minimum length of RF lines.
- ☑ Check the footprint and paste mask designed for SARA-R5 series module as illustrated in section 2.13.
- ☑ **VCC** line should be enough wide and as short as possible.
- ☑ Route **VCC** supply line away from RF lines / parts (refer to Figure 29) and other sensitive analog lines / parts.
- ☑ The **VCC** bypass capacitors in the picofarad range should be placed as close as possible to the **VCC** pins, in particular if the application device integrates an internal antenna.
- ☑ Ensure an optimal grounding connecting each **GND** pin with application board solid ground layer.
- ☑ Use as many vias as possible to connect the ground planes on multilayer application board, providing a dense line of vias at the edges of each ground area, in particular along RF and high-speed lines.
- ☑ Keep routing short and minimize parasitic capacitance on the SIM lines to preserve signal integrity.
- ☑ **USB_D+** / **USB_D-** traces should meet the characteristic impedance requirement (90 Ω differential and 30 Ω common mode) and should not be routed close to any RF line / part.

2.15.3 Antennas checklist

- ☑ Antenna termination should provide 50 Ω characteristic impedance with V.S.W.R at least less than 3:1 (recommended 2:1) on operating bands in deployment geographical area.
- ☑ Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).
- ☑ Ensure compliance with any regulatory agency RF radiation requirement, as reported in section 4.2.2 for FCC United States, in section 4.3.1 for ISED Canada, and in section 4.4 for RED Europe.
- ☑ Ensure high isolation between the cellular antenna and any other antennas or transmitters present on the end device.
- ☑ For SARA-R510M8S, ensure high isolation between the cellular antenna and the GNSS antenna (see also section 2.4.4)

3 Handling and soldering

☞ No natural rubbers, no hygroscopic materials or materials containing asbestos are employed.

3.1 Packaging, shipping, storage and moisture preconditioning

For information pertaining to SARA-R5 series reels / tapes, Moisture Sensitivity levels (MSD), shipment and storage information, as well as drying for preconditioning, see the SARA-R5 series data sheet [1] and the u-blox package information user guide [16].

3.2 Handling

The SARA-R5 series modules are Electro-Static Discharge (ESD) sensitive devices.

⚠ Ensure ESD precautions are implemented during handling of the module.

Electro-Static Discharge (ESD) is the sudden and momentary electric current that flows between two objects at different electrical potentials caused by direct contact or induced by an electrostatic field. The term is usually used in the electronics and other industries to describe momentary unwanted currents that may cause damage to electronic equipment.

The ESD sensitivity for each pin of SARA-R5 series modules (as Human Body Model according to JESD22-A114F) is specified in the SARA-R5 series data sheet [1].

ESD prevention is based on establishing an Electrostatic Protective Area (EPA). The EPA can be a small working station or a large manufacturing area. The main principle of an EPA is that there are no highly charging materials near ESD sensitive electronics, all conductive materials are grounded, workers are grounded, and charge build-up on ESD sensitive electronics is prevented. International standards are used to define typical EPA and can be obtained for example from the International Electrotechnical Commission (IEC) or the American National Standards Institute (ANSI).

In addition to standard ESD safety practices, the following measures should be taken into account whenever handling the SARA-R5 series modules:

- Unless there is a galvanic coupling between the local GND (i.e. the work table) and the PCB GND, then the first point of contact when handling the PCB must always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect the ground of the device.
- When handling the module, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna, coax cable, soldering iron).
- To prevent electrostatic discharge through the RF pin, do not touch any exposed antenna area. If there is any risk that such exposed antenna area is touched in a non-ESD protected work area, implement adequate ESD protection measures in the design.
- When soldering the module and patch antennas to the RF pin, make sure to use an ESD-safe soldering iron.

3.3 Soldering

3.3.1 Soldering paste

"No Clean" soldering paste is strongly recommended for SARA-R5 series modules, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.

Soldering paste:	OM338 SAC405 / Nr.143714 (Cookson Electronics)
Alloy specification:	95.5% Sn / 3.9% Ag / 0.6% Cu (95.5% tin / 3.9% silver / 0.6% copper) 95.5% Sn / 4.0% Ag / 0.5% Cu (95.5% tin / 4.0% silver / 0.5% copper)
Melting temperature:	217 °C
Stencil thickness:	150 µm for base boards

The final choice of the soldering paste depends on the approved manufacturing procedures.

The paste-mask geometry for applying soldering paste should meet the recommendations in section 2.13.

☞ The quality of the solder joints should meet the appropriate IPC specification.

3.3.2 Reflow soldering

A convection type-soldering oven is strongly recommended for SARA-R5 series modules over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature and all parts will be heated up evenly, regardless of material properties, thickness of components and surface color.

Consider the "IPC-7530A Guidelines for temperature profiling for mass soldering (reflow and wave) processes". Reflow profiles are to be selected according to the following recommendations.

⚠ Failure to observe these recommendations can result in severe damage to the device!

Preheat phase

Initial heating of component leads and balls. Residual humidity will be dried out. Note that this preheat phase will not replace prior baking procedures.

- Temperature rise rate: max 3 °C/s
  If the temperature rise is too rapid in the preheat phase it may cause excessive slumping.
- Time: 60 ÷ 120 s
  If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.
- End temperature: +150 ÷ +200 °C
  If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

Heating/ reflow phase

The temperature rises above the liquidus temperature of +217 °C. Avoid a sudden rise in temperature as the slump of the paste could become worse.

- Limit time above +217 °C liquidus temperature: 40 ÷ 60 s
- Peak reflow temperature: +245 °C

Cooling phase

A controlled cooling avoids negative metallurgical effects of the solder (solder becomes more brittle) and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.

- Temperature fall rate: max 4 °C/s

To avoid falling off, modules should be placed on the topside of the motherboard during soldering.

The soldering temperature profile chosen at the factory depends on additional external factors like choice of soldering paste, size, thickness and properties of the base board, etc.

Exceeding the maximum soldering temperature and the maximum liquidus time limit in the recommended soldering profile may permanently damage the module.

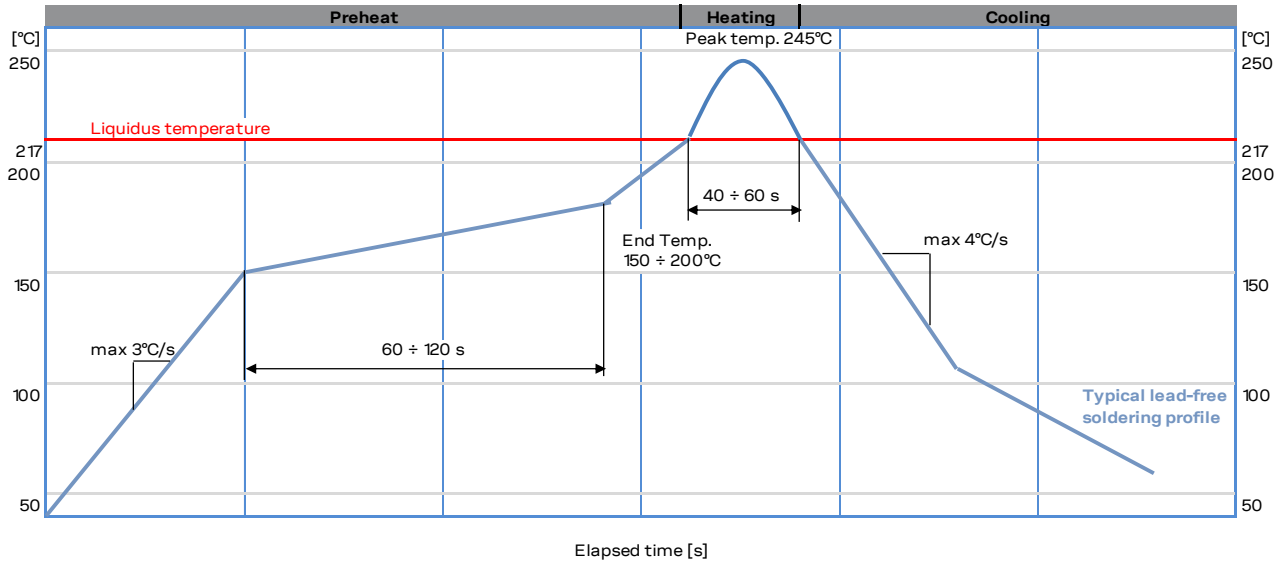

Figure 75: Recommended soldering profile

The modules must not be soldered with a damp heat process.

3.3.3 Optical inspection

After soldering the module, inspect it optically to verify that it is correctly aligned and centered.

3.3.4 Cleaning

Cleaning the modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the housing, area that is not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the quartz oscillators.

For best results, use a “no clean” soldering paste and eliminate the cleaning step after the soldering.

3.3.5 Repeated reflow soldering

Repeated reflow soldering processes and soldering the module upside-down are not recommended.

Boards with components on both sides may require two reflow cycles. In this case, the module should always be placed on the side of the board that is submitted into the last reflow cycle. The reason for this (besides others) is the risk of the module falling off due to the significantly higher weight in relation to other components.

☞ u-blox gives no warranty against damages to the SARA-R5 series modules caused by performing more than a total of two reflow soldering processes (one reflow soldering process to mount the SARA-R5 series module, plus one reflow soldering process to mount other parts).

3.3.6 Wave soldering

SARA-R5 series LGA modules must not be soldered with a wave soldering process.

Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require wave soldering to solder the THT components. No more than one wave soldering process is allowed for a board with a SARA-R5 series module already populated on it.

⚠ Performing a wave soldering process on the module can result in severe damage to the device!

☞ u-blox gives no warranty for damages to the SARA-R5 series modules caused by performing more than a total of two soldering processes (one reflow soldering process to mount the SARA-R5 series module, plus one wave soldering process to mount other THT parts on the application board).

3.3.7 Hand soldering

Hand soldering is not recommended.

3.3.8 Rework

Rework is not recommended.

☞ Never attempt a rework on the module itself, e.g. replacing individual components. Such actions immediately terminate the warranty.

3.3.9 Conformal coating

Certain applications employ a conformal coating of the PCB using HumiSeal® or other related coating products.

These materials affect the RF properties of the cellular modules and it is important to prevent them from flowing into the module.

The RF shields do not provide 100% protection for the module from coating liquids with low viscosity, therefore care is required in applying the coating.

☞ Conformal Coating of the module will void the warranty.

3.3.10 Casting

If casting is required, use viscose or another type of silicon pottant. The OEM is strongly advised to qualify such processes in combination with the cellular modules before implementing this in production.

☞ Casting will void the warranty.

3.3.11 Grounding metal covers

Attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's own risk. The numerous ground pins should be sufficient to provide optimum immunity to interference and noise.

☞ u-blox gives no warranty for damages to the cellular modules caused by soldering metal cables or any other forms of metal strips directly onto the EMI covers.

3.3.12 Use of ultrasonic processes

The cellular modules contain components which are sensitive to ultrasonic waves. Use of any ultrasonic processes (cleaning, welding etc.) may cause damage to the module.

☞ u-blox gives no warranty for damages to the cellular modules caused by any ultrasonic processes.

4 Approvals

4.1 Product certification approval overview

Product certification approval is the process of certifying that a product has passed all tests and criteria required by specifications, typically called “certification schemes”, which can be divided into:

- Regulatory certifications
  - Country-specific approval required by local government in most regions and countries, as:
    - CE (European Conformity) marking for European Union
    - FCC (Federal Communications Commission) approval for the United States
- Industry certifications
  - Telecom industry-specific approval verifying interoperability between devices and networks:
    - GCF (Global Certification Forum)
    - PTCRB (PCS Type Certification Review Board)
- Operator certifications
  - Operator-specific approvals required by some mobile network operator, such as:
    - AT&T network operator in United States
    - Verizon Wireless network operator in United States

The manufacturer of the end-device that integrates a SARA-R5 series module must take care of all certification approvals required by the specific integrating device to be deployed in the market.

The required certification scheme approvals and relative testing specifications applicable to the end-device that integrates a SARA-R5 series module differ depending on the country or the region where the integrating device is intended to be deployed, on the relative vertical market of the device, on type, features and functionalities of the whole application device, and on the network operators where the device is intended to operate.

The main approvals of the modules are indicated in the SARA-R5 series data sheet [1].

☞ Check the appropriate applicability of the SARA-R5 series module’s approvals while starting the certification process of the device integrating the module: the re-use of the u-blox cellular module’s approval can significantly reduce the cost and time to market of the application device certification.

The SARA-R5 series modules include the capability to configure the device by selecting the operating Mobile Network Operator Profile, Radio Access Technology, and bands. In the SARA-R5 series AT commands manual [2], see the +UMNOPROF, +URAT, and +UBANDMASK AT commands.

As these configuration decisions are made, u-blox reminds manufacturers of the host application device integrating the SARA-R5 series modules to take care of compliance with all the certification approvals requirements applicable to the specific integrating device to be deployed in the market.

☞ It is strongly recommended to configure the module to the applicable MNO profile, RAT, and LTE bands intended for the host end-device and within regulatory compliance.

☞ The certification of the host application device that integrates a SARA-R5 series module and the compliance of the host application device with all the applicable certification schemes, directives and standards are the sole responsibility of the host application device manufacturer.

SARA-R5 series modules are certified according to all capabilities and options stated in the Protocol Implementation Conformance Statement document (PICS) of the module. The PICS, according to the 3GPP TS 36.521-2 [13] and 3GPP TS 36.523-2 [14], is a statement of the implemented and supported capabilities and options of a device.

☞ The PICS document of the host device integrating SARA-R5 series modules must be updated from the module PICS statement if any feature stated as supported by the module in its PICS document is not implemented or disabled in the host application device. For more details regarding the AT commands settings that affect the PICS, see the SARA-R5 series AT commands manual [2].

☞ Check the specific settings required by the mobile network operators in use by the host application device, as they may differ from the AT commands factory-programmed settings of the module.

4.2 US Federal Communications Commission notice

United States Federal Communications Commission (FCC) ID: XPYUBX19KM01

4.2.1 Safety warnings review the structure

- Equipment for building-in. Requirements for fire enclosure must be evaluated in the end product
- The clearance and creepage current distances required by the end product must be withheld when the module is installed
- The cooling of the end product shall not negatively be influenced by the installation of the module
- Excessive sound pressure from earphones and headphones can cause hearing loss
- No natural rubbers, hygroscopic materials, or materials containing asbestos are employed

4.2.2 Declaration of Conformity

This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions:

- this device may not cause harmful interference
- this device must accept any interference received, including interference that may cause undesired operation

⚠ Radiofrequency radiation exposure information: this equipment complies with the radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

⚠ The gain of the system antenna(s) used for the SARA-R5 series modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed the value specified in the FCC Grant for mobile and fixed or mobile operating configurations:

- 7.8 dBi in 700 MHz, i.e. LTE FDD-12 band
- 9.2 dBi in 750 MHz, i.e. LTE FDD-13 band
- 9.4 dBi in 850 MHz, i.e. LTE FDD-5 band
- 7.4 dBi in 850 MHz, i.e. LTE FDD-26 band
- 6.8 dBi in 1700 MHz, i.e. LTE FDD-4 band
- 10.3 dBi in 1900 MHz, i.e. LTE FDD-2 band
- 10.4 dBi in 1900 MHz, i.e. LTE FDD-25 band

4.2.3 Modifications

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by u-blox could void the user's authority to operate the equipment.

⚠ Manufacturers of mobile or fixed devices incorporating SARA-R5 series modules are authorized to use the FCC Grants of the SARA-R5 series modules for their own final host products according to the conditions referenced in the certificates.

⚠ Manufacturers of mobile or fixed devices incorporating SARA-R5 series modules are authorized to use the FCC Grants of the SARA-R5 series modules for their own final host products if, as per FCC KDB 996369, the antenna trace design implemented on the host PCB is electrically equivalent to the antenna trace design implemented on the u-blox host PCB used for regulatory type approvals of the SARA-R5 series modules, described in details in section 2.4.2.3.

⚠ In case of antenna trace design change, an FCC Class II Permissive Change application is required to be filed by the grantee, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by an FCC Class II Permissive Change application.

⚠ If the FCC Grants of the SARA-R5 series modules can be used for the final host product, as the conditions above are met, the FCC Label of the module shall be visible from the outside, or the host device shall bear a second label stating:

"Contains FCC ID: XPYUBX19KM01"

⚠ IMPORTANT: Manufacturers of portable applications incorporating the SARA-R5 series modules are required to have their final product certified and apply for their own FCC Grant related to the specific portable device. This is mandatory to meet the SAR requirements for portable devices.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

⚠ Additional Note: as per 47 CFR 15.105 this equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consultant the dealer or an experienced radio/TV technician for help

4.3 Innovation, Science, Economic Development Canada notice

ISED Canada (formerly known as IC – Industry Canada) Certification Number: 8595A-UBX19KM01

4.3.1 Declaration of Conformity

This device complies with the ISED Canada license-exempt RSS standard(s). Operation is subject to the following two conditions:

- this device may not cause harmful interference
- this device must accept any interference received, including interference that may cause undesired operation

⚠ Radiofrequency radiation exposure information: this equipment complies with the radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

⚠ The gain of the system antenna(s) used for the SARA-R5 series modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed the value stated in the ISED Canada Grant for mobile and fixed or mobile operating configurations:

- 5.6 dBi in 700 MHz, i.e. LTE FDD-12 band
- 5.9 dBi in 750 MHz, i.e. LTE FDD-13 band
- 6.1 dBi in 850 MHz, i.e. LTE FDD-5 band
- 6.1 dBi in 850 MHz, i.e. LTE FDD-26 band
- 6.8 dBi in 1700 MHz, i.e. LTE FDD-4 band
- 8.5 dBi in 1900 MHz, i.e. LTE FDD-2 band
- 8.5 dBi in 1900 MHz, i.e. LTE FDD-25 band

4.3.2 Modifications

ISED Canada requires the user to be notified that any changes or modifications made to this device that are not expressly approved by u-blox could void the user's authority to operate the equipment.

⚠ Manufacturers of mobile or fixed devices incorporating SARA-R5 series modules are authorized to use the ISED Canada Certificates of the SARA-R5 series modules for their own final host products according to the conditions referenced in the certificates.

⚠ Manufacturers of mobile or fixed devices incorporating SARA-R5 series modules are authorized to use the ISED Certificates of SARA-R5 series modules for their own final host products if, as per FCC KDB 996369, the antenna trace design implemented on the host PCB is electrically equivalent to the antenna trace design implemented on the u-blox host PCB used for the regulatory type approvals of the SARA-R5 series modules, described in details in section 2.4.2.3.

⚠ In case of antenna trace design change, a Class IV Permissive Change application is required to be filed by the grantee, or the host manufacturer can take responsibility through the ISED Multiple Listing (new application) procedure followed by an ISED Class IV Permissive Change application.

⚠ If the ISED Certificates of the SARA-R5 series modules can be used for the final host product, as the conditions above are met, the ISED Label of the module shall be visible from the outside, or the host device shall bear a second label stating:

"Contains IC: 8595A-UBX19KM01"

⚠ **Innovation, Science and Economic Development Canada (ISED) Notices**

This Class B digital apparatus complies with Canadian CAN ICES-3(B) / NMB-3(B).
Operation is subject to the following two conditions:

- this device may not cause interference
- this device must accept any interference, including interference that may cause undesired operation of the device

Radio Frequency (RF) Exposure Information

The radiated output power of the u-blox Cellular Module is below the Innovation, Science and Economic Development Canada (ISED) radio frequency exposure limits. The u-blox Cellular Module should be used in a manner such that the potential for human contact during normal operation is minimized.

This device has been evaluated and shown compliant with the IC RF Exposure limits under mobile exposure conditions (antennas are greater than 20 cm from a person's body).

This device has been certified for use in Canada. Status of the listing in the Industry Canada's REL (Radio Equipment List) can be found at the following web address:
http://www.ic.gc.ca/app/sitt/reltel/srch/nwRdSrch.do?lang=eng

Additional Canadian information on RF exposure also can be found at the following web address:
http://www.ic.gc.ca/eic/site/smt-gst.nsf/eng/sf08792.html

⚠ IMPORTANT: Manufacturers of portable applications incorporating the SARA-R5 series modules are required to have their final product certified and apply for their own Industry Canada Certificate related to the specific portable device. This is mandatory to meet the SAR requirements for portable devices.
Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

⚠ **Avis d'Innovation, Sciences et Développement économique Canada (ISDE)**

Cet appareil numérique de classe B est conforme aux normes canadiennes CAN ICES-3(B) / NMB-3(B). Son fonctionnement est soumis aux deux conditions suivantes :

- cet appareil ne doit pas causer d'interférence
- cet appareil doit accepter toute interférence, notamment les interférences qui peuvent affecter son fonctionnement

Informations concernant l'exposition aux fréquences radio (RF)

La puissance de sortie émise par l'appareil de sans-fil u-blox Cellular Module est inférieure à la limite d'exposition aux fréquences radio d'Innovation, Sciences et Développement économique Canada (ISDE). Utilisez l'appareil de sans-fil u-blox Cellular Module de façon à minimiser les contacts humains lors du fonctionnement normal.

Ce périphérique a été évalué et démontré conforme aux limites d'exposition aux fréquences radio (RF) d'IC lorsqu'il est installé dans des produits hôtes particuliers qui fonctionnent dans des conditions d'exposition à des appareils mobiles (les antennes se situent à plus de 20 centimètres du corps d'une personne).

Ce périphérique est homologué pour l'utilisation au Canada. Pour consulter l'entrée correspondant à l'appareil dans la liste d'équipement radio (REL – Radio Equipment List) d'Industrie Canada rendez-vous sur : http ://www.ic.gc.ca/app/sitt/reltel/srch/nwRdSrch.do?lang=fra

Pour des informations supplémentaires concernant l'exposition aux RF au Canada rendez-vous sur : http ://www.ic.gc.ca/eic/site/smt-gst.nsf/fra/sf08792.html

⚠ IMPORTANT: les fabricants d'applications portables contenant les modules de la SARA-R5 series doivent faire certifier leur produit final et déposer directement leur candidature pour une certification FCC ainsi que pour un certificat ISDE Canada délivré par l'organisme chargé de ce type d'appareil portable. Ceci est obligatoire afin d'être en accord avec les exigences SAR pour les appareils portables.
Tout changement ou modification non expressément approuvé par la partie responsable de la certification peut annuler le droit d'utiliser l'équipement.

4.4 European Conformance

The SARA-R5 series modules have been evaluated against the essential requirements of the Radio Equipment Directive 2014/53/EU (RED). In order to satisfy the essential requirements of the RED, the modules are compliant with the following standards:

- Radio Spectrum Efficiency (Article 3.2):
  - EN 301 908-1
  - EN 301 908-13
  - EN 303 413
- Electromagnetic Compatibility (Article 3.1b):
  - EN 301 489-1
  - EN 301 489-19
  - EN 301 489-52
- Health and Safety (Article 3.1a)
  - EN 62368-1
  - EN 62311

⚠ Radiofrequency radiation exposure Information: this equipment complies with radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

⚠ The gain of the system antenna(s) used for SARA-R5 series modules (i.e. combined transmission line, connector, cable losses and radiating element gain) must not exceed the values stated in the Declaration of Conformity of the modules, for mobile and fixed or mobile operating configurations:

- 7.4 dBi in 700 MHz, i.e. LTE FDD-28 band
- 8.2 dBi in 800 MHz, i.e. LTE FDD-20 band
- 8.4 dBi in 900 MHz, i.e. LTE FDD-8 band
- 11.3 dBi in 1800 MHz, i.e. LTE FDD-3 band
- 11.8 dBi in 2100 MHz, i.e. LTE FDD-1 band

The conformity assessment procedure for the SARA-R5 series modules, referred to in Article 17 and detailed in Annex II of Directive 2014/53/EU, has been followed.

Thus, the following marking is included in the product:

CE

4.5 GITEKI Japan

- SARA-R500S-00B, SARA-R510S-00B, SARA-R510M8S-00B

T D200145003
R 003-200173

The gain of the system antenna used for SARA-R5 series modules must not exceed 3 dBi to comply with Japan Technical Standard Conformity Certification (GITEKI Certification) requirements.

Additionally, the antenna used in the end-device system for SARA-R5 series modules has to be listed on the technology conformity certified Antenna list of the related module. Please contact u-blox for more information about how to add the antenna used in the end-device system into the Antenna list of the related module.

5 Product testing

5.1 u-blox in-series production test

u-blox focuses on high quality for its products. All units produced are fully tested automatically on the production line. Stringent quality control processes have been implemented in the production line. Defective units are analyzed in detail to improve production quality.

This is achieved with automatic test equipment (ATE) in the production line, which logs all production and measurement data. A detailed test report for each unit can be generated from the system. The following Figure 76 illustrates the typical automatic test equipment (ATE) in a production line.

The following typical tests are among the production tests.

- Digital self-test (firmware download, flash firmware verification, IMEI programming)
- Measurement of voltages and currents
- Adjustment of ADC measurement interfaces
- Functional tests (serial interface communication, SIM card communication)
- Digital tests (GPIOs and other interfaces)
- Measurement and calibration of RF characteristics in all supported bands (such as receiver S/N verification, frequency tuning of the reference clock, calibration of transmitter and receiver power levels, etc.)
- Verification of the RF characteristics after calibration (i.e. modulation accuracy, power levels, spectrum, etc. are checked to ensure they are all within tolerances when calibration parameters are applied)

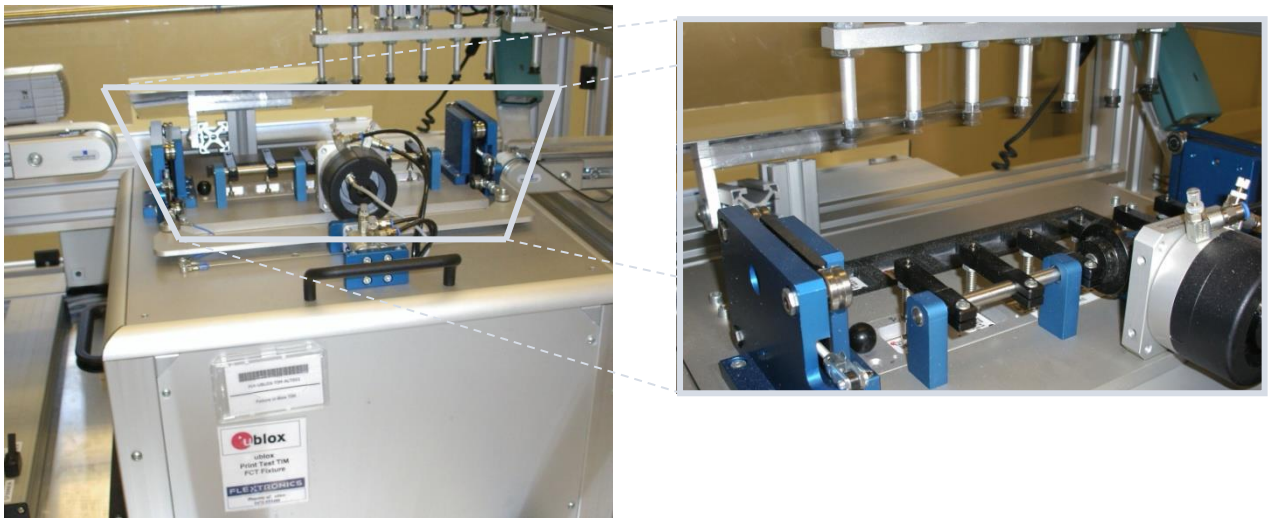

Figure 76: Automatic test equipment for module tests

5.2 Test parameters for OEM manufacturers

Because of the testing done by u-blox (with 100% coverage), an OEM manufacturer does not need to repeat the firmware tests or measurements of the module RF performance or tests over analog and digital interfaces in their production test.

However, an OEM manufacturer should focus on:

- Module assembly on the application device; it should be verified that:
  - The soldering and handling process did not damage the module components
  - All module pins are well soldered on the device board
  - There are no short circuits between pins

- Component assembly on the application device; it should be verified that:
  - Communication with the host controller can be established
  - The interfaces between the module and device are working
  - Overall RF functional test of the device including the antenna/s

Dedicated tests can be implemented to check the device. For example, the measurement of the module current consumption when set in a specified status can detect a short circuit if compared with a "Golden Device" result.

In addition, module AT commands can be used to perform functional tests on the digital interfaces (communication with the host controller, check the SIM interface, GPIOs, etc.) or to perform RF functional tests (see the following section 5.2.2 for details).

5.2.1 "Go / No go" tests for integrated devices

A "Go / No go" test is typically used to compare the signal quality with a "Golden Device".

The cellular RF functionality should be checked with the DUT (Device Under Test) placed in a location with excellent cellular network coverage and known cellular signal quality. This test should be performed after the data connection has been established. +CSQ is the typical AT command used to check signal quality in term of RSSI, comparing the DUT with a "Golden Device". See the SARA-R5 series AT commands manual [2] for detail usage of the AT command.

☞ These kinds of test may be useful as a "go / no go" test but not for cellular RF performance measurements neither for certifications purpose.

This test is suitable also to check the communications with the host controller, the SIM card and the power supply. It is also a mean to verify if components at the cellular RF interface are well soldered.

The GNSS RF functionality should be checked with the device under test (DUT) placed in an outdoor position, with excellent sky view (HDOP < 3.0). Let the receiver acquire satellites and compare the signal strength with a "Golden Device".

☞ As the electro-magnetic field of a redistribution antenna is not homogenous, indoor tests are in most cases not reliable to check the GNSS RF functionality. This kind of tests may be useful as a 'go/no go' test but not for GNSS sensitivity measurements.

5.2.2 Cellular RF functional tests

As mentioned before, OEM manufacturers need only to verify proper assembly of the module in the OEM production line, i.e. proper soldering joint of the **ANT** pad and related parts along the RF path, and this can be done by performing a simple RF functional test with basic instruments such as a spectrum analyzer (or an RF power meter), and optionally a signal generator, with the assistance of the +UTEST AT command over the AT command user interface.

The +UTEST AT command provides a simple interface to set the module to Rx or Tx test modes ignoring the LTE signaling protocol. The command can set the module into:

- transmitting mode in a specified channel and power level in all supported bands
- receiving mode in a specified channel to return the measured power level in all supported bands

The minimum recommended RF verification in production consists in forcing the module to transmit in a supported frequency the +UTEST AT command, and then checking that some power is emitted from the antenna system using any suitable power detector, power meter or equivalent equipment.

☞ See the SARA-R5 series AT commands manual [2] and SARA-R5 series application development guide [22] for the +UTEST AT command syntax description and detail guide of usage.

This feature allows the measurement of the transmitter and receiver power levels to check the component assembly related to the module cellular antenna interface and to check other device interfaces on which the RF performance depends.

⚠ To avoid module damage during a transmitter test, a suitable antenna according to module specifications or a 50 Ω termination must be connected to the **ANT** port.

⚠ To avoid module damage during a receiver test, the maximum power level received at the **ANT** port must meet module specifications.

☞ The +UTEST AT command sets the module to emit RF power ignoring LTE signaling protocol. This emission can generate interference that can be prohibited by law in some countries. The use of this feature is intended for testing purposes in controlled environments by qualified users and must not be used during the normal module operation. Follow the instructions suggested in the u-blox documentation. U-blox assumes no responsibilities for the inappropriate use of this feature.

Figure 77 illustrates a typical test setup for such an RF functional test.

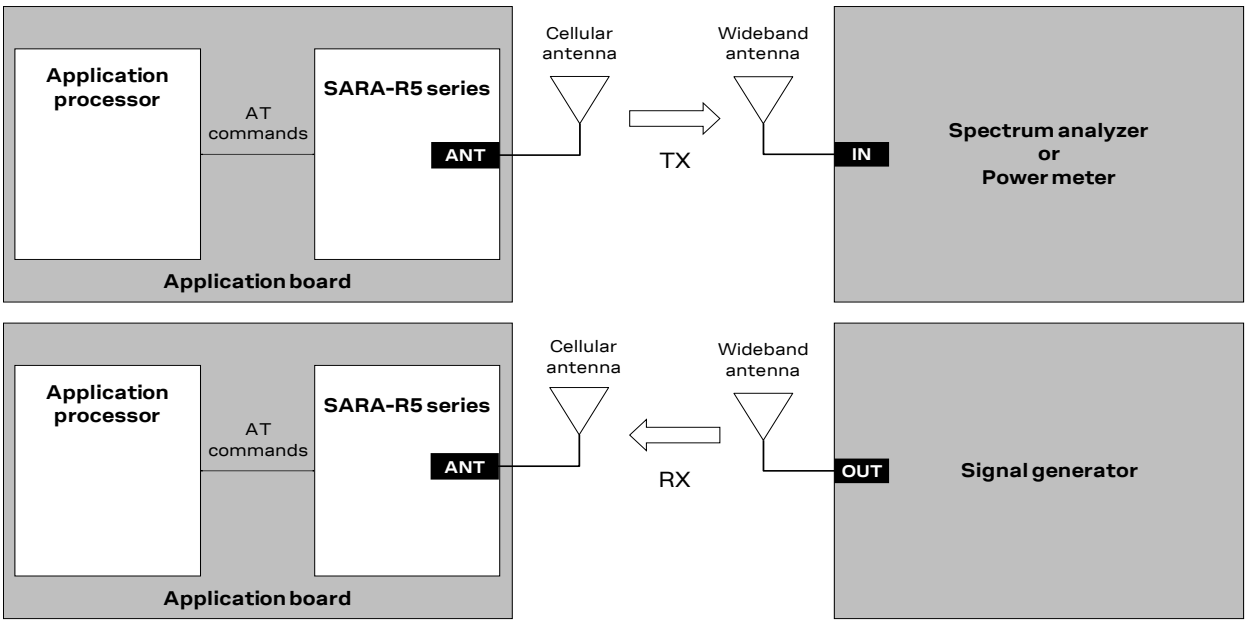

Figure 77: Setup with spectrum analyzer or power meter and signal generator for SARA-R5 series RF verification

5.2.3 GNSS RF functional tests

The best way to test the GNSS RF functionality is with the use of a Multi-GNSS generator, as it assures reliable and constant signals at every measurement.

u-blox recommends the following Multi-GNSS generator:

- Spirent GSS6300
  Spirent Communications Positioning Technology
  www.positioningtechnology.co.uk

Guidelines for GNSS RF functionality tests:

1. Connect a Multi-GNSS generator to the OEM product.
2. Choose the power level in a way that the “Golden Device” would report a C/No ratio of 38-40 dBHz.
3. Power up the DUT (Device Under Test) and allow enough time for the acquisition.
4. Read the C/No value from the NMEA GSV or the UBX-NAV-SVINFO message (e.g. with u-center).
5. Compare the results to a “Golden Device”.

Appendix

A Migration between SARA modules

Guidelines to migrate from u-blox SARA-G3, SARA-G4, SARA-U2, SARA-N2, SARA-N3, and SARA-R4 series modules to SARA-R5 series modules are available in the u-blox SARA modules migration guidelines application note [20].

B Glossary

Abbreviation	Definition
3GPP	3rd Generation Partnership Project
ADC	Analog to Digital Converter
AR	Axial Ratio
AT	AT Command Interpreter Software Subsystem, or attention
BeiDou	Chinese satellite navigation system
BJT	Bipolar Junction Transistor
C/No	Carrier to Noise ratio
C2PC	Class II Permissive Change
C4PC	Class IV Permissive Change
Cat	Category
CE	European Conformity
CMOS	Complementary Metal-Oxide-Semiconductor
CoAP	Constrained Application Protocol
CTS	Clear To Send
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DDC	Display Data Channel interface
DL	Down-Link (Reception)
DRX	Discontinuous Reception
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTLS	Datagram Transport Layer Security
DTR	Data Terminal Ready
eDRX	Extended Discontinuous Reception
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
ESD	Electro-Static Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
E-UTRA	Evolved Universal Terrestrial Radio Access
FCC	Federal Communications Commission United States
FDD	Frequency Division Duplex
FOAT	Firmware Over AT commands

Abbreviation	Definition
FOTA	Firmware Over The Air
FTP	File Transfer Protocol
FW	Firmware
Galileo	European satellite navigation system
GCF	Global Certification Forum
GLONASS	GLObal Navigation Satellite System (Russian satellite navigation system)
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
GPS	Global Positioning System
GSM	Global System for Mobile communication
HBM	Human Body Model
HDLC	High-level Data Link Control
HTTP	HyperText Transfer Protocol
HW	Hardware
I2C	Inter-Integrated Circuit interface
I2S	Inter IC Sound interface
IC	Integrated Circuit
IEC	International Electrotechnical Commission
IoT	Internet of Things
IP	Internet Protocol
IPC	Institute of Printed Circuits
ISED	Innovation, Science and Economic Development Canada
ISO	International Organization for Standardization
LDO	Low-Dropout
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
LPWA	Low Power Wide Area
LTE	Long Term Evolution
LwM2M	Open Mobile Alliance Lightweight Machine-to-Machine protocol
M2M	Machine-to-Machine
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MQTT	Message Queuing Telemetry Transport
MQTT-SN	Message Queuing Telemetry Transport for Sensor Networks
N/A	Not Applicable
NAS	Non Access Stratum
NB	Narrow Band
NTC	Negative Temperature Coefficient
OEM	Original Equipment Manufacturer device: an application device integrating a u-blox cellular module
OTA	Over The Air
PA	Power Amplifier
PCB	Printed Circuit Board
PCN	Product Change Notification / Sample Delivery Note / Information Note
PFM	Pulse Frequency Modulation
PIFA	Planar Inverted-F Antenna

Abbreviation	Definition
PPS	Pulse Per Second
PSM	Power Saving Mode
PTCRB	PCS Type Certification Review Board
PTW	Paging Time Window (during eDRX cycles)
PWM	Pulse Width Modulation
QZSS	Quasi-Zenith Satellite System
RAT	Radio Access Technology
RF	Radio Frequency
RI	Ring Indicator
RSSI	Received Signal Strength Indication
RSVD	Reserved
RTC	Real Time Clock
RTS	Request To Send
Rx	Receiver
SAIF	Sub-meter-class Augmentation with Integrity Function
SAW	Surface Acoustic Wave
SBAS	Satellite-Based Augmentation System
SDIO	Secure Digital Input Output
SIM	Subscriber Identification Module
SMA	Sub-Miniature version A
SMD	Surface Mounting Device
SMS	Short Message Service
SMT	Surface Mount Technology
SP4T	Single-Pole, 4-Throws
SPI	Serial Peripheral Interface
SQI	Serial Quad Input/Output
SRF	Self-Resonant Frequency
TBD	To Be Defined
TCP	Transmission Control Protocol
TCXO	Temperature-Controlled Crystal Oscillator
THT	Through-Hole Technology
TIS	Total Isotropic Sensitivity
TLS	Transport Layer Security
TP	Test Point
TRP	Total Radiated Power
Tx	Transmitter
UART	Universal Asynchronous Receiver-Transmitter
UDP	User Datagram Protocol
UICC	Universal Integrated Circuit Card
UL	Up-Link (Transmission)
URC	Unsolicited Result Code
USB	Universal Serial Bus
VSWR	Voltage Standing Wave Ratio

Table 46: Explanation of the abbreviations and terms used

Related documentation

[1] u-blox SARA-R5 series data sheet, UBX-19016638
[2] u-blox SARA-R5 series AT commands manual, UBX-19047455
[3] u-blox EVK-R5 user guide, UBX-19042592
[4] Universal Serial Bus revision 2.0 specification, https://www.usb.org/
[5] ITU-T recommendation V.24 – 02-2000 – List of definitions for interchange circuits between Data Terminal Equipment (DTE) and Data Circuit-terminating Equipment (DCE), http://www.itu.int/rec/T-REC-V.24-200002-I/en
[6] 3GPP TS 27.007 – AT command set for User Equipment (UE)
[7] 3GPP TS 27.005 – Use of Data Terminal Equipment – Data Circuit terminating; Equipment (DTE – DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
[8] 3GPP TS 27.010 – Terminal Equipment to User Equipment (TE-UE) multiplexer protocol
[9] u-blox mux implementation application note, UBX-13001887
[10] I2C-bus specification and user manual – UM10204 – NXP Semiconductors, https://www.nxp.com/docs/en/user-guide/UM10204.pdf
[11] GSM Association TS.09 – Battery Life Measurement and Current Consumption Technique, https://www.gsma.com/newsroom/wp-content/uploads//TS.09-v10.2.pdf
[12] 3GPP TS 36.521-1 – Evolved Universal Terrestrial Radio Access; User Equipment conformance specification; Radio transmission and reception; Part 1: Conformance Testing
[13] 3GPP TS 36.521-2 – Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment conformance specification; Radio transmission and reception; Part 2: Implementation Conformance Statement (ICS)
[14] 3GPP TS 36.523-2 – Evolved Universal Terrestrial Radio Access (E-UTRA) and Evolved Packet Core (EPC); User Equipment conformance specification; Part 2: Implementation Conformance Statement (ICS)
[15] u-blox end user test application note, UBX-13001922
[16] u-blox package information user guide, UBX-14001652
[17] u-blox B36 vehicle tracking blueprint product summary, UBX-20012630
[18] u-blox SARA-R5 / SARA-R4 positioning and timing implementation application note, UBX-20012413
[19] u-blox GNSS antennas application note, UBX-15030289
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[21] u-blox SARA-R5 series firmware update application note, UBX-20033314
[22] u-blox SARA-R5 series application development guide application note, UBX-20009652

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Revision history

Revision	Date	Name	Comments
R01	20-Dec-2019	fvid/psca/sses	Initial release
R02	10-Mar-2020	sses/fvid	Extended document applicability to SARA-R500S-00B Updated SARA-R510S-00B and SARA-R510M8S-00B product status Added regulatory certification approval info GPIO, power-on, power-off, reset sections updated Other minor corrections and clarifications
R03	15-Jul-2020	sses/fvid	Updated SARA-R5 series modules product status Revised certification approval info Added antenna trace design used for SARA-R5 series modules' type approvals Revised GPIO description section Revised VCC, Antennas, GNSS, UART, USB, I2C, GPIO design-in guidelines Other minor corrections and clarifications
R04	12-Oct-2020	sses/fvid	Updated SARA-R5 series modules product status Updated power-on, power-off and reset sections Added GITEKI certification Other minor corrections and clarifications
R05	22-Dec-2020	lpah	Extended document applicability to SARA-R500S-00B-01, SARA-R510S-00B-01, and SARA-R510M8S-00B-01. Other minor clarifications.
R06	11-May-2021	sses/fvid	Extended document applicability to SARA-R500S-01B, SARA-R510S-01B, and SARA-R510M8S-01B. Other minor clarifications.
R07	22-Jul-2021	sses/fvid	Updated power-off section. Other minor clarifications.

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