TEXAS INSTRUMENTS

TPD3S713-Q1

SLUSDH1 – MAY 2020

TPD3S713-Q1 Automotive USB 2.0 Interface Protection with Adjustable Current Limit and Short-to-V_{BATT} Protection

1 Features

- AEC-Q100 Qualified for automotive applications:
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
  - Device HBM ESD classification level H2
  - Device CDM ESD classification level C5
- Short-to-Battery (up to 18 V) and Short-to-Ground protection on V_{BUS} pin
- Short-to-Battery (up to 18 V) and Short-to-V_{BUS} protection on DM_IN, DP_IN pins
- DP_IN and DM_IN IEC 61000-4-2 Rated
  - ±8-kV Contact and ±15-kV air discharge
- High speed data switches (1230 MHz BW)
- 4.5-V to 5.5-V Input operating range
- 50-mA to 600-mA adjustable current limit (±13.5% at 200 mA)
- Integrated 73-mΩ (typical) High-Side MOSFET
- 500-mA Maximum continuous output current
- V_{BUS} Cable compensation
- 20-Pin QFN (3-mm × 4-mm) Package

2 Applications

- Automotive USB interface
  - Head unit
  - Telematics
  - Navigation module
- Automotive USB charging ports
  - Media interface

3 Description

The TPD3S713-Q1 is a single-chip solution for short-to-battery, short-circuit, and ESD protection for high speed data and power lines in automotive USB hub, head unit, telematics, and media interface applications. The integrated data switches provide best-in-class bandwidth for minimal signal degradation during USB short-to-battery events. The high bandwidth of 1.2 GHz allows for a clean USB2.0 high-speed 480 Mbps eye diagram with the long captive cables that are common in the automotive USB environment.

The short-to-battery protection isolates the internal system circuits from any overvoltage conditions at the V_{BUS}, DP_IN, and DM_IN pins. On these pins, the TPD3S713-Q1 can handle overvoltages up to 18 V for hot plug and DC events and shut off the internal switches to the upstream transceiver from harmful voltage and current spikes.

The V_{BUS} pin also provides an adjustable current limited load switch from 50 mA to 600 mA, which provides flexibility and also saves system power budget when the port requires only several tens of milliampere.

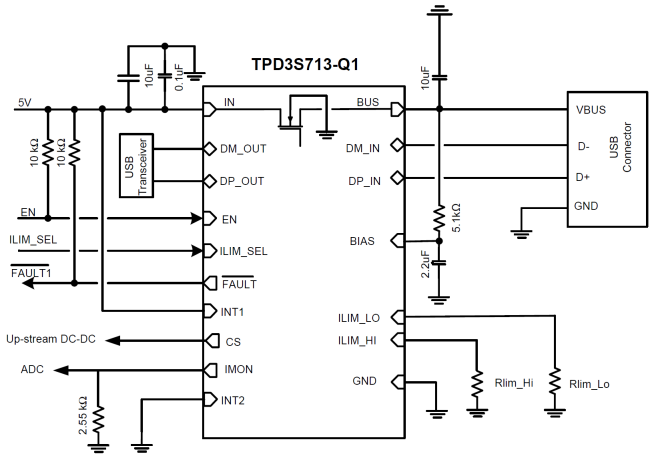
The TPD3S713-Q1 device has a current-sense output that is able to control an upstream supply, which allows it to maintain 5 V at the remote USB port connected after a long USB cables.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD3S713-Q1	WQFN (20)	3.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

DATE	REVISION	NOTES
May 2020	*	Initial Release

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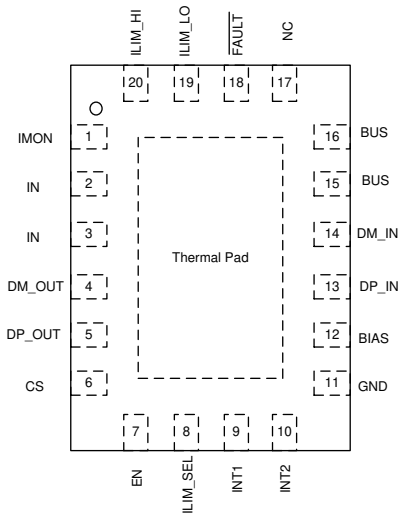
5 Pin Configuration and Functions

RVC Package
20-Pin WQFN
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IMON	1	O	This pin sources a scaled-down ratio of current through the internal FET. A resistor from this pin to GND converts current to proportional voltage; used as an analog current monitor.
IN	2,3	PWR	Input supply voltage; connect a 0.1-µF or greater ceramic capacitor from IN to GND as close to the IC as possible.
DM_OUT	4	I/O	DM data line to upstream USB host controller
DP_OUT	5	I/O	DP data line to upstream USB host controller
CS	6	O	Linear cable compensation current. Connect to divider resistor of front-end dc-dc converter.
EN	7	I	Logic-level control input for turning the power and signal switches on or off. When EN is low, the device is disabled, and the signal and power switches are OFF.
ILIM_SEL	8	I	Logic-level control input for choosing the current limit resistor and current limit threshold. When ILIM_SEL = High, ILIM_HI resistor is valid; When ILIM_SEL = Low, ILIM_LO resistor is valid.
INT1	9	I	Logic-level control input, the device can be set in normal mode or client mode through pin configuration. If INT1 = high, the device is in normal mode; If INT1 = low and ILIM_SEL = Low, the device is in client mode.
INT2	10	I	For internal circuit, must connect to ground without a pull down resistor.
GND	11	—	Ground connection; should be connected externally to the thermal pad.
BIAS	12	PWR	Used for IEC protection. Typically, connect a 2.2-µF capacitor to ground and 5.1 kΩ resistor to BUS.
DP_IN	13	I/O	DP data line to downstream connector
DM_IN	14	I/O	DM data line to downstream connector
BUS	15,16	PWR	Power-switch output
NC	17	NC	No connect, leave floating or connect to ground.
$\overline{\text{FAULT}}$	18	O	Active-low, open-drain output, asserted during overtemperature, overcurrent, and overvoltage conditions.
ILIM_LO	19	I	External resistor used to set the low current-limit threshold, selected by ILIM_SEL pin.
ILIM_HI	20	I	External resistor used to set the high current-limit threshold, selected by ILIM_SEL pin.
Thermal pad		—	Thermal pad on the bottom of the package

(1) I = Input, O = Output, I/O = Input and output, PWR = Power

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6 Specifications

6.1 Absolute Maximum Ratings

Voltages are with respect to GND unless otherwise noted(1)

		MIN	MAX	UNIT
Voltage range	CS, ILIM_SEL, INT1, EN, $\overline{\text{FAULT}}$, ILIM_HI, ILIM_LO, IN, IMON, INT2	–0.3	7	V
	DM_OUT, DP_OUT	–0.3	5.7	
	BIAS, DM_IN, DP_IN, VBUS	–0.3	18	
Continuous current	DM_IN to DM_OUT or DP_IN to DP_OUT	–100	100	mA
	IBUS	Internally limited		
Continuous output source current, I_{SRC}	ILIM_HI, LIM_LO, IMON	Internally limited		A
Continuous output sink current, I_{SNK}	$\overline{\text{FAULT}}$		25	mA
	CS	Internally limited		A
Operating junction temperature, T_J		–40	150	°C
Storage temperature,T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000(2)	V
		Charged-device model (CDM), per AEC Q100-011		±750(3)	
		IEC 61000-4-2 contact discharge	DP_IN and DM_IN pins(4)	±8000	
		IEC 61000-4-2 air discharge	DP_IN and DM_IN pins(4)	±15000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) The passing level per AEC-Q100 Classification H2.
(3) The passing level per AEC-Q100 Classification C5
(4) Surges per IEC 61000-4-2, level 4, 1999 applied from DP_IN and DM_IN to output ground of the TPD3S713Q1EVM-103 evaluation module.

6.3 Recommended Operating Conditions

Voltages are with respect to GND unless otherwise noted.

			MIN	NOM	MAX	UNIT
$V_{(IN)}$	Supply voltage	IN	4.5		5.5	V
	Input voltage	EN, ILIM_SEL, INT1, INT2	0		5.5	V
		DM_IN, DM_OUT, DP_IN, DP_OUT	0		3.6	V
$I_{(BUS)}$	Output continuous current	IBUS			500	mA
		DM_IN to DM_OUT or DP_IN to DP_OUT	–30		30	mA
	Continuous output sink current	$\overline{\text{FAULT}}$			10	mA
$R_{(ILIM_xx)}$	Current-limit-set resistors		6.98		100	kΩ
T_J	Operating junction temperature		–40		125	°C

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6.4 Thermal Information

THERMAL METRIC(1)		TPD3S713-Q1 RVC (WQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Unless otherwise noted, –40°C ≤ T_J ≤ 125°C and 4.5 V ≤ $V_{(IN)}$ ≤ 5.5 V, $V_{(EN)}$ = $V_{(INT1)}$ = $V_{(ILIM_SEL)}$ = $V_{(IN)}$, $V_{(INT2)}$ = GND, $R_{(FAULT)}$ = 10 kΩ, $R_{(IMON)}$ = 2.55 kΩ, $R_{(ILIM_HI)}$ = 52.3 kΩ. Positive currents are into pins. Typical values are at T_J = 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUT – POWER SWITCH						
$r_{DS(on)}$	On-resistance(1)	T_J = 25°C		73	90	mΩ
		–40°C ≤T_J ≤ 125°C		73	120	
I_{lkg}	Reverse leakage current	V_{BUS} = 5 V, V_{IN} = V_{EN} = 0 V, –40°C ≤ T_J ≤ 125°C, measure $I_{(IN)}$		0.01	2	µA
OUT – DISCHARGE						
$R_{(DCHG)}$	Discharge resistance (ILIM_SEL change)		400	500	630	Ω
ENABLE, ILIM_SEL, INT1, INT2 INPUTS						
	Input pin rising logic threshold voltage		0.8	1.35	2	V
	Input pin falling logic threshold voltage		0.7	1.15	1.65	V
	Hysteresis(2)			200		mV
	Input current	Pin voltage = 0 V or 5.5 V	–1		1	µA
CURRENT LIMIT						
I_{OS}	VBUS short-circuit current limit	R_{ILIM_HI} or R_{ILIM_LO} = 80.6 kΩ	38	55	71	mA
		R_{ILIM_HI} or R_{ILIM_LO} = 52.3 kΩ	62	82	102	
		R_{ILIM_HI} or R_{ILIM_LO} = 22.1 kΩ	166	192	218	
		R_{ILIM_HI} or R_{ILIM_LO} = 15.4 kΩ	245	275	305	
		R_{ILIM_HI} or R_{ILIM_LO} = 6.98 kΩ	560	600	640	
		R_{ILIM_HI} Shorted to GND	860	1150	1440	
R_{ILIM_HI} Shorted to GND						
$I_{(IN_OFF)}$	Disabled IN supply current	$V_{(EN)}$ = 0 V, $V_{(BUS)}$ = 0 V, –40°C ≤ T_J ≤ 125°C, no 5.1-kΩ resistor (open) between BIAS and VBUS		0.1	10	µA
$I_{(IN_ON)}$	Enabled IN supply current	$V_{(INT1)}$ = $V_{(ILIM_SEL)}$ = High		200	280	µA

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature. Thermal effects must be taken into account separately.
(2) This parameter is provided for reference only and does not constitute part of TI's published device specifications for purposes of TI's product warranty.

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Electrical Characteristics (continued)

Unless otherwise noted, –40°C ≤ T_J ≤ 125°C and 4.5 V ≤ $V_{(IN)}$ ≤ 5.5 V, $V_{(EN)}$ = $V_{(INT1)}$ = $V_{(ILIM_SEL)}$ = $V_{(IN)}$, $V_{(INT2)}$ = GND, $R_{(FAULT)}$ = 10 kΩ, $R_{(IMON)}$ = 2.55 kΩ, $R_{(ILIM_HI)}$ = 52.3 kΩ. Positive currents are into pins. Typical values are at T_J = 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UNDERVOLTAGE LOCKOUT, IN						
$V_{(UVLO)}$	UVLO threshold voltage	IN rising	3.9	4.1	4.3	V
		IN falling	3.3	3.5	3.7	
$\overline{FAULT}$						
	Output low voltage	$I_{(FAULT)}$ = 1 mA			100	mV
	Off-state leakage	$V_{(FAULT)}$ = 5.5 V			2	µA
THERMAL SHUTDOWN						
$T_{(OTSD2)}$	Thermal shutdown threshold		155			°C
$T_{(OTSD1)}$	Thermal shutdown threshold in current-limit		135			°C
	Hysteresis(3)			20		°C
DM_IN AND DP_IN OVERVOLTAGE PROTECTION						
$V_{(OV_Data)}$	Protection trip threshold	DP_IN and DM_IN rising	3.3	3.9	4.15	V
	Hysteresis(3)			100		mV
$R_{(DCHG_Data)}$	Discharge resistor after OVP(3)	DP_IN = DM_IN = 18 V, IN = 5 V or 0 V		200		kΩ
		DP_IN = DM_IN = 5 V, IN = 5 V		370		
		DP_IN = DM_IN = 5 V, IN = 0		390		
BUS OVERVOLTAGE PROTECTION						
$V_{(OV_BUS)}$	Protection trip threshold	VBUS rising	5.65	6	6.35	V
	Hysteresis(3)			90		mV
$R_{(DCHG_BUS)}$	Discharge resistor	VBUS = 18 V, IN = 5 V		55	85	kΩ
		VBUS = 18 V, IN = 0		80	120	
CABLE COMPENSATION						
$I_{(CS)}$	Sink current	Load = 0.5 A, 2.5 V ≤ $V_{(CS)}$ ≤ 5.5 V	190	210	230	µA

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Electrical Characteristics (continued)

Unless otherwise noted, –40°C ≤ T_J ≤ 125°C and 4.5 V ≤ $V_{(IN)}$ ≤ 5.5 V, $V_{(EN)}$ = $V_{(INT1)}$ = $V_{(ILIM_SEL)}$ = $V_{(IN)}$, $V_{(INT2)}$ = GND, $R_{(FAULT)}$ = 10 kΩ, $R_{(IMON)}$ = 2.55 kΩ, $R_{(ILIM_HI)}$ = 52.3 kΩ. Positive currents are into pins. Typical values are at T_J = 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT MONITOR OUTPUT (IMON)						
$I_{(IMON)}$	Source current	Load = 0.5 A, 0 ≤ $V_{(IMON)}$ ≤ 2.5 V	245	265	285	µA
HIGH-BANDWIDTH ANALOG SWITCH						
$R_{(HS_ON)}$	DP and DM switch on-resistance	$V_{(DP_OUT)}$ = $V_{(DM_OUT)}$ = 0 V, $I_{(DP_IN)}$ = $I_{(DM_IN)}$ = 30 mA		3.2	6.5	Ω
		$V_{(DP_OUT)}$ = $V_{(DM_OUT)}$ = 2.4 V, $I_{(DP_IN)}$ = $I_{(DM_IN)}$ = –15 mA		3.8	7.6	
$\lvert\Delta R_{(HS_ON)}\rvert$	Switch resistance mismatch between DP and DM channels	$V_{(DP_OUT)}$ = $V_{(DM_OUT)}$ = 0 V, $I_{(DP_IN)}$ = $I_{(DM_IN)}$ = 30 mA		0.05	0.15	Ω
		$V_{(DP_OUT)}$ = $V_{(DM_OUT)}$ = 2.4 V, $I_{(DP_IN)}$ = $I_{(DM_IN)}$ = –15 mA		0.05	0.15	
$C_{(IO_OFF)}$	DP and DM switch off-state capacitance(4)	V_{EN} = 0 V, $V_{(DP_IN)}$ = $V_{(DM_IN)}$ = 0.3 V, Vac = 0.03 V_{PP}, f = 1 MHz		8.8		pF
$C_{(IO_ON)}$	DP and DM switch on-state capacitance(4)	$V_{(DP_IN)}$ = $V_{(DM_IN)}$ = 0.3 V, Vac = 0.03 V_{PP}, f = 1 MHz		10.9		pF
	Off-state isolation(4)	$V_{(EN)}$ = 0 V, f = 250 MHz		12		dB
	On-state cross-channel isolation(4)	f = 250 MHz		34		dB
$I_{lkg(OFF)}$	Off-state leakage current	V_{EN} = 0 V, $V_{(DP_IN)}$ = $V_{(DM_IN)}$ = 3.6 V, $V_{(DP_OUT)}$ = $V_{(DM_OUT)}$ = 0 V, measure $I_{(DP_OUT)}$ and $I_{(DM_OUT)}$		0.1	1.5	µA
BW	Bandwidth (–3 dB)(4)	$R_{(L)}$ = 50 Ω		1230		MHz

(4) This parameter is provided for reference only and does not constitute part of TI's published device specifications for purposes of TI's product warranty.

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6.6 Switching Characteristics

Unless otherwise noted, –40°C ≤ T_J ≤ 125°C and 4.5 V ≤ $V_{(IN)}$ ≤ 5.5 V, $V_{(EN)}$ = $V_{(INT1)}$ = $V_{(ILIM_SEL)}$ = $V_{(IN)}$, $V_{(INT2)}$ = GND, $R_{(FAULT)}$ = 10 kΩ, $R_{(IMON)}$ = 2.55 kΩ, $R_{(ILIM_HI)}$ = 52.3 kΩ. Positive currents are into pins. Typical values are at T_J = 25°C. All voltages are with respect to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	BUS voltage rise time	$V_{(IN)}$ = 5 V, $C_{(L)}$ = 1 µF, $R_{(L)}$ = 100 Ω	1.05	1.75	3.1	ms
t_f	BUS voltage fall time		0.27	0.47	0.82	ms
t_{on}	BUS voltage turnon time	$V_{(IN)}$ = 5 V, $C_{(L)}$ = 1 µF, $R_{(L)}$ = 100 Ω		7.5	11	ms
t_{off}	BUS voltage turnoff time			2.7	5	ms
$t_{(DCHG_S)}$	Discharge hold time (ILIM_SEL change)	Time $V_{(OUT)}$ < 0.7V	1.1	2	2.9	s
$t_{(IOS)}$	BUS short-circuit response time(1)	$V_{(IN)}$ = 5 V, $R_{(SHORT)}$ = 50 mΩ		2		µs
$t_{(OC_BUS_FAULT)}$	BUS $\overline{FAULT}$ deglitch time	Bidirectional deglitch applicable to current-limit condition only (no deglitch assertion for OTSD)	5.5	8.5	11.5	ms
t_{pd}	Analog switch propagation delay (1)	$V_{(IN)}$ = 5 V		0.14		ns
$t_{(SK)}$	Analog switch skew between opposite transitions of the same port (t_{PHL} – t_{PLH}) (1)	$V_{(IN)}$ = 5 V		0.02		ns
$t_{(OV_Data)}$	DP_IN and DM_IN overvoltage protection response time			5		µs
$t_{(OV_BUS)}$	BUS overvoltage protection response time			0.3		µs
$t_{(OV_Data_FAULT)}$	DP_IN and DM_IN $\overline{FAULT}$-asserted degltich time		11	16	23	ms
	BUS $\overline{FAULT}$-asserted degltich time		11	16	23	ms

(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

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6.7 Typical Characteristics

T_A = 25°C, $V_{(IN)}$ = 5 V, $V_{(EN)}$ = $V_{(IN)}$, $V_{(ILIM_SEL)}$ = $V_{(INT1)}$ = $V_{(IN)}$, $V_{(INT2)}$ = GND, $\overline{FAULT}$ connect to $V_{(IN)}$ via a 10-kΩ pullup resistor (unless stated otherwise)

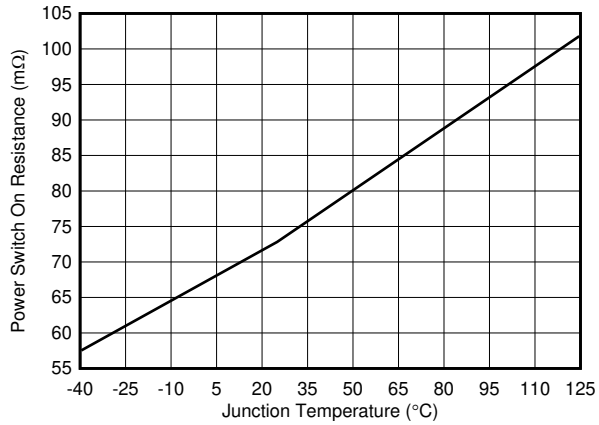

Figure 1. Power Switch On-Resistance vs Temperature

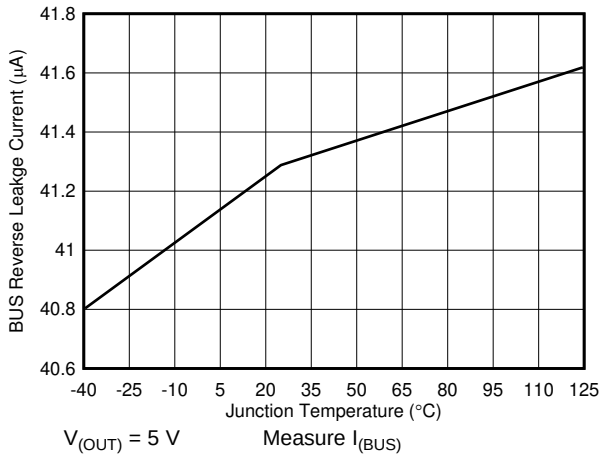

Figure 2. Reverse Leakage Current vs Temperature

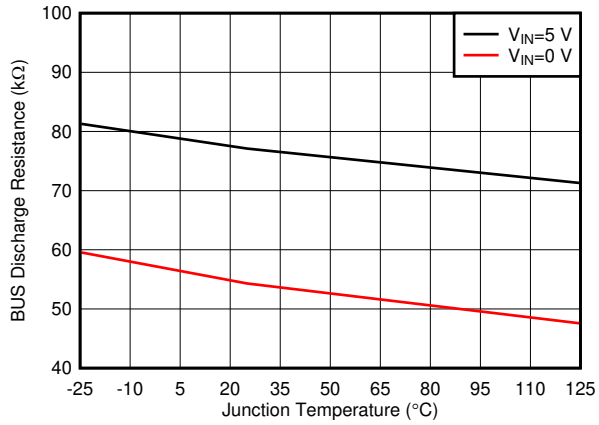

Figure 3. BUS Discharge Resistance (OVP) vs Temperature

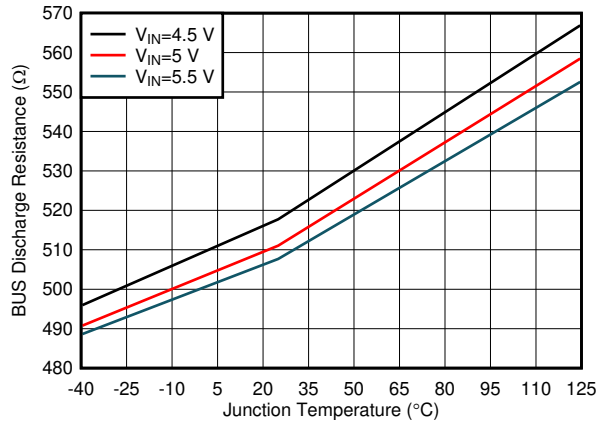

Figure 4. BUS Discharge Resistance (Mode Change) vs Temperature

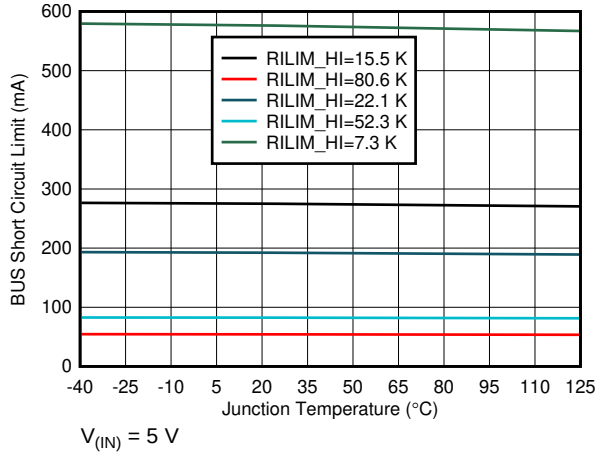

Figure 5. VBUS Short-Circuit Current Limit vs Temperature

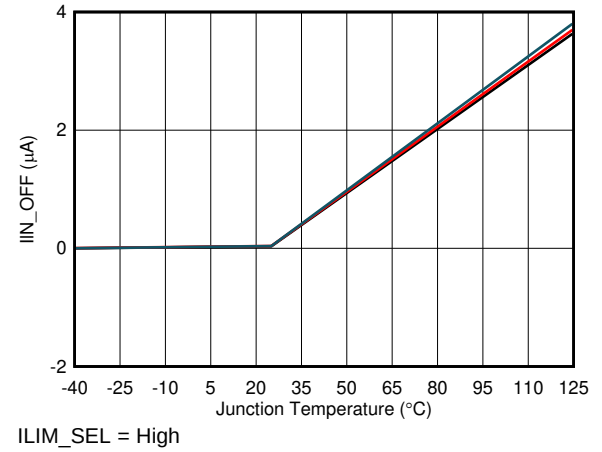

Figure 6. Disabled IN Supply Current vs Temperature

Typical Characteristics (continued)

T_A = 25°C, $V_{(IN)}$ = 5 V, $V_{(EN)}$ = $V_{(IN)}$, $V_{(ILIM_SEL)}$ = $V_{(INT1)}$ = $V_{(IN)}$, $V_{(INT2)}$ = GND, $\overline{FAULT}$ connect to $V_{(IN)}$ via a 10-kΩ pullup resistor (unless stated otherwise)

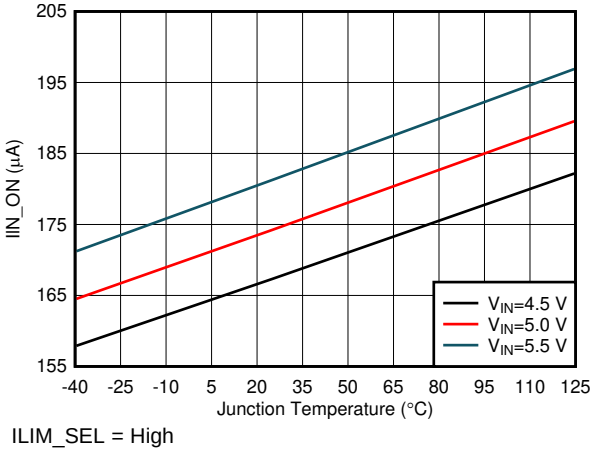

Figure 7. Enabled IN Supply Current vs Temperature

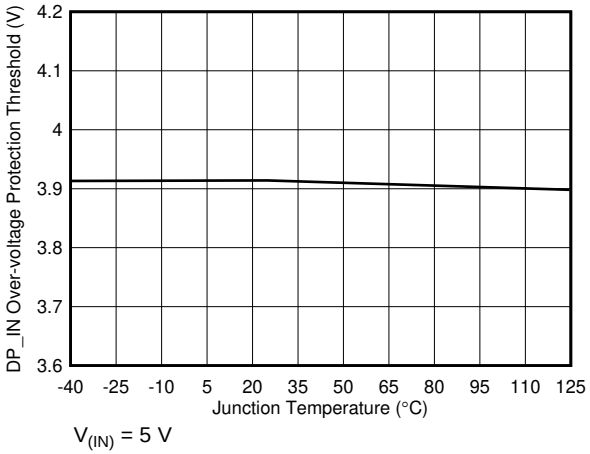

Figure 8. DP_IN Overvoltage Protection Threshold vs Temperature

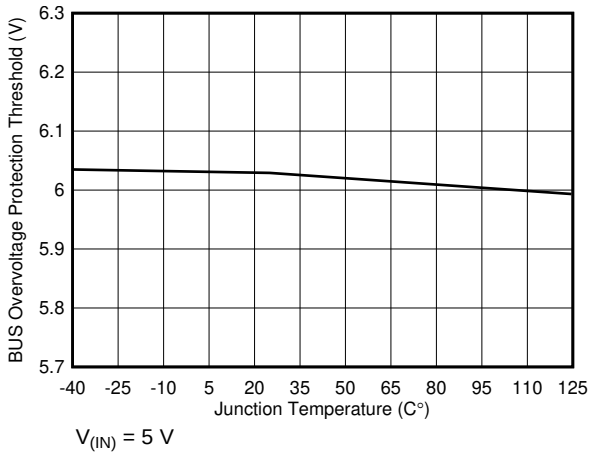

Figure 9. BUS Overvoltage Protection Threshold vs Temperature

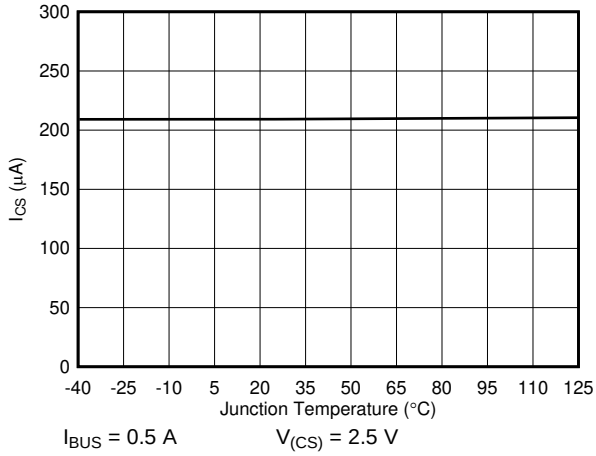

Figure 10. $I_{(CS)}$ vs Temperature

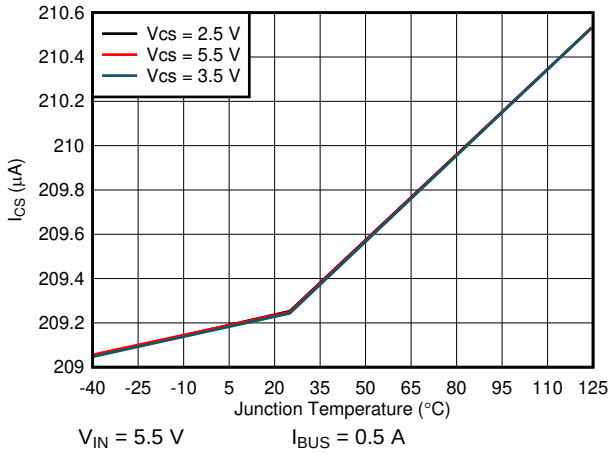

Figure 11. $I_{(CS)}$ vs $V_{(CS)}$ Voltage

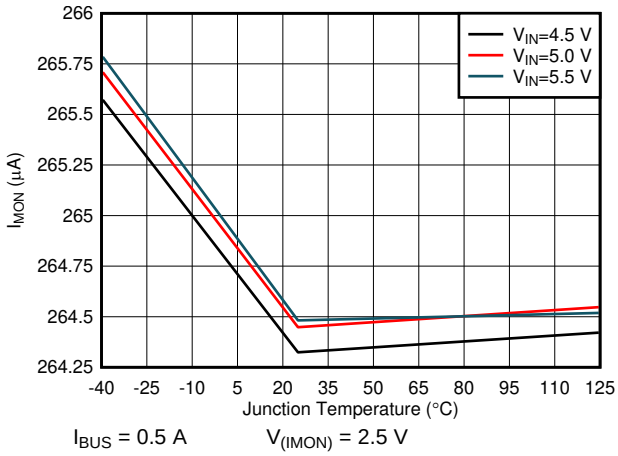

Figure 12. $I_{(IMON)}$ vs Temperature

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Typical Characteristics (continued)

T_A = 25°C, $V_{(IN)}$ = 5 V, $V_{(EN)}$ = $V_{(IN)}$, $V_{(ILIM_SEL)}$ = $V_{(INT1)}$ = $V_{(IN)}$, $V_{(INT2)}$ = GND, $\overline{FAULT}$ connect to $V_{(IN)}$ via a 10-kΩ pullup resistor (unless stated otherwise)

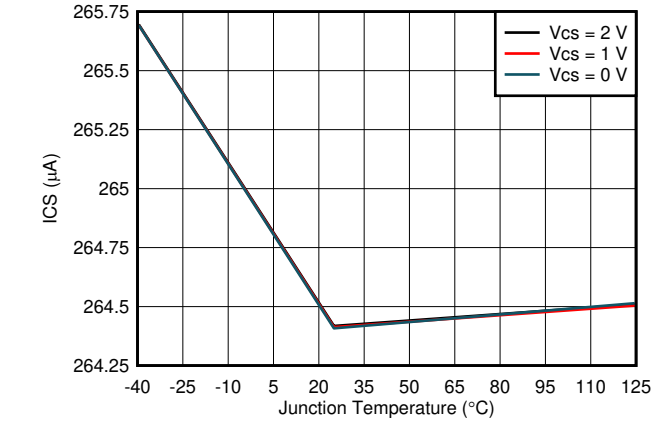
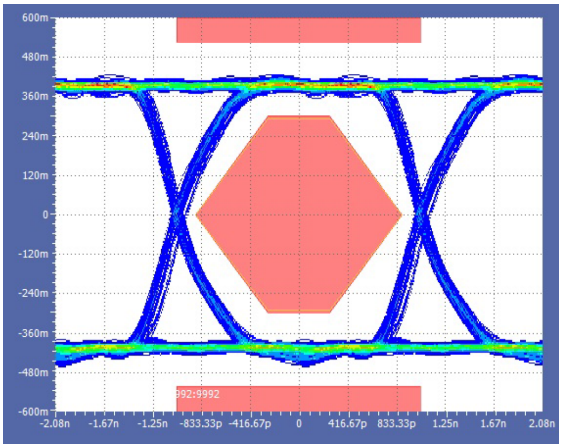


Figure 13. $I_{(IMON)}$ vs $V_{(CS)}$ Voltage

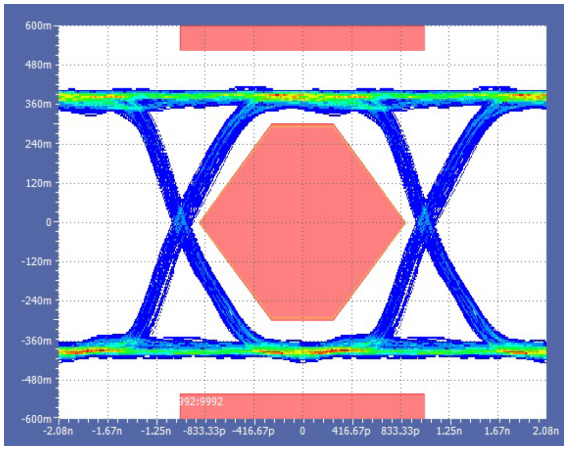
Typical Characteristics (continued)

T_A = 25°C, $V_{(IN)}$ = 5 V, $V_{(EN)}$ = $V_{(IN)}$, $V_{(ILIM_SEL)}$ = $V_{(INT1)}$ = $V_{(IN)}$, $V_{(INT2)}$ = GND, $\overline{FAULT}$ connect to $V_{(IN)}$ via a 10-kΩ pullup resistor (unless stated otherwise)



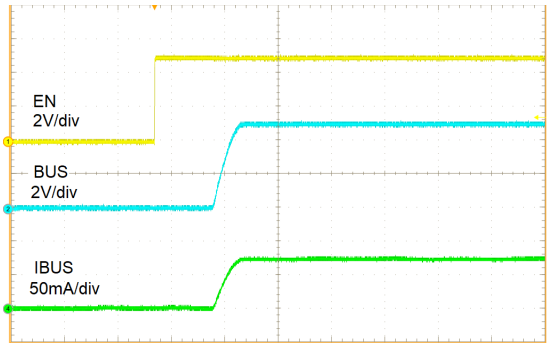
Measured on EVM with 10-cm cable

Figure 14. Bypassing the TPD3S713-Q1 Data Switch



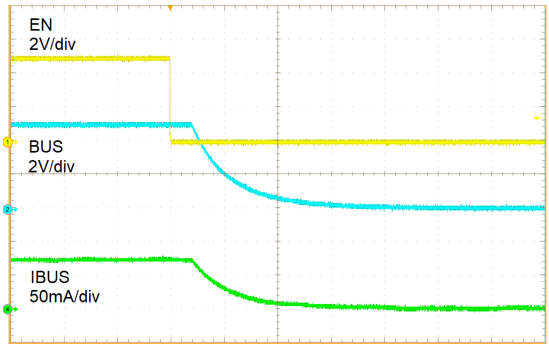
Measured on EVM with 10-cm cable

Figure 15. Through the TPD3S713-Q1 Data Switch



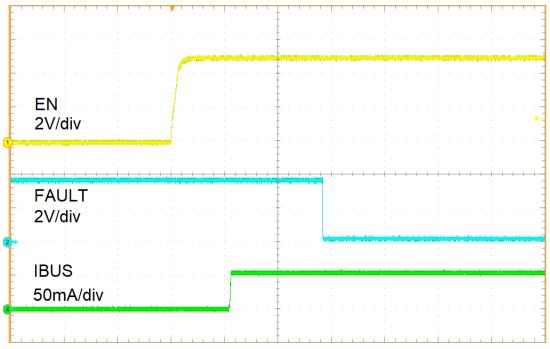
$R_{(LOAD)}$ = 68 Ω $C_{(LOAD)}$ = 10 µF t = 5 ms/div

Figure 16. Turnon Response



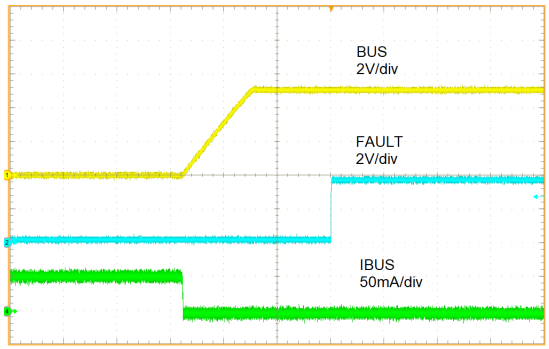
$R_{(LOAD)}$ = 68 Ω $C_{(LOAD)}$ = 10 µF t = 5 ms/div

Figure 17. Turnoff Response



$R_{(ILIM_LO)}$ = 80.6 kΩ t = 5 ms/div

Figure 18. Enable Into Short



$R_{(ILIM_HI)}$ = 80.6 kΩ t = 5 ms/div

Figure 19. Short Circuit to No Load

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Typical Characteristics (continued)

T_A = 25°C, $V_{(IN)}$ = 5 V, $V_{(EN)}$ = $V_{(IN)}$, $V_{(ILIM_SEL)}$ = $V_{(INT1)}$ = $V_{(IN)}$, $V_{(INT2)}$ = GND, $\overline{FAULT}$ connect to $V_{(IN)}$ via a 10-kΩ pullup resistor (unless stated otherwise)

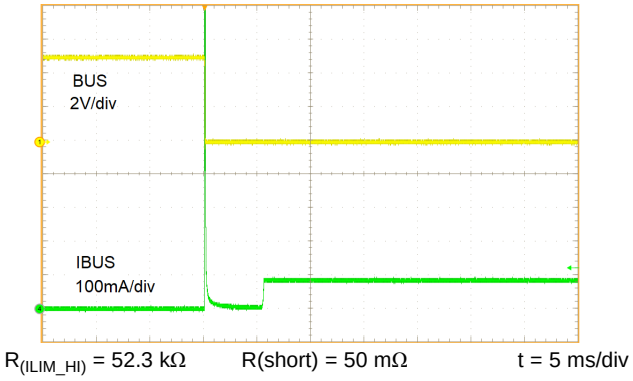

Figure 20. Hot Short

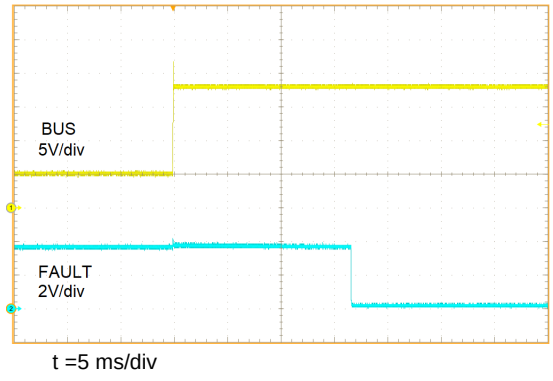

Figure 21. VBUS Short to Battery

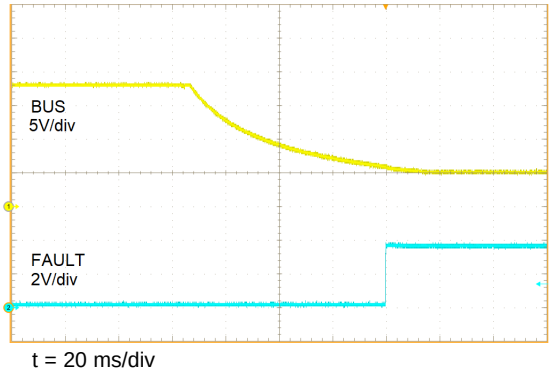

Figure 22. VBUS Short-to-Battery Recovery

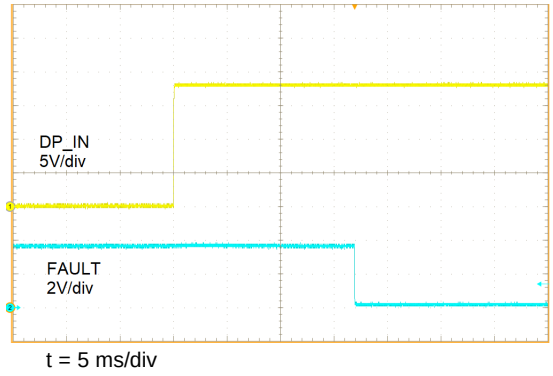

Figure 23. DP_IN Short to Battery

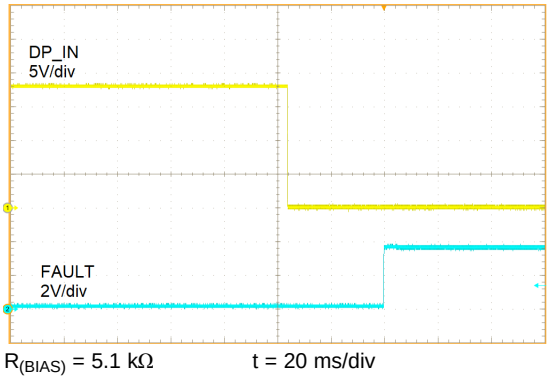

Figure 24. DP_IN Short-to-Battery Recovery

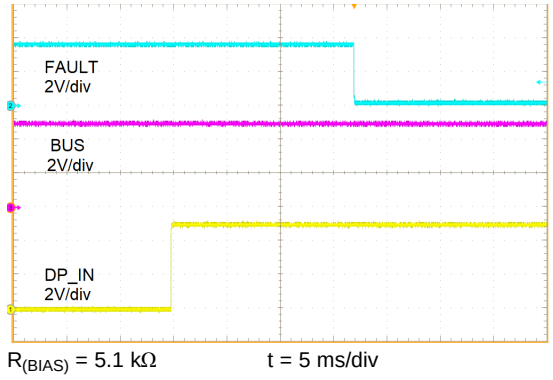

Figure 25. DP_IN Short to V_{BUS}

Typical Characteristics (continued)

T_A = 25°C, $V_{(IN)}$ = 5 V, $V_{(EN)}$ = $V_{(IN)}$, $V_{(ILIM_SEL)}$ = $V_{(INT1)}$ = $V_{(IN)}$, $V_{(INT2)}$ = GND, $\overline{FAULT}$ connect to $V_{(IN)}$ via a 10-kΩ pullup resistor (unless stated otherwise)

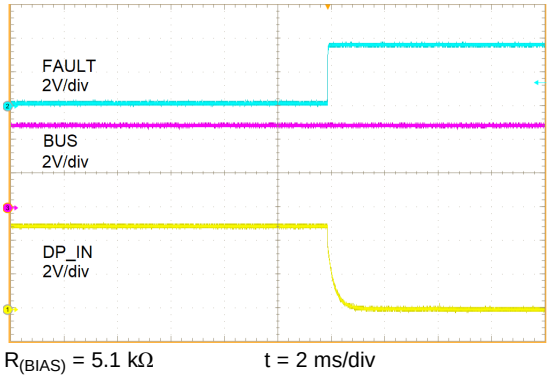

Figure 26. DP_IN Short-to-V_{BUS} and Recovery

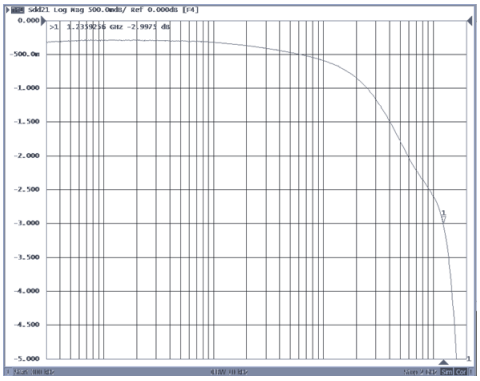

Figure 27. Data Transmission Characteristics vs Frequency

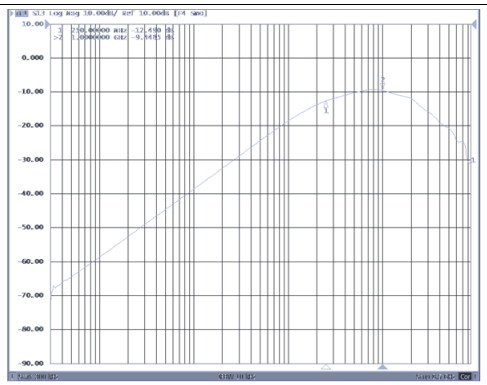

Figure 28. Off-State Data-Switch Isolation vs Frequency

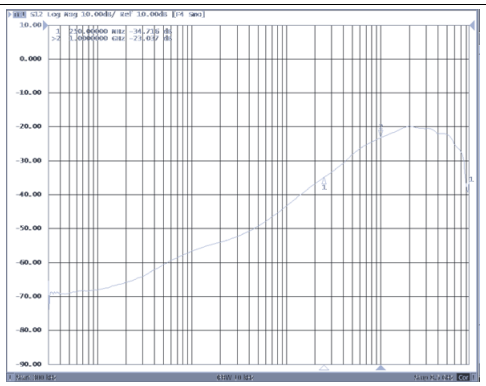

Figure 29. On-State Cross-Channel Isolation vs Frequency

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7 Parameter Measurement Information

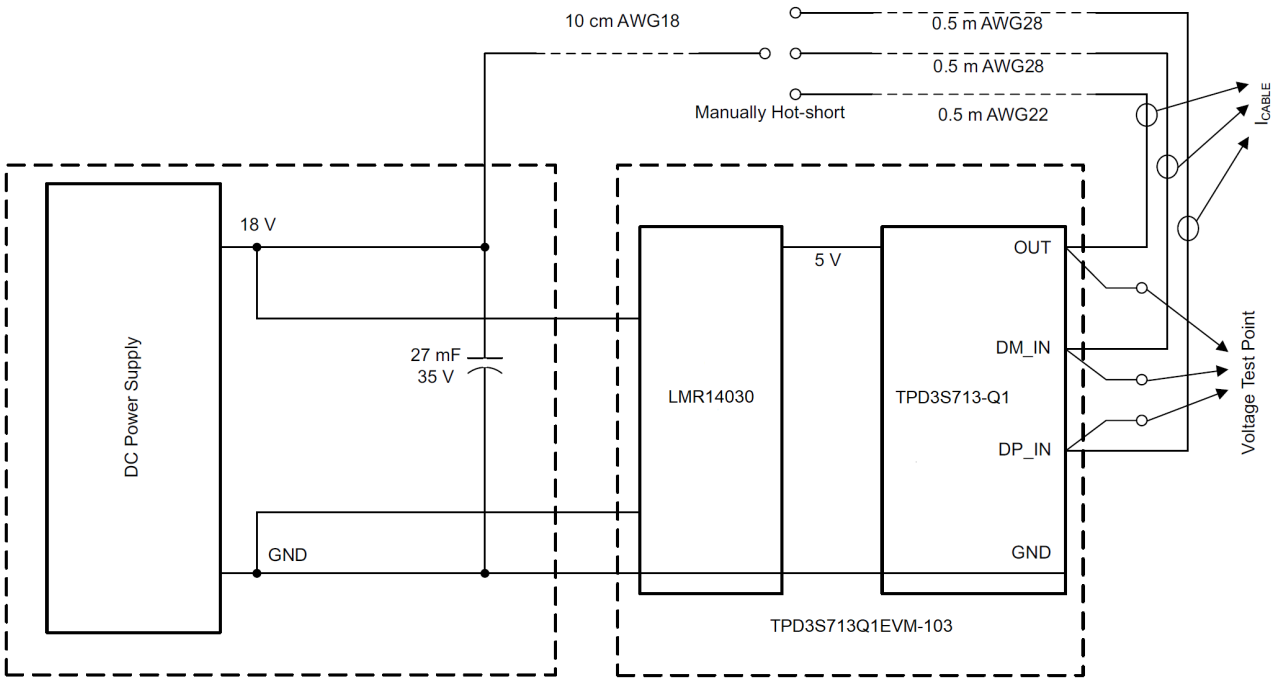

Figure 30. Short-to-Battery System Test Setup

8 Detailed Description

8.1 Overview

The TPD3S713-Q1 is a single-chip solution for short-to-battery, short-circuit, and ESD protection for high speed data and power lines in automotive USB hub, head unit, telematics, and media interface applications. The integrated data switches provide best-in-class bandwidth for minimal signal degradation during USB short-to-battery events. The high bandwidth allows for a clean USB2.0 high-speed eye diagram which helps pass stringent USB certification tests in the automotive USB environment.

The short-to-battery protection isolates the internal system circuits from any overvoltage conditions at the V_{BUS}, DP_IN, and DM_IN pins. On these pins, the TPD3S713-Q1 can handle overvoltages up to 18 V for hot plug and DC events. This protects the upstream voltage regulator, automotive processor, and hub when these pins are exposed to fault conditions.

The V_{BUS} pin also provides an accurate current limited load switch from 55 mA to 600 mA. The leading overcurrent protection automatically limits current to prevent drooping of the upstream rail during short-to-ground events. Also TPD3S713-Q1 can save power budget for the whole system.

The TPD3S713-Q1 device integrates a cable compensation (CS) feature to compensate for long-cable voltage drop. This keeps the remote USB port output voltage constant to enhance the user experience under high-current charging conditions.

The TPD3S713-Q1 device provides a current-monitor function (IMON) by connecting a resistor from the IMON pin to GND to provide a positive voltage linearly with load current. This can be used for system power or dynamic power management.

Additionally, the device provides ESD protection up to ±8 kV (contact discharge) and ±15 kV (air discharge) per IEC 61000-4-2 on DP_IN and DM_IN.

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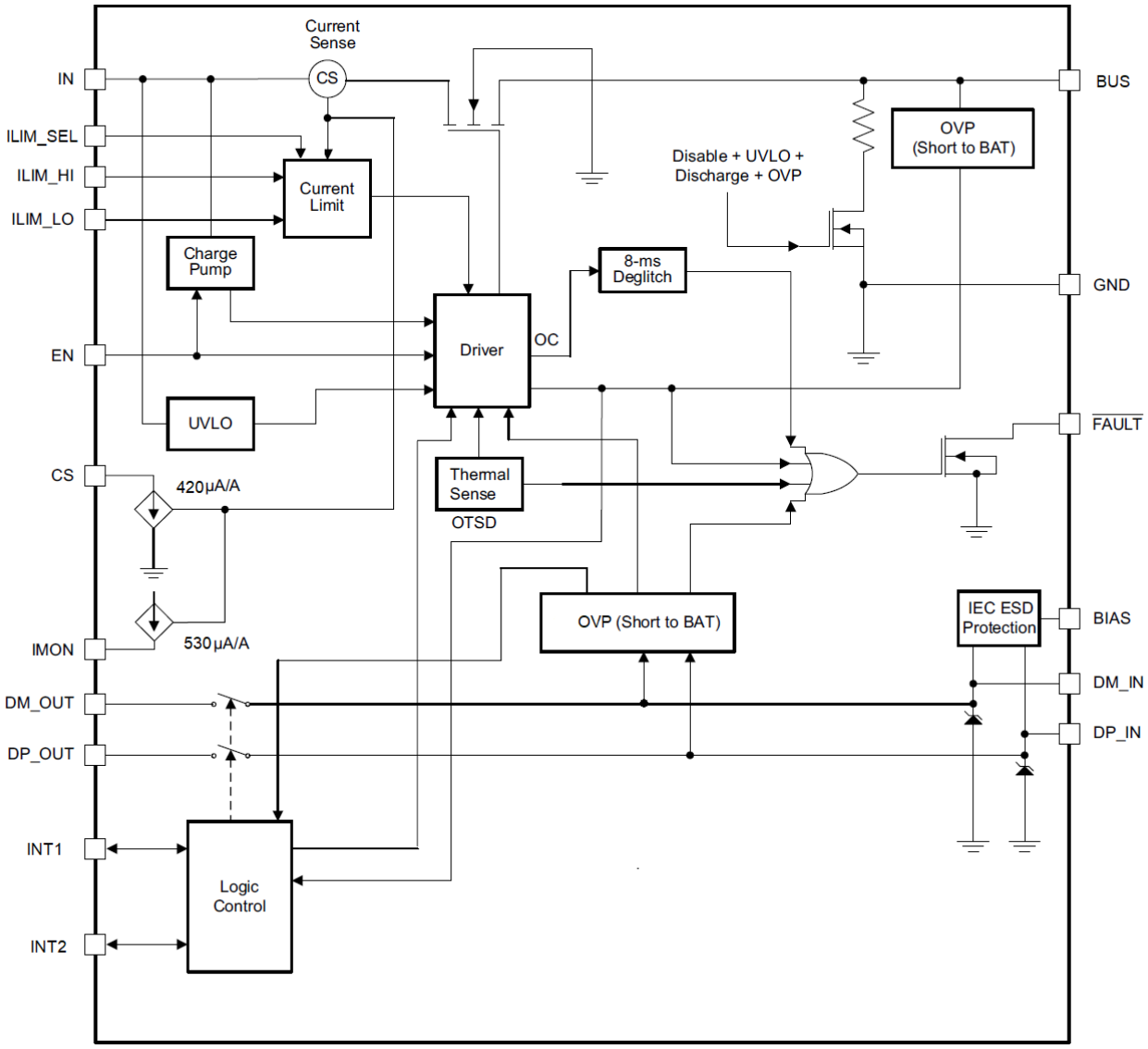
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 $\overline{\text{FAULT}}$ Response

The device features an active-low, open-drain fault output. $\overline{\text{FAULT}}$ goes low when there is a fault condition. Fault detection includes overtemperature, overcurrent, or overvoltage on V_{BUS}, DP_IN and DM_IN. Connect a 10-kΩ pullup resistor from $\overline{\text{FAULT}}$ to IN.

Table 1 summarizes the conditions that generate a fault and actions taken by the device.

Feature Description (continued)

Table 1. Fault Conditions

EVENT	CONDITION	ACTION
Overvoltage on the data lines	$V_{(DP_IN)}$ or $V_{(DM_IN)}$ > 3.9 V	The device immediately shuts off the USB data switches and the internal power switch. The fault indicator asserts with a 16-ms deglitch, and deasserts without deglitch.
Overvoltage on $V_{(BUS)}$	$V_{(BUS)}$ > 6 V	The device immediately shuts off the internal power switch and the USB data switches. The fault indicator asserts with a 16-ms deglitch and deasserts without deglitch.
Overcurrent on $V_{(BUS)}$	$I_{(BUS)}$ > $I_{(OS)}$	The device regulates switch current at $I_{(OS)}$ until thermal cycling occurs. The fault indicator asserts and deasserts with an 8-ms deglitch.
Overtemperature	T_J > OTSD2 in non-current-limited or T_J > OTSD1 in current-limited mode.	The device immediately shuts off the internal power switch and the USB data switches. The fault indicator asserts immediately when the junction temperature exceeds OTSD2 or OTSD1 while in a current-limiting condition. The device has a thermal hysteresis of 20°C.

8.3.2 Cable Compensation

When a load draws current through a long or thin wire, there is an IR drop that reduces the voltage delivered to the load. In the vehicle from the voltage regulator 5-V output to the loading, the total resistance of power switch $r_{DS(on)}$ and cable resistance causes an IR drop at the loading input. So the charging current of most portable devices is less than their expected maximum charging current.

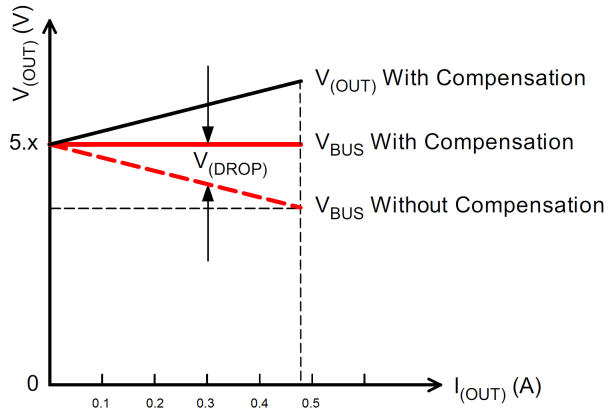


Figure 31. Voltage Drop

The TPD3S713-Q1 device detects the load current and applies a proportional sink current that can be used to adjust the output voltage of the upstream regulator to compensate for the IR drop in the charging path. The gain $G_{(CS)}$ of the sink current proportional to load current is 420 µA/A.

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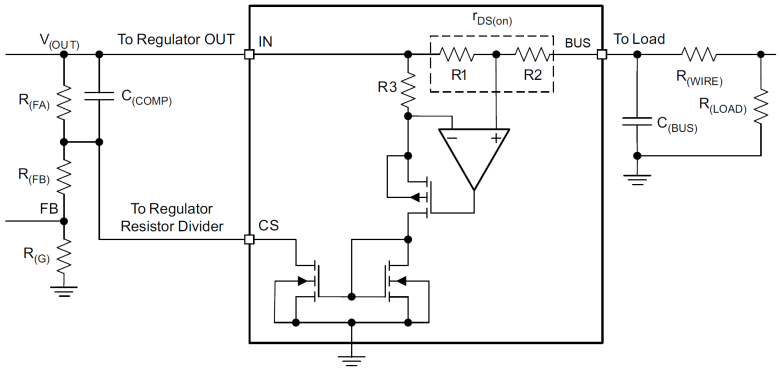

Figure 32. Cable Compensation Equivalent Circuit

8.3.2.1 Design Procedure

To start the procedure, the total resistance, including the power switch $r_{DS(on)}$ and wire resistance $R_{(WIRE)}$, must be known.

1. Choose $R_{(G)}$ following the voltage-regulator feedback resistor-divider design guideline.
2. Calculate $R_{(FA)}$ according to Equation 1.

$$R_{FA} = (r_{DS(on)} + R_{(WIRE)}) / G_{(CS)} \quad (1)$$

3. Calculate $R_{(FB)}$ according to Equation 2.

$$R_{(FB)} = \frac{V_{(OUT)}}{V_{(FB)} / R_{(G)}} - R_{(G)} - R_{(FA)} \quad (2)$$

4. $C_{(COMP)}$ in parallel with $R_{(FA)}$ is required to stablilize $V_{(OUT)}$ when $C_{(BUS)}$ is large. Start with $C_{(COMP)} \geq 3 \times G_{(CS)} \times C_{(OUT)}$, then adjust $C_{(COMP)}$ to optimize the load transient of the voltage regulator output. $V_{(OUT)}$ stability should always be verified in the end application circuit.

8.3.3 DP and DM Protection

DP and DM protection consists of ESD and OVP (overvoltage protection). The DP_IN and DM_IN pins provide ESD protection up to ±15 kV (air discharge) and ±8 kV (contact discharge) per IEC 61000-4-2 (see the *ESD Ratings* section for test conditions).

The ESD stress seen at DP_IN and DM_IN is impacted by many external factors, like the parasitic resistance and inductance between ESD test points and the DP_IN and DM_IN pins. For air discharge, the temperature and humidity of the environment can cause some difference, so the IEC performance should always be verified in the end-application circuit.

The IEC ESD performance of the TPD3S713-Q1 device depends on the capacitance connected from BIAS to GND. A 2.2-µF capacitor placed close to the BIAS pin is recommended. Connect the BIAS pin to BUS using a 5.1-kΩ resistor as a discharge path for the ESD stress.

OVP protection is provided for short-to-V_{BUS} or short-to-battery conditions in the vehicle harness, preventing damage to the upstream USB transceiver or hub. When the voltage on DP_IN or DM_IN exceeds 3.9 V (typical), the TPD3S713-Q1 device quickly responds to block the high-voltage reverse connection to DP_OUT and DM_OUT. Overcurrent short-to-GND protection for DP and DM is provided by the upstream USB transceiver.

8.3.4 V_{BUS} OVP Protection

The TPD3S713-Q1 BUS pin can withstand up to 18 V. The internal MOSFET turns off quickly when a short-to-battery condition occurs.

The TPD3S713-Q1 device OVP thresholds is 6 V (typical).

8.3.5 Output and DP or DM Discharge

When an OVP condition occurs on DP_IN or DM_IN, the TPD3S713-Q1 device enables an internal 200-kΩ discharge resistance from DP_IN to ground and from DM_IN to ground. The analog switches are also turned off. The TPD3S713-Q1 device automatically disables the discharge paths and turns on the analog switches once the OVP condition is removed.

When an OVP condition occurs on BUS, the TPD3S713-Q1 device turns on an internal discharge path (see Table 2 for the discharge resistance). The TPD3S713-Q1 device automatically turns off the discharge path and turns on the power switch once the OVP condition is removed.

Table 2. BUS Discharge Resistance

VIN(1)	EN(1)	OVP(1)	BUS DISCHARGE RESISTANCE(2)
0	0	0	—
0	0	1	80 kΩ
0	1	0	—
0	1	1	80 kΩ
1	0	0	500 Ω
1	0	1	55 kΩ
1	1	0	—
1	1	1	55 kΩ

(1) 0 = inactive, 1 = active
(2) — = no discharge resistance

8.3.6 Overcurrent Protection

When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur. In the first condition, the output is shorted before the device is enabled or before the application of $V_{(IN)}$. The TPD3S713-Q1 device senses the short and immediately switches into a constant-current output. In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents flow for 1 to 2 μs (typical) before the current-limit circuit reacts. The device operates in constant-current mode after the current-limit circuit has responded. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting. The device remains off until the junction temperature cools approximately 20°C and then restarts. The device continues to cycle on and off until the overcurrent condition is removed.

8.3.7 Undervoltage Lockout

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turnon threshold. Built-in hysteresis prevents unwanted oscillations on the output due to input voltage drop from large current surges.

8.3.8 Thermal Sensing

Two independent thermal-sensing circuits protect the TPD3S713-Q1 device if the temperature exceeds recommended operating conditions. These circuits monitor the operating temperature of the power-distribution switch and disable operation. The power dissipation in the package is proportional to the voltage drop across the power switch, so the junction temperature rises during an overcurrent condition. The first thermal sensor turns off the power switch when the die temperature exceeds 135ºC and the device is in current limit. The second thermal sensor turns off the power switch when the die temperature exceeds 155ºC regardless of whether the power switch is in current limit. Hysteresis is built into both thermal sensors, and the switch turns on after the device has cooled by approximately 20°C. The switch continues to cycle off and then on until the fault is removed. The open-drain false-reporting output, $\overline{\text{FAULT}}$, is asserted (low) during an overtemperature shutdown condition.

8.3.9 Current-Limit Setting

The TPD3S713-Q1 has two independent current-limit settings that are each adjusted externally with a resistor. The ILIM_HI setting is adjusted with $R_{(ILIM_HI)}$ connected between ILIM_HI and GND. The ILIM_LO setting is adjusted with $R_{(ILIM_LO)}$ connected between ILIM_LO and GND.

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The current limit is selected by ILIM_SEL pin. If ILIM_SEL = high, ILIM_HI will be selected; If ILIM_SEL = low, ILIM_LO will be selected.

The following equation calculates the value of resistor for adjusting the typical current limit (need update):

$$I_{os(nom)}(\text{mA}) = \frac{4200\text{V}}{R_{(ILIM_xx)}{}^{0.99}\,k\Omega} \tag{3}$$

Many applications require that the current limit meet specific tolerance limits. When designing to these tolerance limits, both the tolerance of the TPD3S713-Q1 current limit and the tolerance of the external adjusting resistor must be taken into account. The following equations approximate the TPD3S713-Q1 minimum and maximum current limits to within a few milliamperes and are appropriate for design purposes. The equations do not constitute part of TI's published device specifications for purposes of TI's product warranty. These equations assume an ideal—no variation—external adjusting resistor. To take resistor tolerance into account, first determine the minimum and maximum resistor values based on its tolerance specifications and use these values in the equations. Because of the inverse relation between the current limit and the adjusting resistor, use the maximum resistor value in the $I_{OS(min)}$ equation and the minimum resistor value in the $I_{OS(max)}$ equation.

$$I_{os(min)}(\text{mA}) = \frac{4150\text{V}}{R_{(ILIM_xx)}{}^{1.05}\,k\Omega} \tag{4}$$

$$I_{os(max)}(\text{mA}) = \frac{4600\text{V}}{R_{(ILIM_xx)}{}^{0.96}\,k\Omega} \tag{5}$$

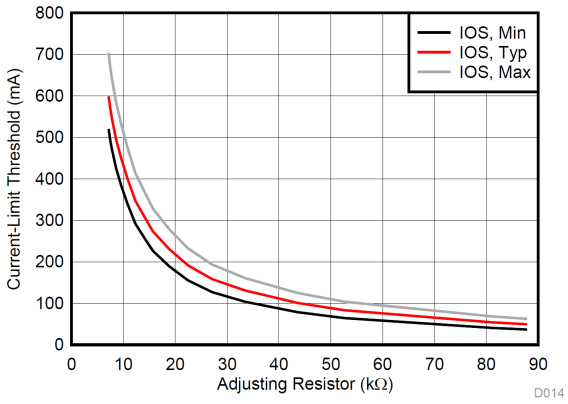

Figure 33. Current-Limit Setting vs Adjusting Resistor

The routing of the traces to the $R_{(ILIM_xx)}$ resistors should have a sufficiently low resistance so as not to affect the current-limit accuracy. The ground connection for the $R_{(ILIM_xx)}$ resistors is also very important. The resistors must reference back to the TPD3S713-Q1 GND pin. Follow normal board layout practices to ensure that current flow from other parts of the board does not impact the ground potential between the resistors and the TPD3S713-Q1 GND pin.

8.4 Device Functional Modes

8.4.1 Device Truth Table (TT)

The device truth table (Table 3) lists all valid combinations for both ILIM_SEL and INT1 pins, and the corresponding mode. The TPD3S713-Q1 device monitors the INT1 and ILIMI_SEL input change, and there will be 2s discharge on BUS pin during mode change.

Device Functional Modes (continued)

Table 3. Truth Table

INT1	ILIM_SEL	CURRENT LIMIT SELECTED	MODE	Power Switch	Data Switch	IMON FOR CURRENT MONITOR	$\overline{\text{FAULT}}$ REPORT
0	0	N/A	Client mode	OFF	ON	OFF	ON(1)
0	1	RESERVED, DO NOT USE					
1	0	ILIM_LO	Normal mode	ON	ON	ON	ON
1	1	ILIM_HI	Normal mode	ON	ON	ON	ON

(1) In the client mode ,the FAULT only report in case of BUS,DP_IN and DM_IN OVP.

8.4.2 Client Mode

The TPD3S713-Q1 device integrates client mode as shown in Figure 34. The internal power switch is OFF to block current flow from BUS to IN, and the signal switches are ON. This mode can be used for software upgrades from the USB port.

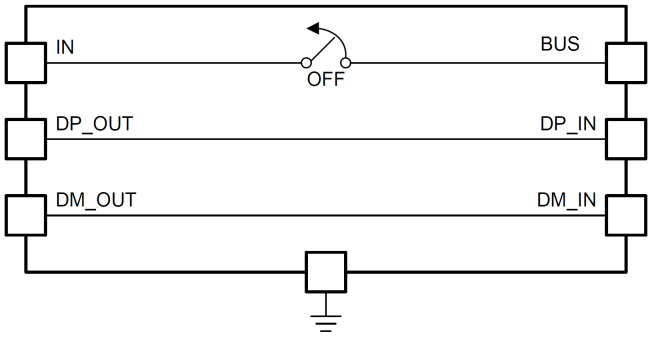

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Figure 34. Client-Mode Equivalent Circuit

In client mode, because the power switch is OFF, BUS must be 5 V so that the device can work normally (usually powered by an external downstream USB port). If the BUS voltage is low, the communication may not work properly.

8.4.3 High-Bandwidth Data-Line Switch

The DP and DM data lines pass through the device. A wide-bandwidth signal switch allows data to pass through the device without corrupting signal integrity. The data-line switches are turned on in any of the operating modes. The EN input must be at logic high for the data-line switches to be enabled.

NOTE

- While in client and normal mode, the data switches are ON.
- The data switches are only for the USB-2.0 differential pair. In the case of a USB-3.0 host, the super-speed differential pairs must be routed directly to the USB connector without passing through the TPD3S713-Q1 device.
- Data switches are OFF during BUS (V_{BUS}) discharge.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPD3S713-Q1 device is a USB power switch with cable compensation and short-to-battery protection for V_{BUS}, DP, and DM. The device is typically used for automotive USB port protection. The following design procedure can be used to select components for the TPD3S713-Q1 device. This section presents a simplified discussion of how to choose external components for V_{BUS}, DP, and DM short-to-battery protection.

9.2 Typical Application

For an automotive USB charging port, the V_{BUS}, DP, and DM pins are exposed and require a protection device. The protection required includes V_{BUS} overcurrent, DP and DM ESD protection, and short-to-battery protection. This charging-port device protects the upstream dc-dc converter (bus line) and automotive SOC or hub chips (DP and DM data lines). An application schematic of this circuit with short-to-battery protection is shown in Figure 35.

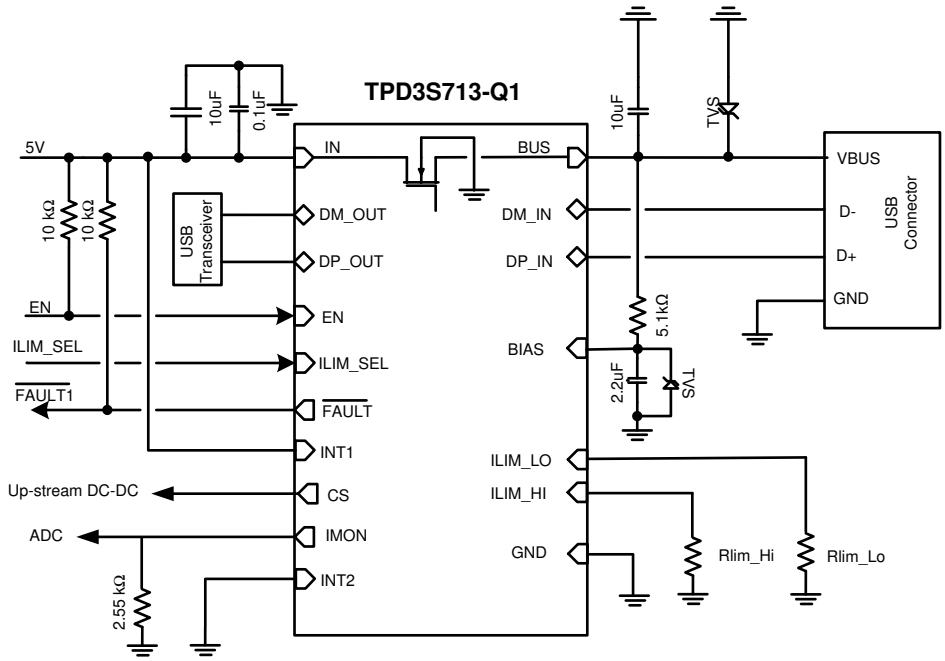

Figure 35. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the following as the input parameters.

DESIGN PARAMETER	EXAMPLE VALUE
Battery voltage, $V_{(BAT)}$	18 V
Short-circuit cable	0.5 m

9.2.2 Detailed Design Procedure

To begin the design process, the designer must know the following:

- The battery voltage
- The short-circuit cable length
- The maximum continuous output current for the USB port. The minimum current-limit setting of TPD3S713-Q1 device must be higher than this current.
- The maximum output current of the upstream dc-dc converter. The maximum current-limit setting of TPD3S713-Q1 device must be lower than this current.
- For cable compensation, the total resistance including power switch $r_{DS(on)}$, cable resistance, and connector contact resistance must be specified.

9.2.2.1 Input Capacitance

Consider the following application situations when choosing the input capacitors.

For all applications, TI recommends a 0.1-µF or greater ceramic bypass capacitor between IN and GND, placed as close as possible to the device for local noise decoupling.

During output short or hot plug-in of a capacitive load, high current flows through the TPD3S713-Q1 device back to the upstream dc-dc converter until the TPD3S713-Q1 device responds (after $t_{(IOS)}$). During this response time, the TPD3S713-Q1 input capacitance and the dc-dc converter output capacitance source current to keep V_{IN} above the UVLO of the TPD3S713-Q1 device and any shared circuits. Size the input capacitance for the expected transient conditions and keep the path between the TPD3S713-Q1 device and the dc-dc converter short to help minimize voltage drops.

Input voltage overshoots can be caused by either of two effects. The first cause is an abrupt application of input voltage in conjunction with input power-bus inductance and input capacitance when the IN pin is in the high-impedance state (before turnon). Theoretically, the peak voltage is 2 times the applied voltage. The second cause is due to the abrupt reduction of output short-circuit current when the TPD3S713-Q1 device turns off and energy stored in the input inductance drives the input voltage high. Applications with large input inductance (for example, a connection between the evaluation board and the bench power supply through long cables) may require large input capacitance to prevent the voltage overshoot from exceeding the absolute-maximum voltage of the device.

During the short-to-battery (EN = HIGH) condition, the input voltage follows the output voltage until OVP protection is triggered ($t_{(OV_BUS)}$). After the TPD3S713-Q1 device responds and turns off the power switch, the stored energy in the input inductance can cause ringing.

Based on the three situations described, 10-µF and 0.1-µF low-ESR ceramic capacitors, placed close to the input, are recommended.

9.2.2.2 Output Capacitance

Consider the following application situations when choosing the output capacitors.

After an output short occurs, the TPD3S713-Q1 device abruptly reduces the BUS current, and the energy stored in the output power-bus inductance causes voltage undershoot and potentially reverse voltage as it discharges.

Applications with large output inductance (such as from a cable) benefit from the use of a high-value output capacitor to control the voltage undershoot.

For USB port applications, because the V_{BUS} pin is exposed to IEC61000-4-2 level-4 ESD, use a low-ESR capacitance to protect BUS.

The TPD3S713-Q1 device is capable of handling up to 18-V battery voltage. When V_{BUS} is shorted to the battery, the LCR tank circuit formed can induce ringing. The peak voltage seen on the BUS pin depends on the short-circuit cable length. The parasitic inductance and resistance varies with length, causing the damping factor and peak voltage to differ. Longer cables with larger resistance reduce the peak current and peak voltage. Consider high-voltage derating for the ceramic capacitor, because the peak voltage can be higher than twice the battery voltage.

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Based on the three situations described, a 10-µF, 35-V, X7R, 1210 low-ESR ceramic capacitor placed close to BUS is recommended. If the battery voltage is 16 V and a 16-V transient voltage suppressor (TVS) is used, then the capacitor voltage can be reduced to 25 V. Considering temperature variation, placing an additional 35-V aluminum electrolytic capacitor can lower the peak voltage and make the system more robust.

9.2.2.3 BIAS Capacitance

The capacitance on the BIAS pin helps the IEC ESD performance on the DM_IN and DP_IN pins.

When a short to battery on DP_IN, DM_IN and/or BUS occurs, high voltage can be seen on the BIAS pin. Place a 2.2-µF, 50-V, X7R, 0805, low-ESR ceramic capacitor close to the BIAS pin. The whole current path from BIAS to GND should be as short as possible. Additionally, use a 5.1-kΩ discharge resistor from BIAS to BUS.

9.2.2.4 Output and BIAS TVS

The TPD3S713-Q1 device can withstand high transient voltages up to 18 V. In real application, the ringing may exceed 18V due to LCR tank ringing, but in order to make BUS, DP_IN, and DM_IN robust, place one TVS close to the BUS pin, and another TVS close to the BIAS pin. When choosing the TVS, the reverse standoff voltage V_R depends on the battery voltage (16 V or 18 V). Considering the peak pulse power capability, a 400-W device is recommended such as an SMAJ16 for a 16-V battery or an SMAJ18 for an 18-V battery.

9.2.3 Application Curves

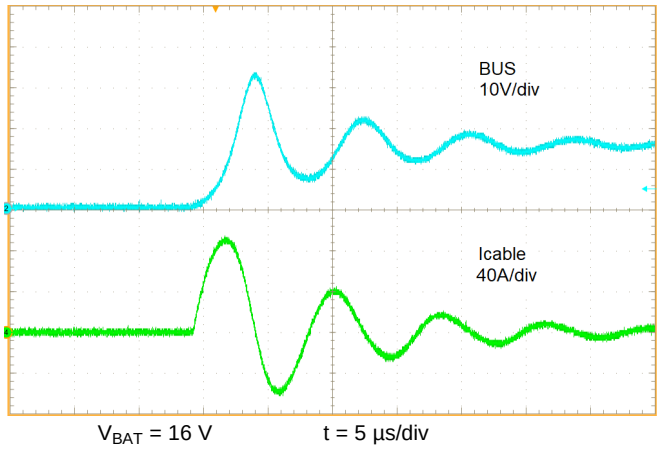

Figure 36. Disabled, 25-V, 1206, X7R C_{OUT} Capacitor Without SMAJ16

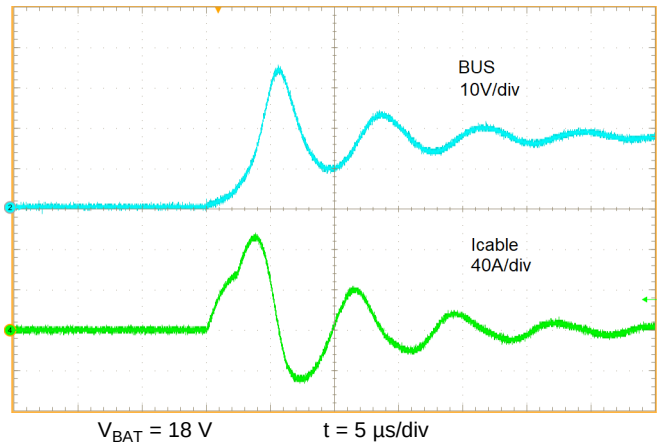

Figure 37. Disabled, 35-V, 1210, X7R C_{OUT} Capacitor Without SMAJ18

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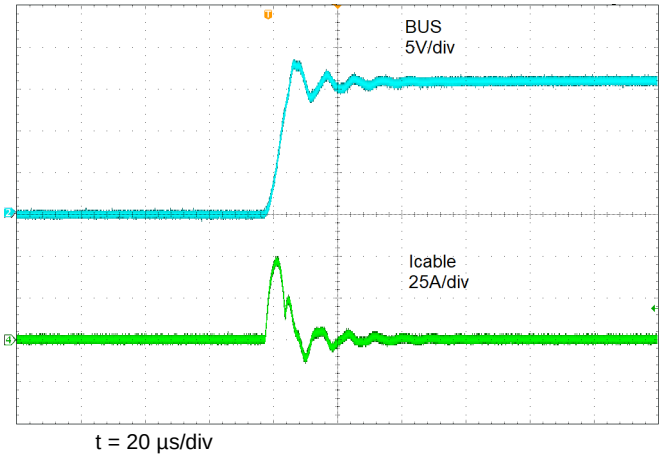

Figure 38. Disabled, 25-V, 1206, X7R C_{OUT} Capacitor With SMAJ16, BUS Shorted to Battery

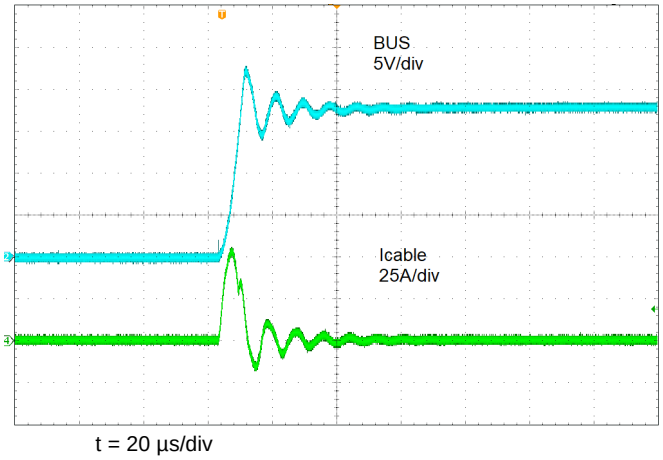

Figure 39. Disabled, 35-V, 1210, X7R C_{OUT} Capacitor With SMAJ18, BUS Shorted to Battery

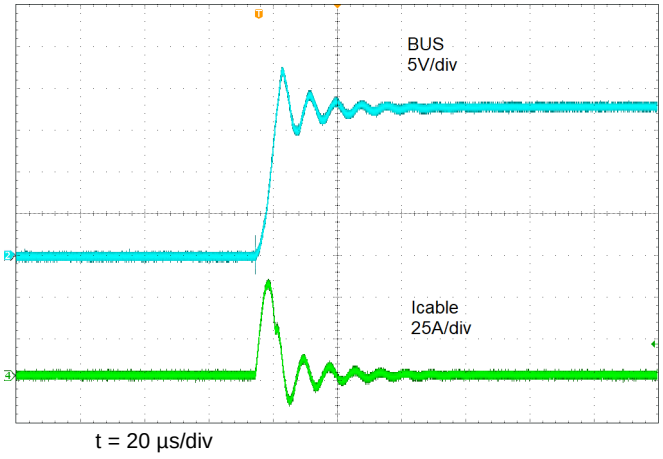

Figure 40. DC-DC VIN Floating, BUS Shorted to Battery

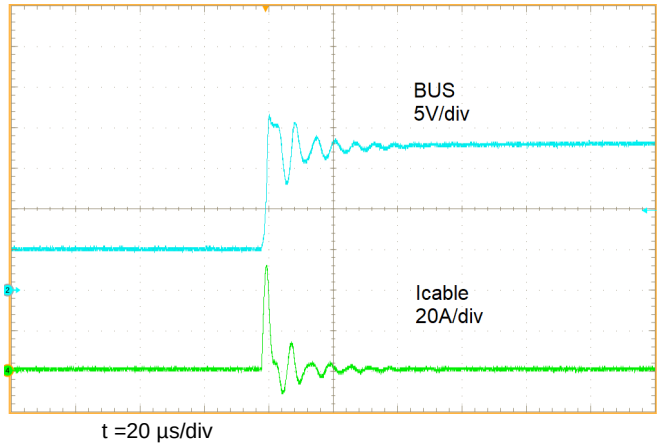

Figure 41. Enable BUS Shorted to Battery

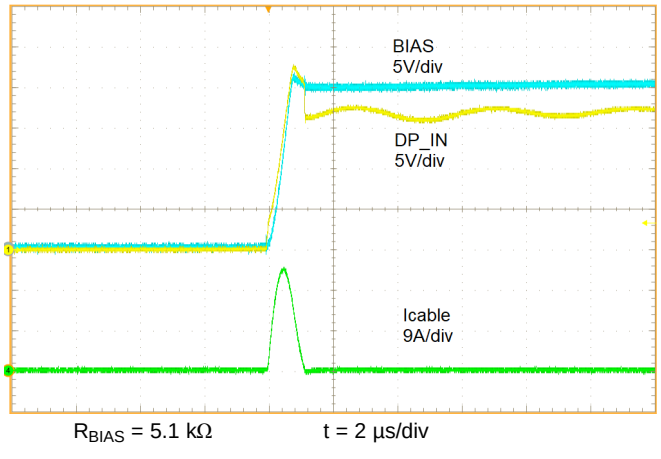

Figure 42. Disabled, DP_IN Shorted to Battery

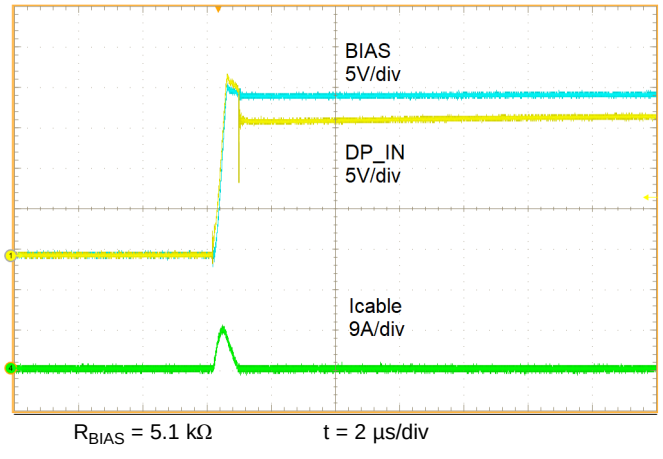

Figure 43. DC-DC VIN Floating, DP_IN Shorted to Battery

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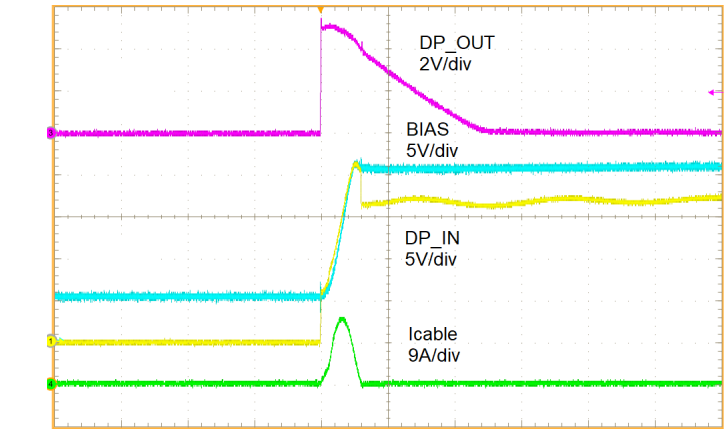

Figure 44. Enabled, DP_IN Shorted to Battery

10 Power Supply Recommendations

The TPD3S713-Q1 device is designed for a supply voltage range of 4.5 V ≤ V_{IN} ≤ 5.5 V, with its power switch used for protecting the upstream power supply when a fault such as overcurrent or short to ground occurs on the USB port. Therefore, the power supply should be rated higher than the current-limit setting to avoid voltage drops during overcurrent or short-circuit conditions.

11 Layout

11.1 Layout Guidelines

Layout best practices for the TPD3S713-Q1 device are listed as follows.

- Considerations for input and output power traces
  - Make the power traces as short as possible.
  - Make the power traces as wide as possible.
- Considerations for input-capacitor traces
  - For all applications, 10-µF and 0.1-µF low-ESR ceramic capacitors are recommended, placed close to the IN pin.
- The resistors attached to the ILIM_HI and ILIM_LO pins of the device have several requirements.
  - It is recommended to use 1% low-temperature-coefficient resistors.
  - The trace routing between these two pins and GND should be as short as possible to reduce parasitic effects on current limit. These traces should not have any coupling to switching signals on the board.
- Locate all TPD3S713-Q1 pullup resistors for open-drain outputs close to their connection pin. Pullup resistors should be 100 kΩ.
  - If a particular open-drain output is not used or needed in the system, tie it to GND.
- ESD considerations
  - The TPD3S713-Q1 device has built-in ESD protection for DP_IN and DM_IN. Keep trace lengths minimal from the USB connector to the DP_IN and DM_IN pins on the TPD3S713-Q1 device, and use minimal vias along the traces.
  - The capacitor on BIAS helps to improve the IEC ESD performance. A 2.2-µF capacitor should be placed close to BIAS, and the current path from BIAS to GND across this capacitor should be as short as possible. Do not use vias along the connection traces.
  - A 10-µF output capacitor should be placed close to the BUS pin and TVS.
  - See the *ESD Protection Layout Guide* (SLVA680) for additional information.
- TVS Considerations (BUS, DP_IN and DM_IN exceed 18V)
  - For BUS, a TVS like SMAJ18 should be placed near the BUS pin.

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Layout Guidelines (continued)

  - For BIAS, a TVS like SMAJ18 should be placed close to the BIAS pin, but behind the 2.2-µF capacitor.
  - The whole path from BUS to GND or BIAS to GND across the TVS should be as short as possible.
- DP_IN, DM_IN, DP_OUT, and DM_OUT routing considerations
  - Route these traces as microstrips with nominal differential impedance of 90 Ω.
  - Minimize the use of vias on the high-speed data lines.
  - Keep the reference GND plane devoid from cuts or splits above the differential pairs to prevent impedance discontinuities.
  - For more USB 2.0 high-speed D+ and D– differential routing information, see the *High Speed USB Platform Design Guideline* from Intel.
- Thermal Considerations
  - When properly mounted, the thermal-pad package provides significantly greater cooling ability than an ordinary package. To operate at rated power, the thermal pad must be soldered to the board GND plane directly under the device. The thermal pad is at GND potential and can be connected using multiple vias to inner-layer GND. Other planes, such as the bottom side of the circuit board, can be used to increase heat sinking in higher-current applications. See the *PowerPad™ Thermally Enhanced Package* application report (SLMA002) and *PowerPAD™ Made Easy* application brief (SLMA004) for more information on using this thermal pad package.

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11.2 Layout Example

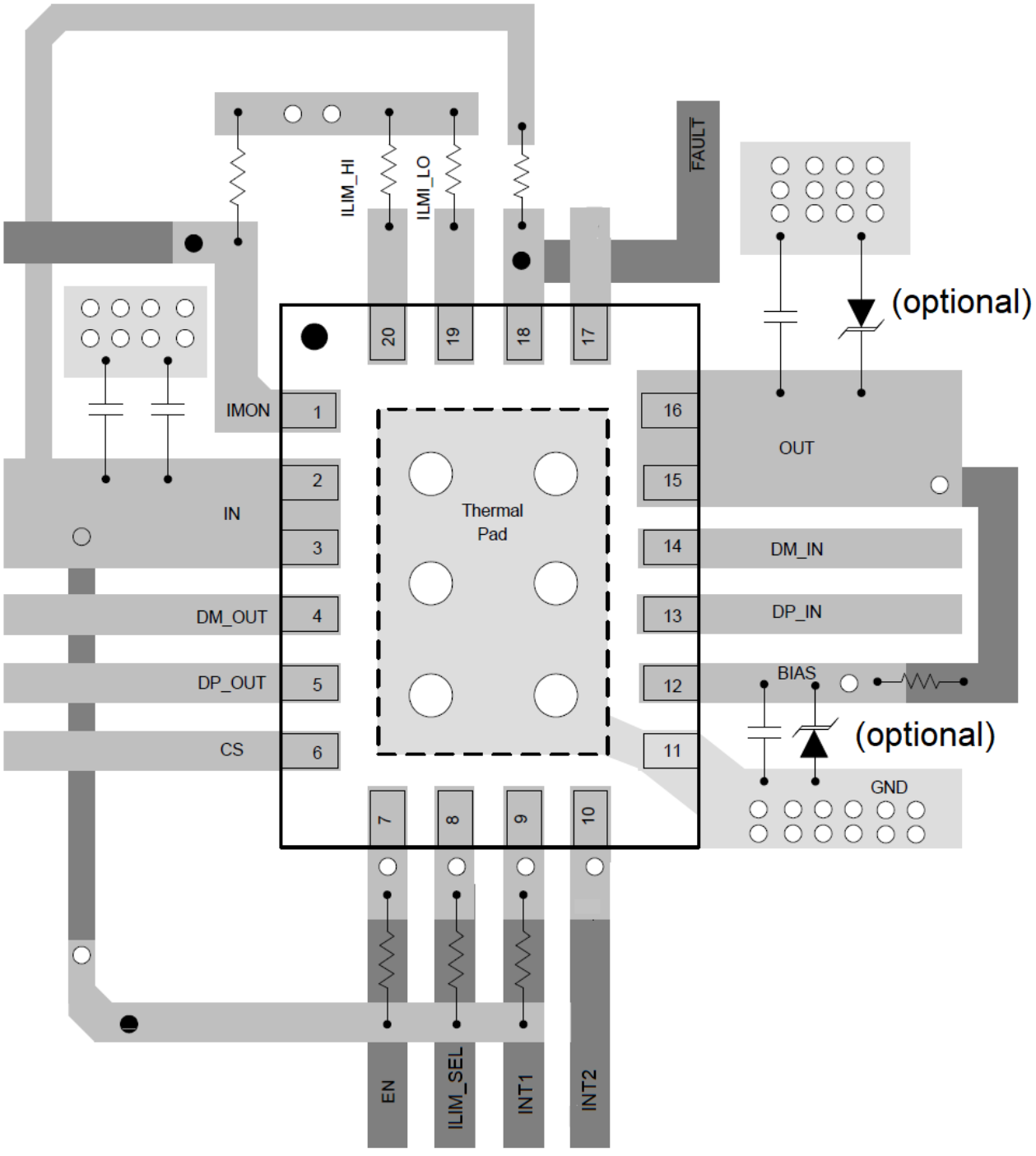

Figure 45. TPD3S713-Q1 Layout Diagram

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *High Speed USB Platform Design Guidelines Intel*
- *ESD Protection Layout Guide*
- *PowerPAD™ Thermally Enhanced Package*
- *PowerPAD™ Made Easy*

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 Trademarks

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is a trademark of ~PowerPAD.
is a trademark of ~PowerPad.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD3S713QRVCRQ1	ACTIVE	WQFN	RVC	20	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	3S713Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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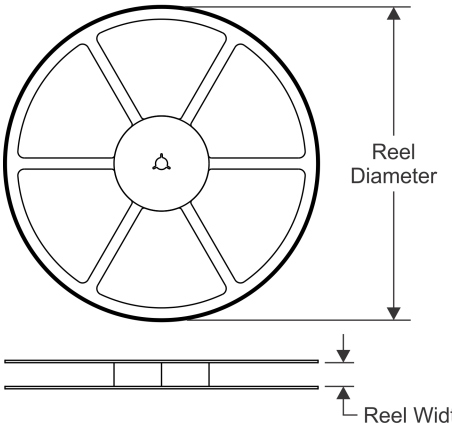
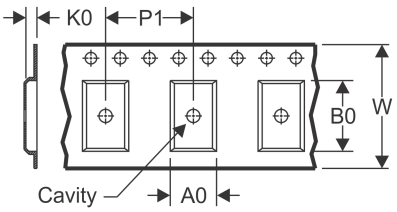
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

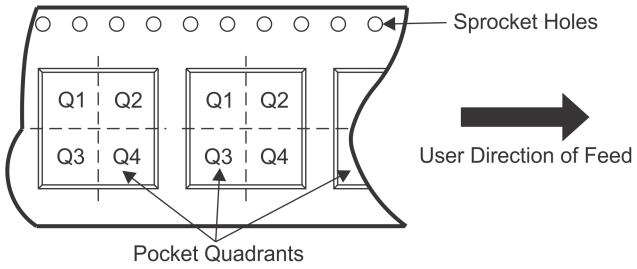


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

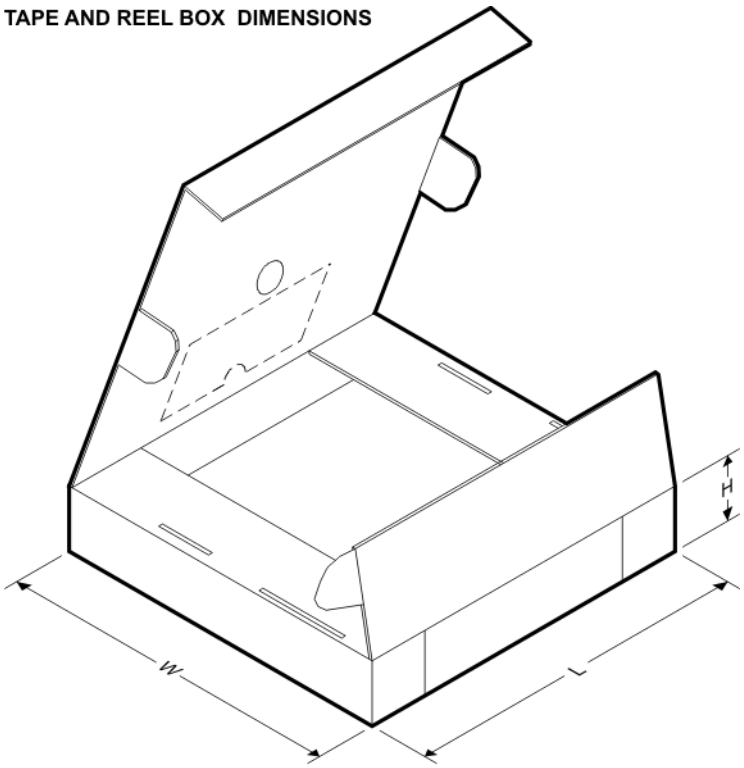
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD3S713QRVCRQ1	WQFN	RVC	20	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



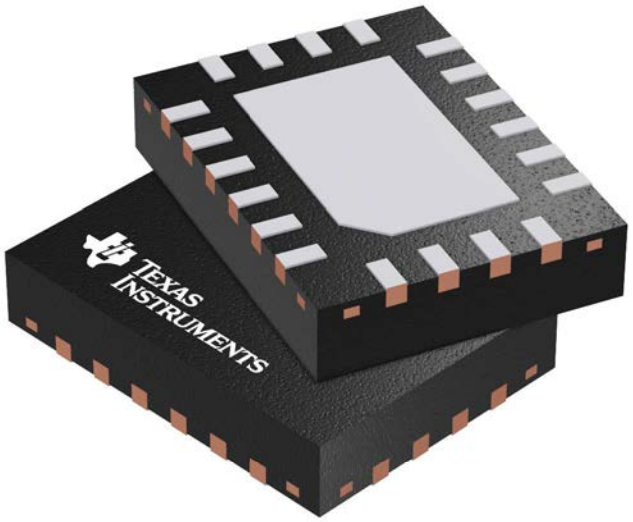
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD3S713QRVCRQ1	WQFN	RVC	20	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

RVC 20 WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



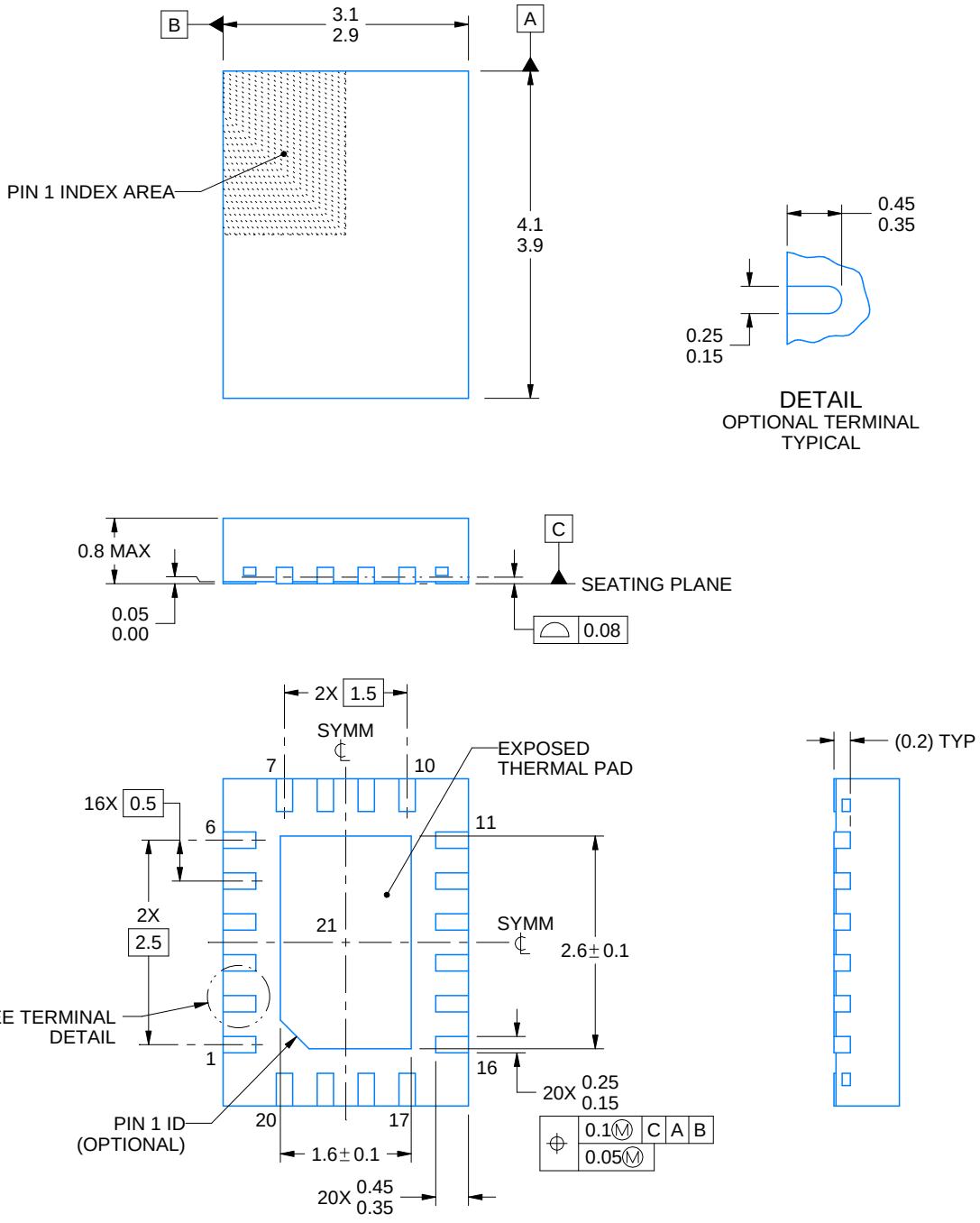
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RVC0020A

PACKAGE OUTLINE

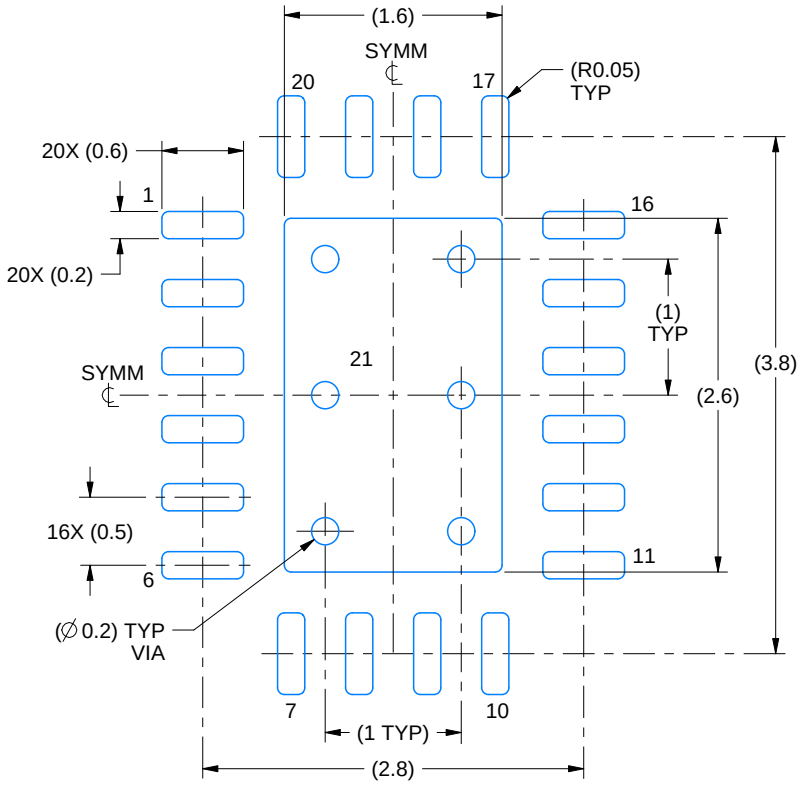
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

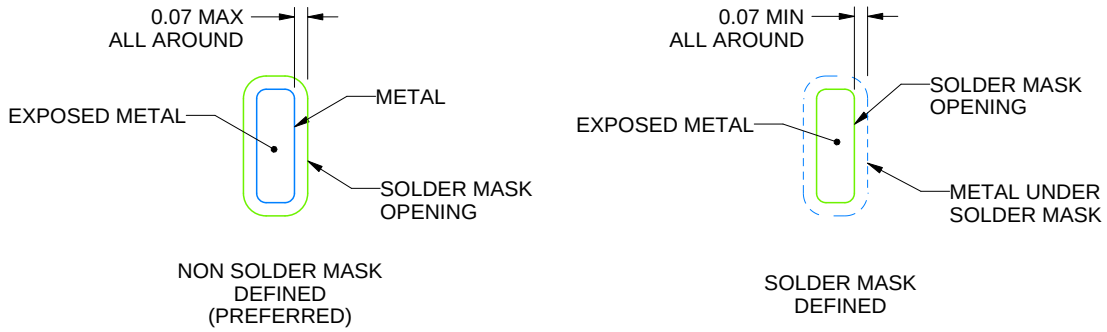


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

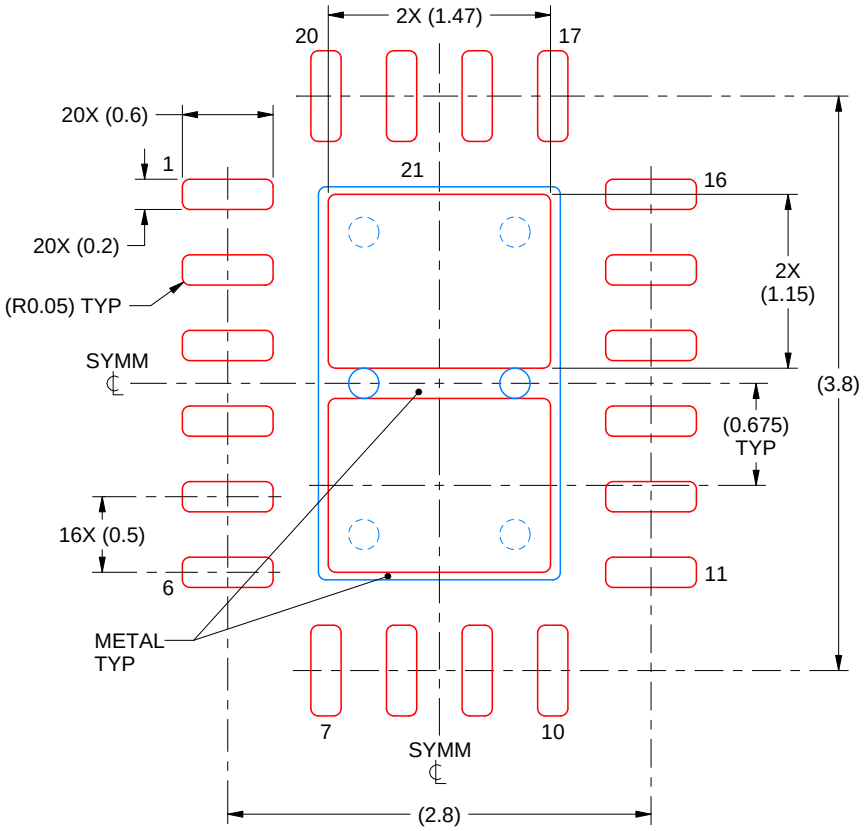


SOLDER MASK DETAILS

4219150/B 03/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD X
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219150/B 03/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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