OriginGPS
mini+mighty

HORNET ORG1411

GPS MODULE WITH INTEGRATED ANTENNA

Datasheet

OriginGPS.com

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FIGURE INDEX

1. SCOPE

This document describes the features and specifications of Nano Hornet ORG1411 GPS antenna module.

2. DISCLAIMER

All trademarks are properties of their respective owners.
Performance characteristics listed in this document do not constitute a warranty or guarantee of product performance. OriginGPS assumes no liability or responsibility for any claims or damages arising out of the use of this document, or from the use of integrated circuits based on this document.
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OriginGPS reserves the right to make changes in its products, specifications and other information at any time without notice.
OriginGPS reserves the right to conduct, from time to time, and at its sole discretion, firmware upgrades. As long as those FW improvements have no material change on end customers, PCN may not be issued.
OriginGPS navigation products are not recommended to use in life saving or life sustaining applications.

3. SAFETY INFORMATION

Improper handling and use can cause permanent damage to the product.

4. ESD SENSITIVITY

This product is ESD sensitive device and must be handled with care.

5. CONTACT INFORMATION

Support - support@origingps.com or Online Form
Marketing and sales - marketing@origingps.com
Web – www.origingps.com

6. RELATED DOCUMENTATION

№	DOCUMENT NAME
1	Nano Hornet – ORG1411 Evaluation Kit Datasheet
2	Spider and Hornet - NMEA Protocol Reference Manual
3	Spider and Hornet - One Socket Protocol Reference Manual
4	Spider and Hornet - Low Power Modes Application Note
5	SiRFLive FAQ

TABLE 1 – RELATED DOCUMENTATION

7. REVISION HISTORY

REVISION	DATE	CHANGE DESCRIPTION
1.0	May 30, 2014	First release
2.0	October 30, 2014	PM04 ordering option (V_{CC} = 2V to 5.5V variant) release
2.1	November 30, 2014	TABLE 3 updated to meet PM04 ordering option
3.0	May 31, 2016	Power Modes update – APM, MPM. Operating Temp. update
3.1	July 4, 2016	Default Interface update-UART
3.2	October 18, 2016	Figure14 – Typical PCB stack-up update
3.3	November 22, 2016	Table 11 - Wakeup states update.
3.4	May 15, 2017	Typical application circuit update, Related Documentation update, ABP update, Mechanical Specifications - Tolerance update
3.5	July 3, 2017	Section 22.1 – default interface update Section 17.4.3 – I2C update Table 11 – reset state update
3.6	October 11, 2017	Tables 8,9,10 – footnotes updates
3.7	November 9, 2017	V_{OH} update in table 4 for pm04
3.8	Mar. 12, 18	Murata filter in typical application circuit
3.9 /4.0	May 22, 18 & 6/June 18	Update typical application circuit schematics. Add I2C appendix
4.1	Dec 2018	Update PCB layout

TABLE 2 – REVISION HISTORY

8. GLOSSARY

A-GPS **A**ssisted **GPS**
ABP™ **A**lmanac **B**ased **P**osition
AC **A**lternating **C**urrent
ADC **A**nalog to **D**igital **C**onverter
AGC **A**utomatic **G**ain **C**ontrol
APM™ **A**daptive **P**ower **M**anagement
ATP™ **A**daptive **T**rickle **P**ower
BBRAM **B**attery **B**acked-up **RAM**
BE **B**roadcast **E**phemeris
BPF **B**and **P**ass **F**ilter
C/N$_0$ **C**arrier to **N**oise density ratio [dB-Hz]
CDM **C**harged **D**evice **M**odel
CE European Community conformity mark
CEP **C**ircular **E**rror **P**robability
CGEE™ **C**lient **G**enerated **E**xtended **E**phemeris
CMOS **C**omplementary **M**etal-**O**xide **S**emiconductor
CPU **C**entral **P**rocessing **U**nit
CTS **C**lear-**T**o-**S**end
CW **C**ontinuous **W**ave
DC **D**irect **C**urrent
DOP **D**ilution **O**f **P**recision

DR **D**ead **R**eckoning
DSP **D**igital **S**ignal **P**rocessor
ECEF **E**arth **C**entred **E**arth **F**ixed
ECHA **E**uropean **Ch**emical **A**gency
EE **E**xtended **E**phemeris
EGNOS **E**uropean **G**eostationary **N**avigation **O**verlay **S**ervice
EIA **E**lectronic **I**ndustries **A**lliance
EMC **E**lectro-**M**agnetic **C**ompatibility
EMI **E**lectro-**M**agnetic **I**nterference
ENIG **E**lectroless **N**ickel **I**mmersion **G**old
ESD **E**lectro-**S**tatic **D**ischarge
ESR **E**quivalent **S**eries **R**esistance
EU **E**uropean **U**nion
EVB **E**valuation **B**oard
EVK **E**valuation **K**it
FCC **F**ederal **C**ommunications **C**ommission
FSM **F**inite **S**tate **M**achine
GAGAN **G**PS **A**ided **G**eo-**A**ugmented **N**avigation
GNSS **G**lobal **N**avigation **S**atellite **S**ystem
GPIO **G**eneral **P**urpose **I**nput or **O**utput
GPS **G**lobal **P**ositioning **S**ystem
HBM **H**uman **B**ody **M**odel
HDOP **H**orizontal **D**ilution **O**f **P**recision
I^2C **I**nter-**I**ntegrated **C**ircuit
I/O **I**nput or **O**utput
IC **I**ntegrated **C**ircuit
ICD **I**nterface **C**ontrol **D**ocument
IF **I**ntermediate **F**requency
ISO **I**nternational **O**rganization for **S**tandardization
JEDEC **J**oint **E**lectron **D**evice **E**ngineering **C**ouncil
KA **K**eep **A**live
KF **K**alman **F**ilter
LDO **L**ow **D**ropo**o**ut regulator
LGA **L**and **G**rid **A**rray
LNA **L**ow **N**oise **A**mplifier7
LP **L**ow **P**ower
LS **L**east **S**quares
LSB **L**east **S**ignificant **B**it
MID **M**essage **Id**entifier
MM **M**achine **M**odel
MPM™ **M**icro **P**ower **M**ode
MSAS **M**ulti-functional **S**atellite **A**ugmentation **S**ystem
MSB **M**ost **S**ignificant **B**it
MSL **M**oisture **S**ensitivity **L**evel
NFZ™ **N**oise-**F**ree **Z**ones **S**ystem
NMEA **N**ational **M**arine **E**lectronics **A**ssociation
NVM **N**on-**V**olatile **M**emory
OSP® **O**ne **S**ocket **P**rotocol
PCB **P**rinted **C**ircuit **B**oard
PLL **P**hase **L**ock **L**oop
PMU **P**ower **M**anagement **U**nit

POR Power-**O**n **R**eset
PPS Pulse **P**er **S**econd
PRN Pseudo-**R**andom **N**oise
PSRR Power **S**upply **R**ejection **R**atio
PTF™ Push-**T**o-**F**ix
QZSS **Q**uasi-**Z**enith **S**atellite **S**ystem
RAM **R**andom **A**ccess **M**emory
REACH **R**egistration, **E**valuation, **A**uthorisation and Restriction of **Ch**emical substances
RF **R**adio **F**requency
RHCP **R**ight-**H**and **C**ircular **P**olarized
RMS **R**oot **M**ean **S**quare
RoHS **R**estriction of **H**azardous **S**ubstances directive
ROM **R**ead-**O**nly **M**emory
RTC **R**eal-**T**ime **C**lock
RTS **R**eady-**T**o-**S**end
SAW **S**urface **A**coustic **W**ave
SBAS **S**atellite-**B**ased **A**ugmentation **S**ystems
SGEE™ **S**erver **G**enerated **E**xtended **E**phemeris
SID **S**ub-**Id**entifier
SIP **S**ystem **I**n **P**ackage
SMD **S**urface **M**ounted **D**evice
SMPS **S**witched **M**ode **P**ower **S**upply
SMT **S**urface-**M**ount **T**echnology
SOC **S**ystem **O**n **C**hip
SPI **S**erial **P**eripheral **I**nterface
SSB® **S**iRF **S**tandard **B**inary
SV **S**atellite **V**ehicle
TCXO **T**emperature-**C**ompensated Crystal **O**scillator
TTFF **T**ime **T**o **F**irst **F**ix
TTL **T**ransistor-**T**ransistor **L**ogic
UART **U**niversal **A**synchronous **R**eceiver/**T**ransmitter
VCCI **V**oluntary **C**ontrol **C**ouncil for **I**nterference by information technology equipment
VEP **V**ertical **E**rror **P**robability
VGA **V**ariable-**G**ain **A**mplifier
WAAS **W**ide **A**rea **A**ugmentation **S**ystem

9. ABOUT HORNET FAMILY

OriginGPS GNSS receiver modules have been designed to address markets where size, weight, stand-alone operation, highest level of integration, power consumption and design flexibility - all are very important.

OriginGPS' Hornet family breaks size barrier, offering the industry's smallest fully-integrated, highly-sensitive GPS and GNSS modules with integrated antennas or on-board RF connectors.

Hornet family features OriginGPS' proprietary NFZ™ technology for high sensitivity and noise immunity even under marginal signal condition, commonly found in urban canyons, under dense foliage or when the receiver's position in space rapidly changes.

Hornet family enables the shortest TTM (Time-To-Market) with minimal design risks.

Just connect power supply on a single layer PCB.

10. ABOUT NANO HORNET MODULE

Nano Hornet is a complete SiP featuring miniature LGA SMT footprint designed to commit unique integration features for high volume cost sensitive applications, sharing same footprint, electrical interface and software with OriginGPS' Micro Hornet ORG1410 module in ultimate ultra-low profile of 3.8mm.

Designed to support space constrained applications such as smart watches, action cameras and wearable devices, Nano Hornet ORG1411 module is an ultra-compact, ultra-low profile and ultra-low weight multi-channel GPS with SBAS, QZSS and other regional overlay systems receiver that continuously tracks all satellites in view, providing real-time positioning data in industry's standard NMEA format.

Nano Hornet ORG1411 module offers superior sensitivity and outstanding performance, achieving rapid TTFF in less than one second, accuracy of approximately two meters, and tracking sensitivity of -163dBm.

Sized only 10mm x 10mm Nano Hornet ORG1411 module is industry's small sized, record breaking solution.

Nano Hornet module integrates OriginGPS proprietary low profile GPS antenna, dual-stage LNA, RF LDO, SAW filter, TCXO, RTC crystal and RF shield with market-leading SiRFstarIV™ GPS SoC.

Nano Hornet ORG1411 module is introducing industry's lowest energy per fix ratio, unparalleled accuracy and extremely fast fixes even under challenging signal conditions, such as in built-up urban areas, dense foliage or even indoor.

Integrated GPS SoC incorporating high-performance microprocessor and sophisticated firmware keeps positioning payload off the host, allowing integration in embedded solutions with low computing resources.

Innovative architecture can detect changes in context, temperature, and satellite signals to achieve a state of near continuous availability by maintaining and opportunistically updating its internal fine time, frequency, and satellite ephemeris data while consuming mere microwatts of battery power.

11. ABOUT ORIGINGPS

OriginGPS is a world leading designer, manufacturer and supplier of miniature positioning modules, antenna modules and antenna solutions.

OriginGPS modules introduce unparalleled sensitivity and noise immunity by incorporating Noise Free Zone system (NFZ™) proprietary technology for faster position fix and navigation stability even under challenging satellite signal conditions.

Founded in 2006, OriginGPS is specializing in development of unique technologies that miniaturize RF modules, thereby addressing the market need for smaller wireless solutions.

12. DESCRIPTION

12.1. FEATURES

- Autonomous operation
- Active antenna on-board

- OriginGPS Noise Free Zone System (NFZ™) technology
- Fully integrating:
  Low profile antenna element, Dual-stage LNA, SAW filter, TCXO, RTC crystal, GPS SoC, PMU, RF shield
- GPS L1 1575.42 frequency, C/A code
- SBAS (WAAS, EGNOS, MSAS) and QZSS support
- 48 channels
- Ultra-high Sensitivity down to -163dBm enabling Indoor Tracking
- TTFF of < 1s in 50% of trials under Hot Start conditions
- Low Power Consumption of ≤ 11mW in ATP™ mode
- High Accuracy of < 2.5m in 50% of trials
- High update rate of 5Hz, 1Hz by default
- Autonomous A-GPS by Client Generated Extended Ephemeris (CGEE™) for non-networked devices
- Predictive A-GPS by Server Generated Extended Ephemeris (SGEE™) for connected devices
- Ephemeris Push™ for storing and loading broadcast ephemeris
- Host controlled power saving mode
- Self-managed low power modes - ATP™, PTF™ and APM™
- Almanac Based Positioning (ABP™)
- Multipath and cross-correlation mitigation
- Active Jammer Detector and Remover
- Fast Time Synchronization for rapid single satellite time solution
- ARM7® microprocessor system
- Selectable UART, SPI or I^2C host interface
- NMEA protocol by default, switchable into One Socket Protocol (OSP®)
- Programmable baud rate and messages rate
- PPS output less than 30ns synchronized to GPS epoch
- Single voltage supply of 1.8V or 2V to 5.5V
- Ultra-small LGA footprint of 10mm x 10mm
- Ultra-low height of 3.8mm
- Ultra-low weight of 1.4g
- Surface Mount Device (SMD)
- Optimized for automatic assembly and reflow processes
- Operating from -40°C to +85°C
- FCC, CE, VCCI certified
- RoHS II/REACH compliant

12.2. ARCHITECTURE

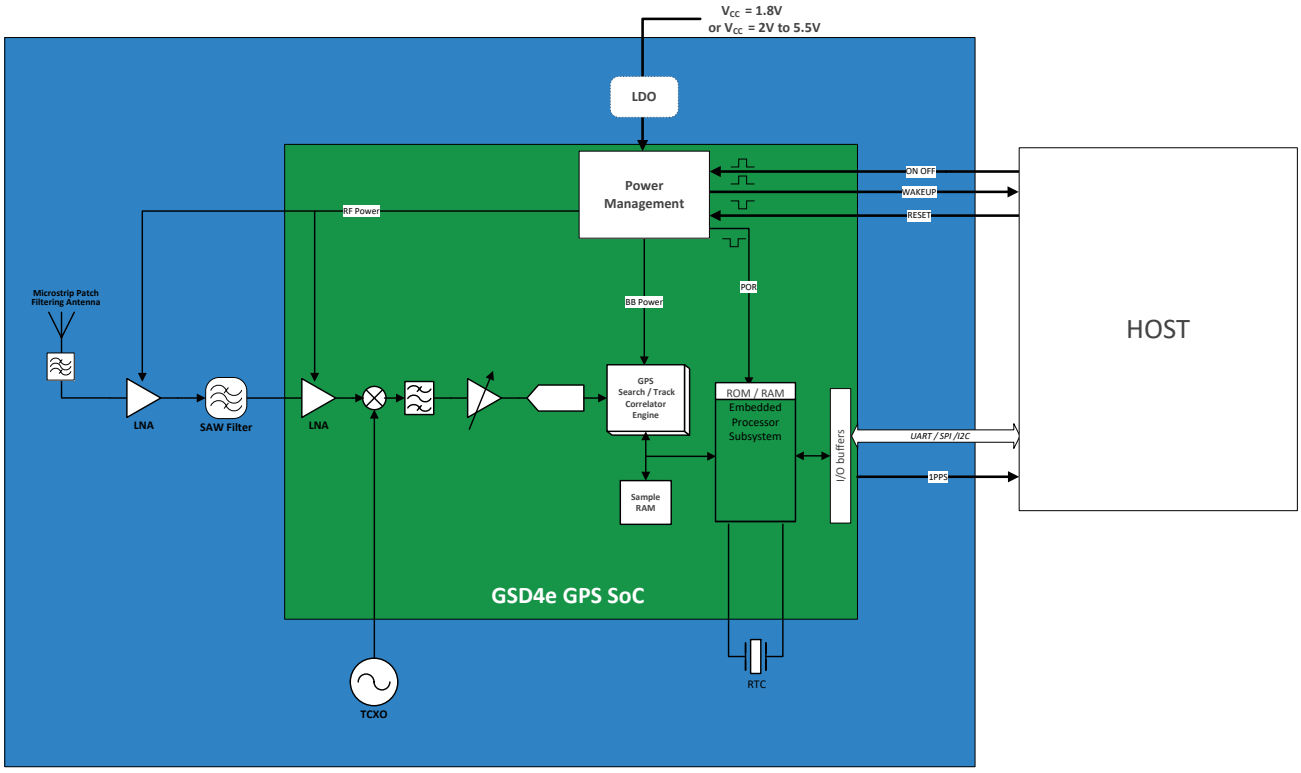

FIGURE 1 – ORG1411 ARCHITECTURE

Antenna

OriginGPS proprietary Microstrip Patch Antenna collects GPS signals from the medium.
Low profile antenna is built from hi-K ceramic element mounted on top of RF shield, providing stable resonance.

SAW Filter

Band-Pass SAW filter eliminates out-of-band signals that may interfere to GPS reception.

SAW filter is optimized for low Insertion Loss in GPS band and low Return Loss outside it.

LNA

Dual-stage cascaded LNAs amplify GPS signals to meet RF down converter input threshold.
Noise Figure optimized design was implemented to provide maximum sensitivity.

TCXO

Highly stable 16.369MHz oscillator controls down conversion process in RF block of the GPS SoC.
Characteristics of this component are important factors for higher sensitivity, shorter TTFF and better navigation stability.

RTC crystal

Tuning fork 32.768KHz quartz crystal with very tight specifications is necessary for maintaining Hot Start and Warm Start capabilities of the module.

LDO regulator

RF LDO provides regulated voltage supply over wide input voltage range, with low quiescent current and high PSRR.

RF Shield

RF enclosure avoids external interference from compromising sensitive circuitry inside the module.
RF shield also blocks module's internal high frequency emissions from being radiated.

SiRFstarIV™ GSD4e GPS SoC

SiRFstarIV™ GSD4e is full SoC built on a low-power RF CMOS single-die, incorporating GPS RF, baseband, integrated navigation solution software and ARM® processor.

FIGURE 2 – SiRFstarIV™ GSD4e GPS SoC BLOCK DIAGRAM

SiRFstarIV™ GSD4e SoC contains the following units:

- GPS radio subsystem containing LNA, harmonic-reject double balanced mixer, fractional-N synthesizer, integrated self-calibrating filters, IF VGA with AGC, high-sample rate ADCs with adaptive dynamic range.
- Measurement subsystem including DSP core for GPS signals acquisition and tracking, interference scanner and detector, wideband and narrowband interference removers, multipath and cross-correlation detectors, dedicated DSP code ROM and DSP cache RAM.
  Measurement subsystem interfaces GPS radio subsystem.
- Navigation subsystem comprising ARM7® microprocessor system for position, velocity and time solution, program ROM, data RAM, cache and patch RAM, host interface UART, SPI and I^2C drivers.
  Navigation subsystem interfaces measurement subsystem.
- Auxiliary subsystem containing RTC block and health monitor, temperature sensor for reference clock compensation, battery-backed SRAM for satellite data storage, voltage supervisor with POR, PLL controller, GPIO controller, 48-bit RTC timer and alarms, CPU watchdog monitor.
  Auxiliary subsystem interfaces navigation subsystem, PLL and PMU subsystems.
- PMU subsystem containing voltage regulators for RF and baseband domains.

13. ELECTRICAL SPECIFICATIONS

13.1. ABSOLUTE MAXIMUM RATINGS

Stresses exceeding Absolute Maximum Ratings may damage the device.

PARAMETER			SYMBOL	MIN	MAX	UNIT
Power Supply Voltage			V_{CC}	-0.30	+2.20	V
Power Supply Current[1]			I_{CC}		100	mA
I/O Voltage			V_{IO}	-0.30	+3.65	V
I/O Source/Sink Current			I_{IO}	-4	+4	mA
ESD Rating	I/O pads	HBM[4] method	$V_{IO(ESD)}$	-2000	+2000	V
		CDM[5] method		-400	+400	V
	Power pads	HBM[4] method	$V_{CC(ESD)}$	-2000	+2000	V
		CDM[5] method		-500	+500	V
	RF[2]	HBM[4] method	$V_{RF(ESD)}$	-2000	+2000	V
		MM[6] method		-100	+100	V
RF Power[3]	f_{IN} = 1560MHz÷1590MHz		P_{RF}		+10	dBm
	f_{IN} <1560MHz, >1590MHz				+30	dBm
Power Dissipation			P_D		220	mW
Operating Temperature			T_{AMB}	-45	+85	°C
Storage Temperature			T_{ST}	-55	+150	°C
Lead Temperature[7]			T_{LEAD}		+260	°C

TABLE 3 – ABSOLUTE MAXIMUM RATINGS

Notes:

1. Inrush current of up to 100mA for about 20µs duration.
2. Voltage applied on antenna element.
3. Power delivered to antenna element.
4. Human Body Model (HBM) contact discharge per EIA/JEDEC JESD22-A114D.
5. Charged Device Model (CDM) contact discharge per EIA/JEDEC JESD22-C101.
6. Machine Model (MM) contact discharge per EIA/JEDEC JESD22-A115C.
7. Lead temperature at 1mm from case for 10s duration.

13.2. RECOMMENDED OPERATING CONDITIONS

Exposure to stresses above Recommended Operating Conditions may affect device reliability.

PARAMETER	SYMBOL	MODE / PAD	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power supply voltage	V_{CC}	V_{CC}	1.8V ordering option[1]	+1.71	+1.80	+1.89	V
		V_{CC}	2V to 5.5V ordering option[2]	+2.0	+3.3	5.5	V
Power Supply Current[3]	I_{CC}	Acquisition		40	43	47	mA
		Tracking		6		40	mA
		ATP™[4]			6		mA
		CPU only[5]			14	17	mA
		Standby[5]			90	100	µA
		PTF™[6]			400		µA
		MPM™[7]		125			µA
		Hibernate	1.8V ordering option[1]	10	15	18	µA
			2V to 5.5V ordering option[2]	16	18	22	µA
Input Voltage Low State	V_{IL}	GPIO		-0.40		+0.45	V
Input Voltage High State	V_{IH}			0.70·V_{CC}		+3.60	V
Output Voltage Low State	V_{OL}		I_{OL} = 2mA			+0.40	V
Output Voltage High State	V_{OH}		1.8V ordering option[1] I_{OH} = -2mA	0.75·V_{CC}			V
Output Voltage High State[2]	V_{OH}		2V to 5.5V ordering option[2] I_{OH} = -2mA		1.8		V
Input Capacitance	C_{IN}				5		pF
Internal Pull-up Resistor	R_{PU}			50	86	157	kΩ
Internal Pull-down Resistor	R_{PD}			51	91	180	kΩ
Input Leakage Current	$I_{IN(leak)}$		V_{IN} = 1.8V or 0V	-10		+10	µA
Output Leakage Current	$I_{OUT(leak)}$		V_{OUT} = 1.8V or 0V	-10		+10	µA
Input Power Range	P_{IN}	Antenna		-165		-110	dBm
Input Frequency Range	f_{IN}				1575.42		MHz
Operating Temperature[8]	T_{AMB}			-40	+25	+85	°C
Storage Temperature	T_{ST}			-55	+25	+125	°C
Relative Humidity[9]	RH		T_{AMB}	5		95	%

TABLE 4 – RECOMMENDED OPERATING CONDITIONS

Notes:

1. Applicable to part number ORG1411-PM01.
2. Applicable to part number ORG1411-PM04.
3. Typical I_{CC} values are under signal conditions of -130dBm and ambient temperature of +25°C.
4. ATP™ mode 200:1 (200ms on-time, 1s period).

5. Transitional states of ATP™ power saving mode.
6. PTF™ mode 30:30 (30s max. on-time – 18s typical, 30m period).
7. Average current during MPM™ with valid satellite ephemeris data.
8. Longer TTFF is expected while operating below -30°C to -40°C.
9. Relative Humidity is within Operating Temperature range.

14. PERFORMANCE

14.1. ACQUISITION TIME

TTFF (Time To First Fix) – is the period of time from module's power-up till valid position estimation.

14.1.1. HOT START

Hot Start results either from a software reset after a period of continuous navigation or a return from a short idle period that was preceded by a period of continuous navigation.

During Hot Start all critical data (position, velocity, time, and satellite ephemeris) is valid to the specified accuracy and available in RAM.

14.1.2. SIGNAL REACQUISITION

Reacquisition follows temporary blocking of GPS signals.

Typical reacquisition scenario includes driving through tunnel.

14.1.3. AIDED START

Aided Start is a method of effectively reducing TTFF by providing valid satellite ephemeris data.

Aiding can be implemented using Ephemeris Push™, CGEE™ or SGEE™.

14.1.4. WARM START

Warm Start typically results from user-supplied position and time initialization data or continuous RTC operation with an accurate last known position available in RAM.

In this state position and time data are present and valid, but satellite ephemeris data validity has expired.

14.1.5. COLD START

Cold Start occurs when satellite ephemeris data, position and time data are unknown.

Typical Cold Start scenario includes first power application.

OPERATION[1]	VALUE	UNIT
Hot Start	< 1	s
Signal Reacquisition[2]	< 1	s
Aided Start	< 10	s
Warm Start	< 32	s
Cold Start	< 35	s

TABLE 5 – ACQUISITION TIME

Notes:

1. EVK is 24-hrs. static under signal conditions of -130dBm and ambient temperature of +25°C.
2. Outage duration ≤ 30s.

14.2. SENSITIVITY

14.2.1. TRACKING

Tracking is an ability of receiver to maintain valid satellite ephemeris data.

During tracking receiver may stop output valid position solutions.

Tracking sensitivity defined as minimum GPS signal power required for tracking.

14.2.2. REACQUISITION

Reacquisition follows temporary blocking of GPS signals.

Reacquisition sensitivity defined as minimum GPS signal power required for reacquisition.

14.2.3. NAVIGATION

During navigation receiver consequently outputs valid position solutions.

Navigation sensitivity defined as minimum GPS signal power required for reliable navigation.

14.2.4. HOT START

Hot Start sensitivity defined as minimum GPS signal power required for valid position solution under Hot Start conditions.

14.2.5. AIDED START

Aided Start sensitivity defined as minimum GPS signal power required for valid position solution following aiding process.

14.2.6. COLD START

Cold Start sensitivity defined as minimum GPS signal power required for valid position solution under Cold Start conditions, sometimes referred as ephemeris decode threshold.

OPERATION[1]	VALUE	UNIT
Tracking	-163	dBm
Reacquisition[2]	-162	dBm
Navigation	-161	dBm
Hot Start[3]	-160	dBm
Aided Start[4]	-156	dBm
Cold Start	-148	dBm

TABLE 6 – SENSITIVITY

14.3. RECEIVED SIGNAL STRENGTH

PARAMETER[5]	VALUE	UNIT
C/N_0	43	dB-Hz

TABLE 7 – RECEIVED SIGNAL STRENGTH

Notes:

1. GPS signal power level approaching antenna, EVK is static and ambient temperature is +25°C.
2. Outage duration ≤ 30s.
3. Hibernate state duration ≤ 5m.
4. Aiding using Broadcast Ephemeris (Ephemeris Push™) or Extended Ephemeris (CGEE™ or SGEE™).
5. Average C/N_0 reported for 4 SVs, EVK is 24-hrs. static, outdoor, ambient temperature is +25°C.

14.4. POWER CONSUMPTION

OPERATION[1]		VALUE	UNIT
Acquisition		77	mW
Tracking		67	mW
Low Power Tracking	ATP™ 200:1	11	mW
	PTF™ 30s:30m	0.75	mW
	5m Hibernate:10s tracking	2.5	mW
Hibernate		27	µW

TABLE 8 – POWER CONSUMPTION

14.5. ACCURACY

PARAMETER		FORMAT	MODE	VALUE	UNIT
Position[1]	Horizontal	CEP (50%)	GPS + SBAS	< 2.0	m
			GPS	< 2.5	m
		2dRMS (95%)	GPS + SBAS	< 4.0	m
			GPS	< 5.0	m
	Vertical	VEP (50%)	GPS + SBAS	< 3.5	m
			GPS	< 4.0	m
		2dRMS (95%)	GPS + SBAS	< 6.5	m
			GPS	< 7.5	m
Velocity[2]	over ground	50% of samples		< 0.01	m/s
Heading	to north	50% of samples		< 0.01	°
Time[1]		RMS jitter	1 PPS	≤ 30	ns

TABLE 9 – ACCURACY

14.6. DYNAMIC CONSTRAINS

PARAMETER	Metric	Imperial
Velocity and Altitude[3]	515m/s and 18,288m	1,000knots and 60,000ft
Velocity	600m/s	1,166knots
Altitude	-500m to 24,000m	-1,640ft to 78,734ft
Acceleration	4g	
Jerk	5m/s^3	

TABLE 10 – DYNAMIC CONSTRAINS

Notes:

1. V_{CC} = 1.8V, module is static under signal conditions of -130dBm, ambient temperature is +25°C.
2. Speed over ground ≤ 30m/s.
3. Standard dynamic constrains according to regulatory limitations.

15. POWER MANAGEMENT

15.1. POWER STATES

15.1.1. FULL POWER ACQUISITION

ORG1411 module stays in Full Power Acquisition state until a reliable position solution is made.

15.1.2. FULL POWER TRACKING

Full Power Tracking state is entered after a reliable position solution is achieved.

During this state the processing is less intense compared to Full Power Acquisition, therefore power consumption is lower. Full Power Tracking state with navigation update rate at 5Hz consumes more power compared to default 1Hz navigation.

15.1.3. CPU ONLY

CPU Only is the transitional state of ATP™ power saving mode when the RF and DSP sections are partially powered off. This state is entered when the satellites measurements have been acquired, but navigation solution still needs to be computed.

15.1.4. STANDBY

Standby is the transitional state of ATP™ power saving mode when RF and DSP sections are completely powered off and baseband clock is stopped.

15.1.5. HIBERNATE

ORG1411 module boots into Hibernate state after power supply applied, drawing only 10µA[1].

When Hibernate state is following Full Power Tracking state current consumption is 15µA[1].

During this state RF, DSP and baseband sections are completely powered off leaving only RTC and Battery-Backed RAM running.

Module will perform Hot Start if stayed in Hibernate state less than 4 hours from last valid position solution.

15.2. BASIC POWER SAVING MODE

Basic power saving mode is elaborating host in straightforward way for controlling transfers between Full Power and Hibernate states.

Current profile of this mode has no hidden cycles of satellite data refresh.

Host may condition transfers by tracking duration, accuracy, satellites in-view or other parameters.

Notes:

1. V_{CC} = 1.8V, ambient temperature is +25°C.

15.3. SELF MANAGED POWER SAVING MODES

Nano Hornet module has several self-managed power saving modes tailored for different use cases. These modes provide several levels of power saving with degradation level of position accuracy. Initial operation in Full Power state is a prerequisite for accumulation of satellite data determining location, fine time and calibration of reference clocks.

15.3.1. ADAPTIVE TRICKLE POWER (ATP™)

ATP™ is best suited for applications that require navigation solutions at a fixed rate as well as low power consumption and an ability to track weak signals.
This power saving mode provides the most accurate position among self-managed modes.
In this mode module is intelligently cycled between Full Power state, CPU Only state consuming 14mA and Standby state consuming ≤ 100µA, therefore optimizing current profile for low power operation.
ATP™ period that equals navigation solution update can be 1 second to 10 seconds.
On-time including Full Power Tracking and CPU Only states can be 200ms to 900ms.

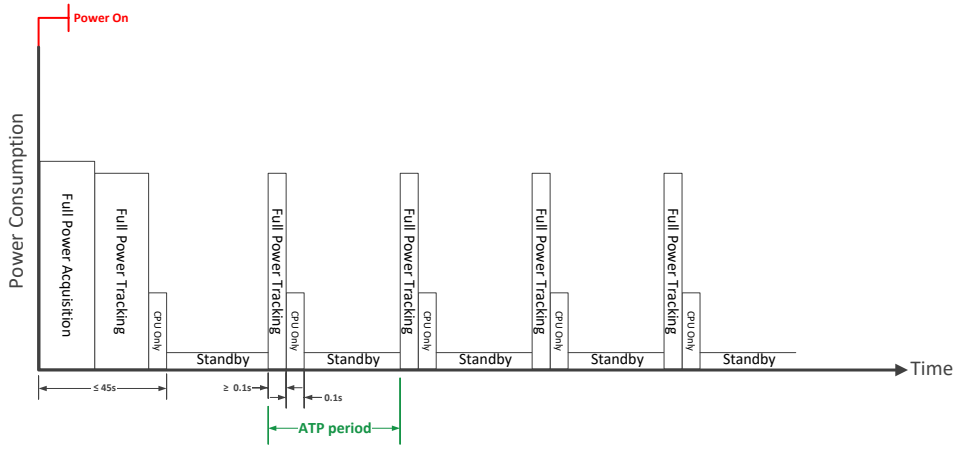

FIGURE 3 – ATP™ TIMING

15.3.2. PUSH TO FIX (PTF™)

PTF™ is best suited for applications that require infrequent navigation solutions.
In this mode ORG1411 module is mostly in Hibernate state, drawing ≤ 18µA of current, waking up for satellite data refresh in fixed periods of time.
PTF™ period can be anywhere between 10 seconds and 2 hours.
Host can initiate an instant position report by toggle the ON_OFF pad to wake up the module.
During fix trial module will stay in Full Power state until good position solution is estimated or pre-configured timeout for it has expired.

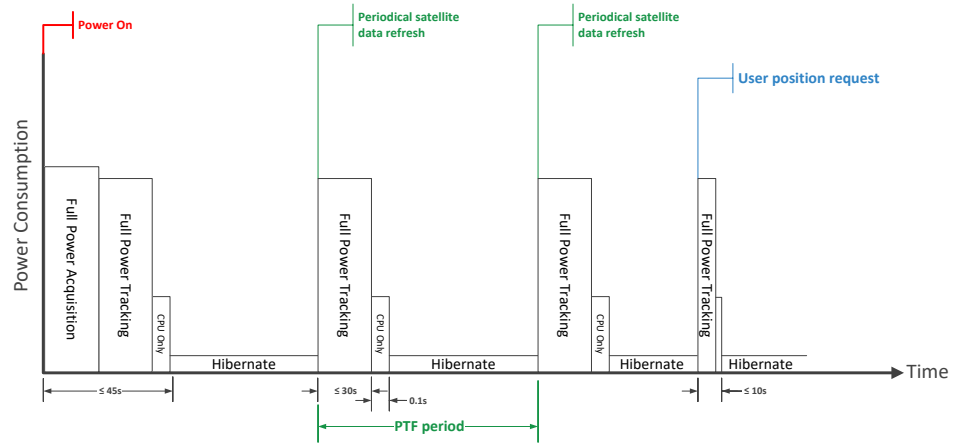

FIGURE 4 – PTF™ TIMING

15.3.3. ADVANCED POWER MANAGEMENT (APM™)

APM™ is designed for aided- GPS applications.
APM™ allows power savings while ensuring that the **Q**uality **o**f the **S**olution (QoS) in maintained when signals level drop.
In APM™ mode the module is intelligently cycled between Full Power and Hibernate states.
In addition to setting the position report interval, a QoS specification is available that sets allowable error estimates and selects priorities between position report interval and more power saving.
User may select between Duty Cycle Priority for more power saving and Time Between Fixes (TBF) priority with defined or undefined maximum horizontal error.
TBF range is from 10s to 180s between fixes, Power Duty Cycle range is between 5% to 100%.
Maximum position error is configurable between 1 to 160m.
The number of APM™ fixes is configurable up to 255 or set to continuous.

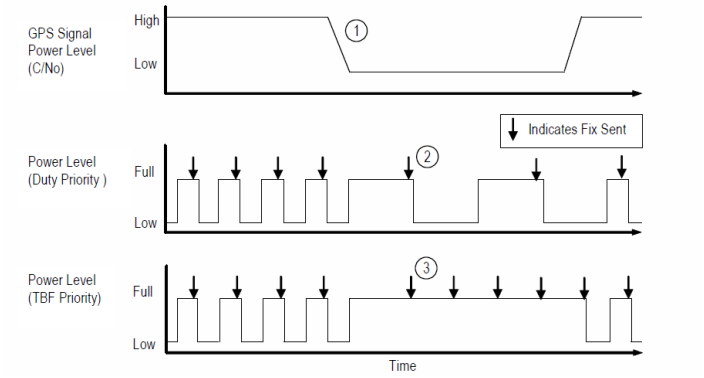

FIGURE 5 – APM™ TIMING

Notes:

1. GPS signal level drops (e.g. user walks indoor).
2. Lower signal results in longer ON time. To maintain Duty Cycle Priority, OFF time is increased.
3. Lower signal means missed fix. To maintain future TBFs module goes Full Power state until signal levels improve.

16. EXTENDED FEATURES

16.1. ALMANAC BASED POSITIONING (ABP™)

With ABP™ mode enabled, the user can get shorter Cold Start TTFF as tradeoff with position accuracy. The reported position in this case is an indication only – hundreds of meters circular error probability. It is not recommended to use ABP™ in applications which demand precise position.

When no sufficient ephemeris data is available to calculate an accurate solution, a coarse solution will be provided where the position is calculated based on one or more of the GPS satellites, having their states derived from the almanac data.

Data source for ABP™ may be either stored factory almanac, broadcasted or pushed almanac.

16.2. ACTIVE JAMMER DETECTOR AND REMOVER

Jamming Detector is embedded DSP software block that detects interference signals in GPS L1 band.

Jamming Remover is additional DPS software block that sort-out Jamming Detector output mitigating up to 8 interference signals of Continuous Wave (CW) type up to 80dB-Hz each.

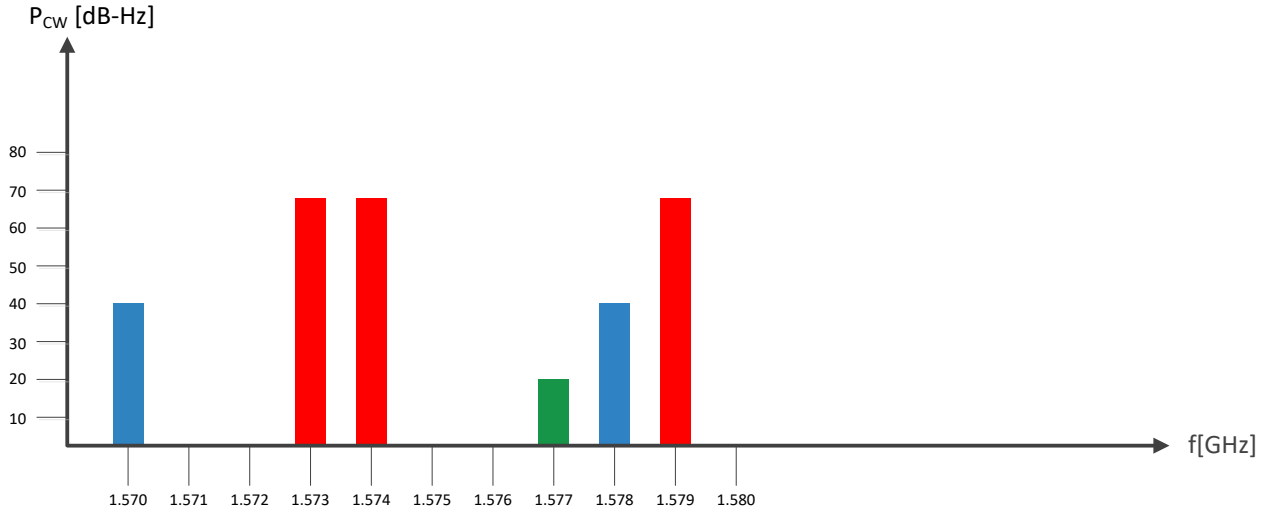

FIGURE 6 – ACTIVE JAMMER DETECTOR FREQUENCY PLOT

16.3. CLIENT GENERATED EXTENDED EPHEMERIS (CGEE™)

CGEE™ feature allows shorter TTFFs by providing predicted (synthetic) ephemeris files created within a non-networked host system from previously received satellite ephemeris data.

The prediction process requires good receipt of broadcast ephemeris data for all satellites.

EE files created this way are good for up to 3 days and then expire.

CGEE™ feature requires avoidance of power supply removal.

CGEE™ data files are stored and managed by host.

16.4. SERVER GENERATED EXTENDED EPHEMERIS (SGEE™)

SGEE™ enables shorter TTFFs by fetching **E**xtended **E**phemeris (EE) file downloaded from web server.

Host is initiating periodic network sessions of EE file downloads, storage and provision to module.

There is one-time charge for set-up, access to OriginGPS EE distribution server and end-end testing for re-distribution purposes, or there is a per-unit charge for each module within direct SGEE™ deployment.

EE files are provided with look-ahead of 1, 3, 7, 14 or 31 days.

17. INTERFACE

17.1. PAD ASSIGNMENT

PAD	NAME	FUNCTION			DIRECTION	FULL POWER[1]	HIBERNATE[2]
1	ON_OFF	Power State Control			Input	Hi-Z	Hi-Z
2	1PPS	UTC Time Mark			Output	Low	Low
3	TX	UART Transmit	SPI Data Out	I^2C Clock	Bi-directional	High	Hi-Z
4	V_{CC}	System Power			Power		
5	GND	System Ground			Power		
6	WAKEUP	Power Status			Output	High	Low
7	$\overline{CTS}$	Interface Select 1	UART Clear To Send	SPI Clock	Bi-directional	Low	Low
8	$\overline{RESET}$	Asynchronous Reset			Input		
9	$\overline{RTS}$	Interface Select 2	UART Ready To Send	SPI Chip Select	Bi-directional	High	High
10	RX	UART Receive	SPI Data In	I^2C Data	Bi-directional	High	High

TABLE 11 – PIN-OUT

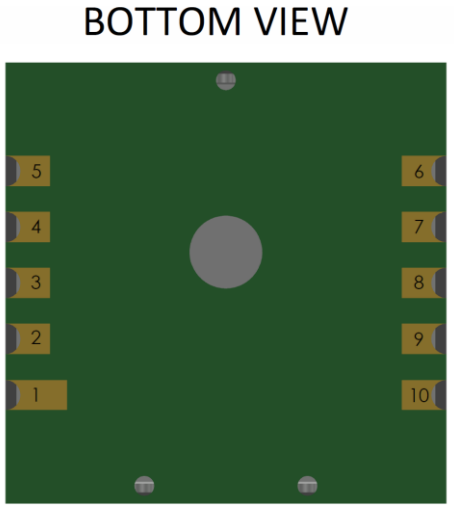

FIGURE 7 – PAD ASSIGNMENT

Notes:

1. Full Power Acquisition, Full Power Tracking and CPU Only states.
2. Hibernate and Standby states.

17.2. POWER SUPPLY

It is recommended to keep the power supply on all the time in order to maintain RTC block active and keep satellite data in RAM for fastest possible TTFF. When V_{CC} is removed settings are reset to factory default and the receiver performs Cold Start on next power up.

17.2.1. V_{CC} = 1.8V ORDERING OPTION PM01

V_{CC} is 1.8V ±5% DC and must be provided from regulated power supply.

Typical I_{CC} is 43mA during acquisition.

Inrush current can be up to 100mA for about 20µs duration, whilst V_{CC} can drop down to 1.7V.

Typical I_{CC} current in Hibernate state is 15µA, while all I/O lines externally held in Hi-Z state.

Output capacitors are critical when powering module from switch-mode power supply.

Filtering is important to manage high alternating current flows on the power input connection. An additional filtering on module power input may be needed to reduce system noise.

The high rate of module input current change requires low ESR bypass capacitors.
Additional higher ESR output capacitors can provide input stability damping.
The ESR and size of the output capacitors directly define the output ripple voltage with a given inductor size. Large low ESR output capacitors are beneficial for low noise.

Voltage ripple below 50mV_{P-P} is allowed for frequencies between 100KHz to 1MHz.

Voltage ripple below 15mV_{P-P} is allowed for frequencies above 1MHz.

Voltage ripple higher than allowed may compromise sensitivity parameter.

17.2.2. V_{CC} = 2V TO 5.5V ORDERING OPTION PM04

V_{CC} range is 2V to 5.5V DC and may be provided from unregulated power supply.

Typical I_{CC} is 43mA during acquisition.

Typical I_{CC} current in Hibernate state is 18µA, while all I/O lines externally held in Hi-Z state.

17.2.3. GROUND

Ground pad must be connected to host PCB Ground with shortest possible trace or by multiple vias.

17.3. CONTROL INTERFACE

17.3.1. ON_OFF

ON_OFF input is used to switch module between different power states:

- While in Hibernate state, ON_OFF pulse will initiate transfer into Full Power state.
- While in ATP™ mode, ON_OFF pulse will initiate transfer into Full Power state.
- While in PTF™ mode, ON_OFF pulse will initiate one PTF™ request.
- While in Full Power state, ON_OFF pulse will initiate orderly shutdown into Hibernate state.

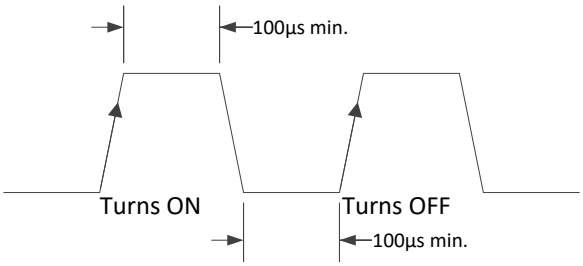

FIGURE 8 – ON_OFF TIMING

ON_OFF detector set requires a rising edge and high logic level that persists for at least 100µs.
ON_OFF detector reset requires ON_OFF asserted to low logic level for at least 100µs.

Recommended ON_OFF Low-High-Low pulse length is 100ms.

ON_OFF pulses with less than 1s intervals are not recommended.

Multiple switch bounce pulses are recommended to be filtered out.

Pull-down resistor of 10kΩ-33kΩ is recommended to avoid accidental power mode change.

ON_OFF input is tolerable up to 3.6V.

Do not drive high permanently or pull-up this input. This line must be connected to host.

17.3.2. WAKEUP

WAKEUP output from module is used to indicate power state.

A low logic level indicates that the module is in one of its low-power states - Hibernate or Standby. A high logic level indicates that the module is in Full Power state.

Connecting WAKEUP to ON_OFF enables autonomous start to Full Power state.

In addition WAKEUP output can be used to control auxiliary devices.

Wakeup output is LVCMOS 1.8V compatible.

Do not connect if not in use.

17.3.3. $\overline{\text{RESET}}$

Power-on-Reset (POR) sequence is generated internally.

In addition, external reset is available through $\overline{\text{RESET}}$ pad.

Resetting module clears the state machine of self-managed power saving modes to default.

$\overline{\text{RESET}}$ signal should be applied for at least 1µs.

$\overline{\text{RESET}}$ input is active low and has internal pull-up resistor of 86kΩ to internal 1.2V domain.

Do not drive this input high.

Do not connect if not in use.

17.3.4. 1PPS

Pulse-Per-Second (PPS) output provides a pulse signal for timing purposes.

PPS output starts when position solution has been obtained using 5 or more GPS satellites.

PPS output stops when 3D position solution is lost.

Pulse length (high state) is 200ms with rising edge is less than 30ns synchronized to GPS epoch.

The correspondent UTC time message is generated and put into output FIFO 300ms after the PPS signal. The exact time between PPS and UTC time message delivery depends on message rate, message queue and communication baud rate.

1PPS output is LVCMOS 1.8V compatible.

Do not connect if not in use.

17.4. DATA INTERFACE

ORG1411 module has 3 types of interface ports to connect to host - UART, SPI or I^2C – all multiplexed on a shared set of pads. At system reset host port interface lines are disabled, so no conflict occurs. Logic values on $\overline{\text{CTS}}$ and $\overline{\text{RTS}}$ are read by the module during startup and define host port type. External resistor of 10kΩ is recommended. Pull-up resistor is referenced to 1.8V.

PORT TYPE	$\overline{\text{CTS}}$	$\overline{\text{RTS}}$
UART	External pull-up	Do not install external pull up
SPI (default)	Do not install external pull up	Do not install external pull up
I^2C	Do not install external pull up	External pull-down

TABLE 12 – HOST INTERFACE SELECT

17.4.1. UART

UART host interface features are:

- TX used for GPS data reports. Output logic high voltage level is LVCMOS 1.8V compatible.
- RX used for receiver control. Input logic high voltage level is 1.45V, tolerable up to 3.6V.
- UART flow control using $\overline{\text{CTS}}$ and $\overline{\text{RTS}}$ lines is disabled by default.
  Can be turned on by sending OSP Message ID 178, Sub ID 2 input command.

17.4.2. SPI

SPI host interface features are:

- Slave SPI Mode 1, supports clock up to 6.8MHz.
- RX and TX have independent 2-byte idle patterns of '0xA7 0xB4'.
- TX and RX each have independent 1024 byte FIFO buffers.
- TX FIFO is disabled when empty and transmits its idle pattern until re-enabled.
- RX FIFO detects a software specified number of idle pattern repeats and then disables FIFO input until the idle pattern is broken.
- FIFO buffers can generate an interrupt at any fill level.
- SPI detects synchronization errors and can be reset by software.
- Output is LVCMOS 1.8V compatible. Inputs are tolerable up to 3.6V.

17.4.3. I^2C

I^2C host interface features are:

- I^2C Multi-Master Mode - module initiates clock and data, operating speed 400kbps.
- I^2C address '0x60' for RX and '0x62' for TX.
- Individual transmit and receive FIFO length of 64 bytes.
- I^2C host interface supports multi-master mode only. Clock rate can be switched 100KHz (default 400KHz), address can be changed (default 0x62 for TX FIFO and 0x60 for RX FIFO) by sending OSP Message ID 178, Sub ID 2 input command.
- SCL and SDA are pseudo open-drain lines, therefore require external pull-up resistors of 2.2kΩ to 1.8V, or 3.3kΩ to 3.3V.
- Data frame size is 8bit octets, MSB transmitted first, unlimited maximum bytes per transfer. Address is 7bit (MSB).

18. TYPICAL APPLICATION CIRCUIT

UART: R1 = 10K R2, R3, R4 = DO NOT ASSEMBLE SN74AUP1T97 if VCC-IO_MCU > 1.8V
SPI: R1, R2, R3, R4 = DO NOT ASSEMBLE
I2C: R2 = 10K and R3, R4 = 2.2K R1 = DO NOT ASSEMBLE

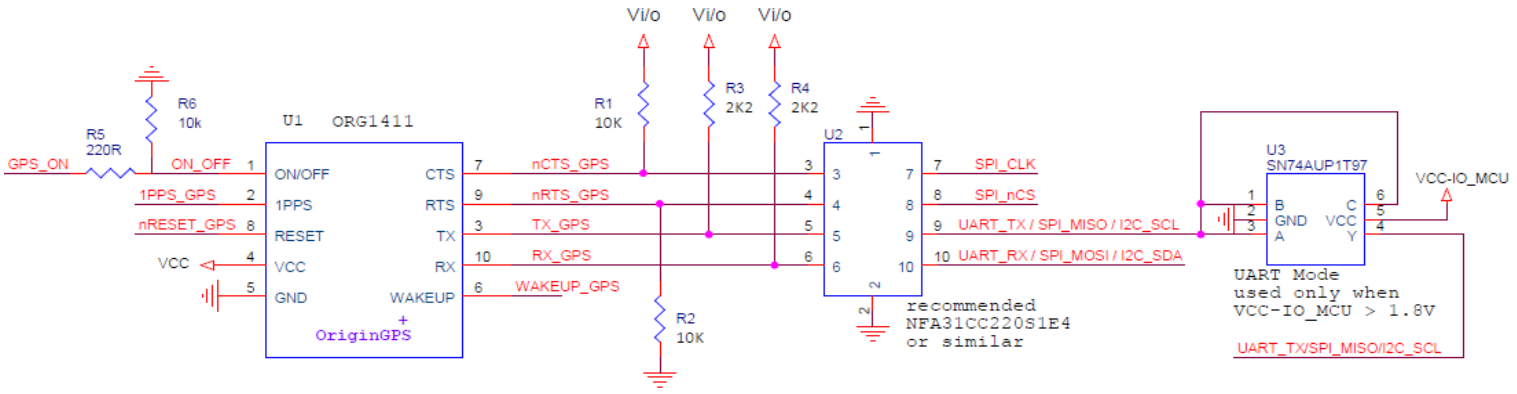

FIGURE 9 – REFERENCE SCHEMATIC DIAGRAM - PM01 ORDERING OPTION

19. RECOMMENDED PCB LAYOUT

Please review the dedicated application note at
https://origingps.com/wp-content/uploads/2018/08/Hornet-Modules-Layout-Recommendations-andIntegration-Application-Note.pdf

20. DESIGN CONSIDERATIONS

ORG1411 incorporates on-board low profile antenna element that is perfectly matched to receiver front-end, frequency trimmed to GPS band and Right-Hand Circularly Polarized (RHCP).

End device enclosure or housing must be of very low electrical permeability properties.

OriginGPS proprietary module structure is providing stable resonance of antenna in GPS band with very low dependence on host PCB size, it's conducting planes geometry and stack-up.

To prevent PCB factor on antenna resonance avoid copper pouring on module side.

To prevent module orientation from causing polarization losses in on-board antenna avoid long and narrow copper planes beneath.

ORG1411 operates with received signal levels down to -163dBm and can be affected by high absolute levels of RF signals out of GPS band, moderate levels of RF interference near GPS band and by low-levels of RF noise in GPS band.

RF interference from nearby electronic circuits or radio transmitters can contain enough energy to desensitize ORG1411. These systems may also produce levels of energy outside of GPS band, high enough to leak through RF filters and degrade the operation of the radios in ORG1411.

This issue becomes more critical in small products, where there are industrial design constraints.

In that environment, transmitters for Wi-Fi, Bluetooth, RFID, cellular and other radios may have antennas physically close to ORG1411.

To prevent degraded performance of ORG1411 OriginGPS recommends performing EMI/jamming susceptibility tests for radiated and conducted noise on prototypes and assessing risks of other factors.

Contact OriginGPS for application specific recommendations and design review services.

21. OPERATION

When power is first applied, module goes into a Hibernate state while integrated RTC starts and internal Finite State Machine (FSM) sequences though to “Ready-to-Start” state.

Host is not required to control external master $\overline{\text{RESET}}$ since module’s internal reset circuitry handles detection of power application.

While in “Ready-to-Start” state, module awaits a pulse to the ON_OFF input.

Since integrated RTC startup times are variable, host is required either to wait for a fixed interval or to monitor a short Low-High-Low pulse on WAKEUP output that indicates FSM “Ready-to-Start” state.

Another option is to repeat a pulse on the ON_OFF input every second until the module starts by either detecting a stable logic high level on WAKEUP output or neither generation of UART messages.

21.1. STARTING THE MODULE

A pulse on the ON_OFF input line when FSM is ready and in startup-ready state, Hibernate state, standby state, will command the module to start.

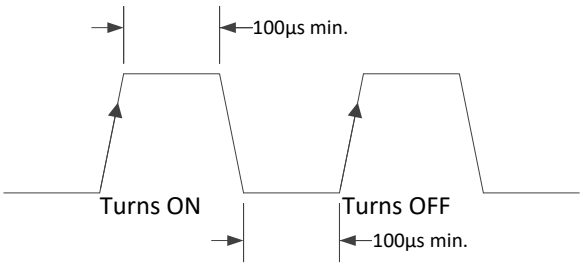

FIGURE 10 – ON_OFF TIMING

ON_OFF detector set requires a rising edge and high logic level that persists for at least 100µs.

ON_OFF detector reset requires ON_OFF asserted to low logic level for at least 100µs.

Recommended ON_OFF Low-High-Low pulse length is 100ms.

ON_OFF pulses with less than 1s intervals are not recommended.

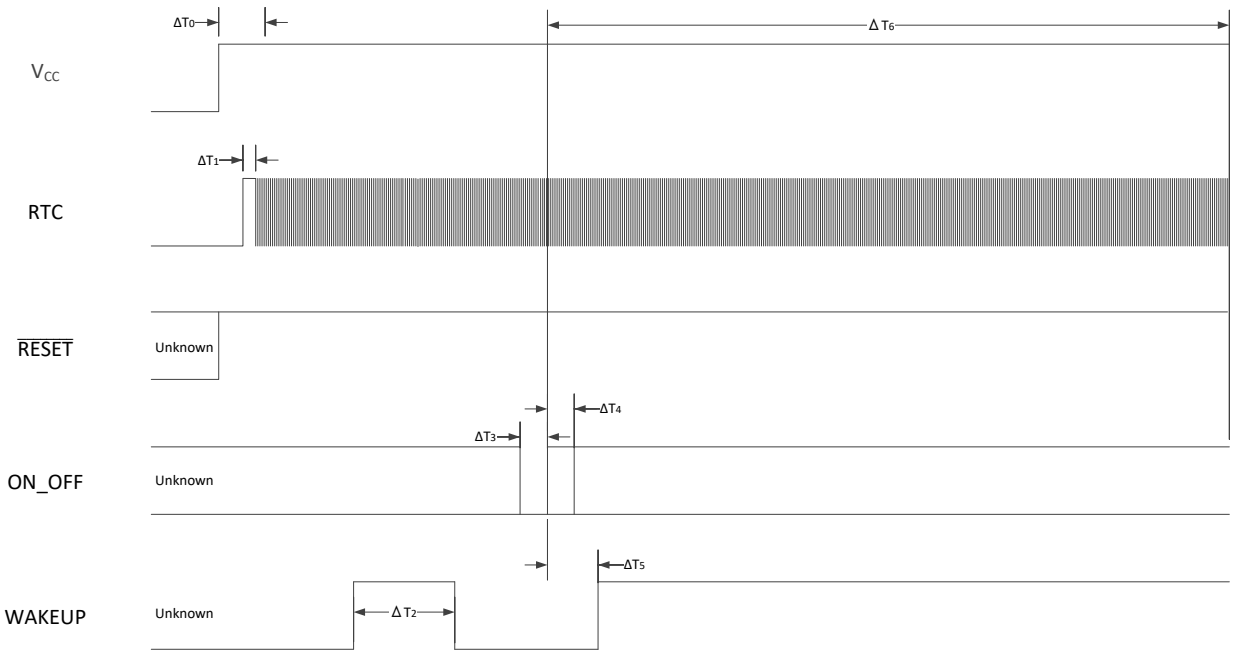

FIGURE 11– START-UP TIMING

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
f_{RTC}	RTC Frequency	+25°C	-20 ppm	32768	+20 ppm	Hz
t_{RTC}	RTC Tick	+25°C		30.5176		µs
ΔT_1	RTC Startup Time			300		ms
ΔT_0	Power Stabilization		$6 \cdot t_{RTC}+\Delta T_1$	$7 \cdot t_{RTC}+\Delta T_1$	$8 \cdot t_{RTC}+\Delta T_1$	µs
ΔT_2	WAKEUP Pulse	RTC running		10		t_{RTC}
ΔT_3	ON_OFF Low		3			t_{RTC}
ΔT_4	ON_OFF High		3			t_{RTC}
ΔT_5	ON_OFF to WAKEUP high	After ON_OFF		6		t_{RTC}
ΔT_6	ON_OFF to ARM boot	After ON_OFF		2130		t_{RTC}

TABLE 13 – START-UP TIMING

21.2. AUTONOMOUS POWER ON

Connecting WAKEUP output (pad 6) to ON_OFF input (pad 1) enables self-start to Full Power state from Ready-To-Start state following boot process.
When host data interface is set UART, module will start autonomously transmitting NMEA messages after first power supply application. Further transfers between Full Power and Hibernate states require additional logic circuitry combined with serial command.

21.3. VERIFYING THE MODULE HAS STARTED

WAKEUP output will go high indicating module has started.
System activity indication depends upon selected serial interface.
The first message to come out of module is “OK_TO_SEND” - ‘$PSRF150,1*3E’.

21.3.1. UART

When active, the module will output NMEA messages at the 4800bps.

21.3.2. I²C

In Multi-Master mode with no bus contention - the module will spontaneously send messages.
In Multi-Master mode with bus contention - the module will send messages after the I²C bus contention resolution process allows it to send.

21.3.3. SPI

Since module is SPI slave device, there is no possible indication of system "ready" through SPI interface. Host must initiate SPI connection approximately 1s after WAKEUP output goes high.

21.4. SHUTTING DOWN THE MODULE

Transferring module from Full Power state to Hibernate state can be initiated in two ways:

- By a pulse on ON_OFF input.
- By NMEA ($PSRF117) or OSP (MID205) serial message.

Orderly shutdown process may take anywhere from 10ms to 900ms to complete, depending upon operation in progress and messages pending, and hence is dependent upon serial interface speed and controls. Module will stay in Full Power state until TX FIFO buffer is emptied.
The last message during shutdown sequence is '$PSRF150,0*3F'.

22. FIRMWARE

22.1. DEFAULT SETTINGS

Power On State		Hibernate
Default Interface[1]		SPI
SPI Data Format		NMEA
UART Settings		4,800bps.
UART Data Format		NMEA
I²C Settings		Multi-Master 400kbps
I²C Data Format		NMEA
Satellite Constellation		GPS
Elevation Mask		5°
Default Output Messages		$GPGGA @1 sec.
		$GPGSA @ 1 sec.
		$GPGSV @ 5 sec.
		$GPRMC @ 1 sec.
Firmware Defaults	SBAS	OFF
	ABP™	OFF
	Static Navigation	OFF
	Track Smoothing	OFF
	Jammer Detector	ON

	Jammer Remover	OFF
	Fast Time Sync	OFF
	Pseudo DR Mode	ON
	Power Saving Mode	OFF
	3SV Solution Mode	ON
	5Hz Update Rate	OFF

TABLE 14 – DEFAULT FIRMWARE SETTINGS

22.2. FIRMWARE UPDATES

Firmware updates can be considered exclusively as patches on top of baseline ROM firmware. Those patch updates may be provided by OriginGPS to address ROM firmware issues as a method of performance improvement. Typical patch file size is 24KB.
Host controller is initiating load and application of patch update by communicating module's Patch Manager software block allocating 16KB of memory space for patch and additional 8KB for cache. Patch updates are preserved until BBRAM is discarded.

Note:
1. Without external resistor straps on $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$.

23. HANDLING INFORMATION

23.1. MOISTURE SENSITIVITY

ORG1411 modules are MSL 3 designated devices according to IPC/JEDEC J-STD-033B standard.

Module in sample or bulk package should be baked prior to assembly at 125°C for 48 hours.

23.2. ASSEMBLY

The module supports automatic pick-and-place assembly and reflow soldering processes.

Suggested solder paste stencil is 5 mil to ensure sufficient solder volume.

23.3. SOLDERING

Reflow soldering of the module always on component side (Top side) of the host PCB according to standard IPC/JEDEC J-STD-020D for LGA SMD.

Avoid exposure of ORG1411 to face-down reflow soldering process.

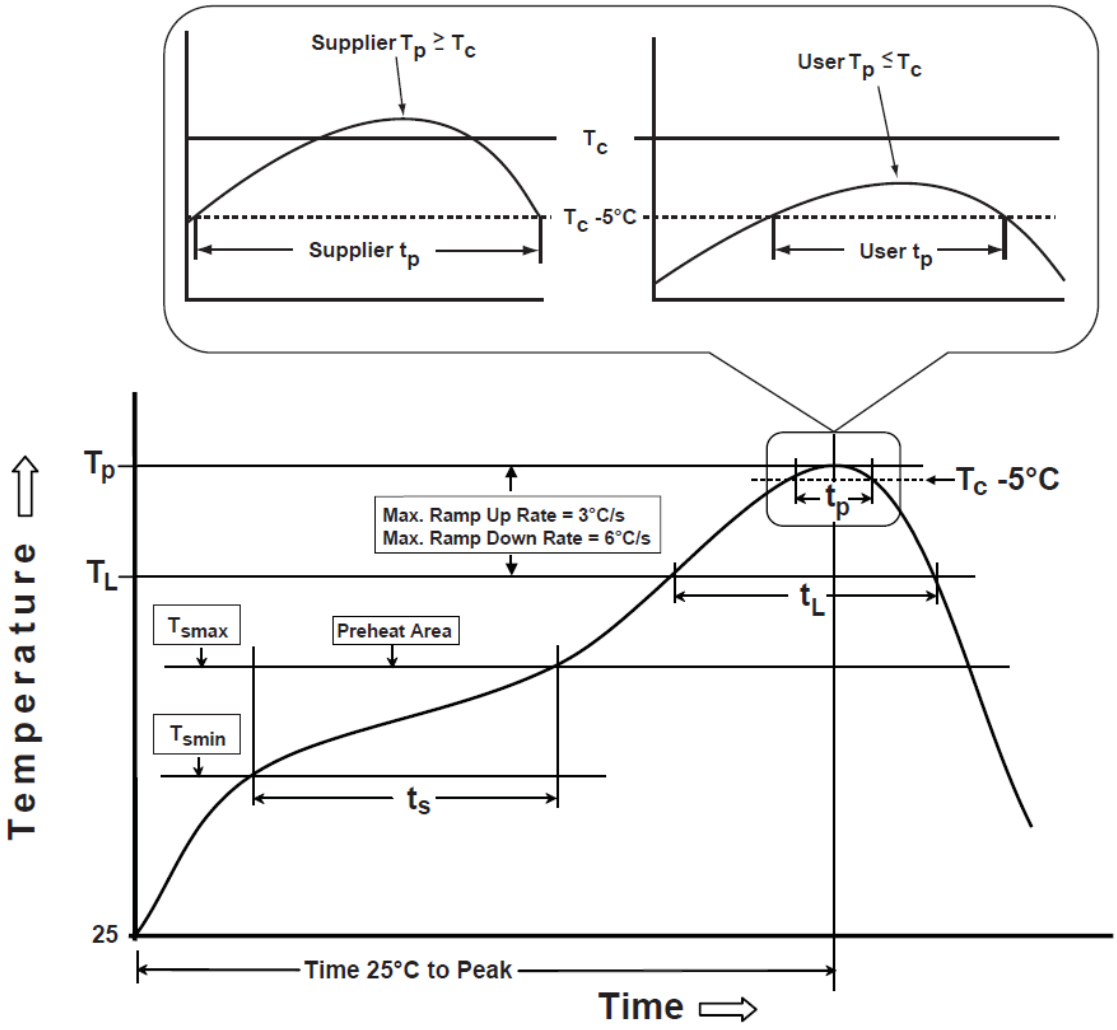

FIGURE 10 – RECOMMENDED SOLDERING PROFILE

Referred temperature is measured on top surface of the package during the entire soldering process.

Suggested peak reflow temperature is 245°C for 30 sec. for Pb-Free solder paste.

Actual board assembly reflow profile must be developed individually per furnace characteristics.

Reflow furnace settings depend on the number of heating/cooling zones, type of solder paste/flux used, board design, component density and packages used.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_C	Classification Temperature		245		°C
T_P	Package Temperature			245	°C
T_L	Liquidous Temperature		217		°C
T_S	Soak/Preheat Temperature	150		200	°C
t_S	Soak/Preheat Time	60		120	s
t_L	Liquidous Time	60		150	s
t_P	Peak Time		30		s

TABLE 15 – SOLDERING PROFILE PARAMETERS

23.4. CLEANING

If flux cleaning is required, module is capable to withstand standard cleaning process in vapor degreaser with the Solvon® n-Propyl Bromide (NPB) solvent and/or washing in DI water.

Avoid cleaning process in ultrasonic degreaser, since specific vibrations may cause performance degradation or destruction of internal circuitry.

23.5. REWORK

If localized heating is required to rework or repair the module, precautionary methods are required to avoid exposure to solder reflow temperatures that can result in permanent damage to the device.

23.6. ESD SENSITIVITY

This product is ESD sensitive device and must be handled with care.

23.7. SAFETY INFORMATION

Improper handling and use can cause permanent damage to the product.

23.8. DISPOSAL INFORMATION

This product must not be treated as household waste.

For more detailed information about recycling electronic components contact your local waste management authority.

24. MECHANICAL SPECIFICATIONS

- ORG1411 module has advanced ultra-miniature LGA SMD packaging sized 10mm x 10mm.
- ORG1411 built on a PCB assembly enclosed with metallic RF shield box and antenna element on top of it.
- There are 10 castellated LGA SMT pads made Cu base and ENIG plating on bottom side.

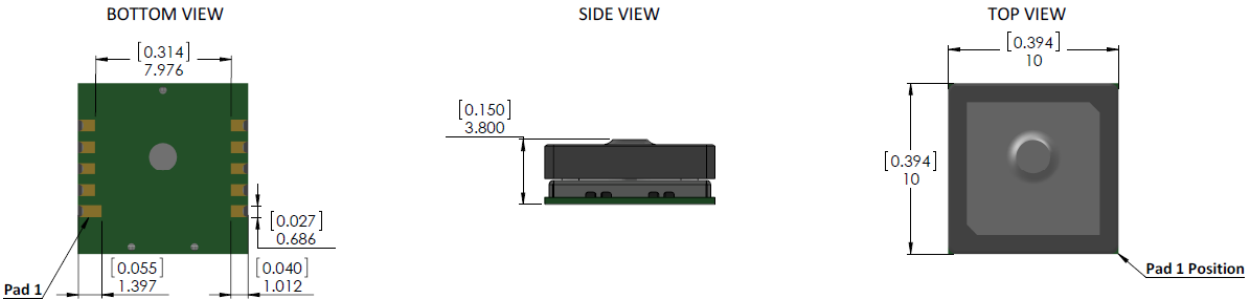

FIGURE 13 – MECHANICAL DRAWING

Dimensions	Length	Width	Height	Weight	
mm	10.00 +0.20/ -0.1	10.00 +0.30/ -0.10	3.80 +0.20/ -0.00	g	1.4
inch	0.394 +0.008/ -0.004	0.394 +0.012/ -0.004	0.150 +0.008/ -0.000	oz	0.045

TABLE 16 – MECHANICAL SUMMARY

25. COMPLIANCE

The following standards are applied on the production of ORG1411 modules:

- IPC-6011/6012 Class2 for PCB manufacturing
- IPC-A-600 Class2 for PCB inspection
- IPC-A-610D Class2 for SMT acceptability

ORG1411 modules are manufactured in ISO 9001:2008 accredited facilities.
ORG1411 modules are manufactured in ISO 14001:2004 accredited facilities.
ORG1411 modules are manufactured in OHSAS 18001:2007 accredited facilities.
ORG1411 modules are designed, manufactured and handled in compliance with the Directive 2011/65/EU of the European Parliament and of the Council of June 2011 on the Restriction of the use of certain Hazardous Substances in electrical and electronic equipment, referred as RoHS II.
ORG1411 modules are manufactured and handled in compliance with the applicable substance bans as of Annex XVII of Regulation 1907/2006/EC on Registration, Evaluation, Authorization and Restriction of Chemicals including all amendments and candidate list issued by ECHA, referred as REACH.
ORG1411 modules comply with the following EMC standards:

- EU CE EN55022:06+A1(07), Class B
- US FCC 47CFR Part 15:09, Subpart B, Class B
- JAPAN VCCI V-3/2006.04

26. PACKAGING AND DELIVERY

26.1. APPEARANCE

ORG1411 modules are delivered in reeled tapes for automatic pick and place assembly process.

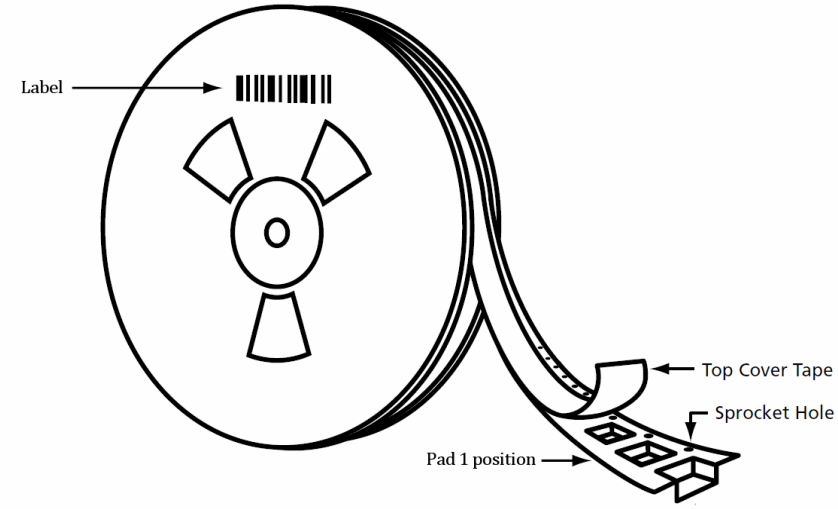

FIGURE 11 – MODULE POSITION

ORG1411 modules are packed in 2 different reel types.

SUFFIX	TR1	TR2
Quantity	150	500

TABLE 17 – REEL QUANTITY

Reels are dry packed with humidity indicator card and desiccant bag according to IPC/JEDEC J-STD-033B standard for MSL 3 devices.

Reels are vacuum sealed inside anti-static moisture barrier bags.

Sealed reels are labeled with MSD sticker providing information about:

- MSL
- Shelf life
- Reflow soldering peak temperature
- Seal date

Sealed reels are packed inside cartons.

Reels, reel packs and cartons are labeled with sticker providing information about:

- Description
- Part number
- Lot number
- Customer PO number
- Quantity
- Date code

26.2. CARRIER TAPE

Carrier tape material - polystyrene with carbon (PS+C).

Cover tape material – polyester based film with heat activated adhesive coating layer.

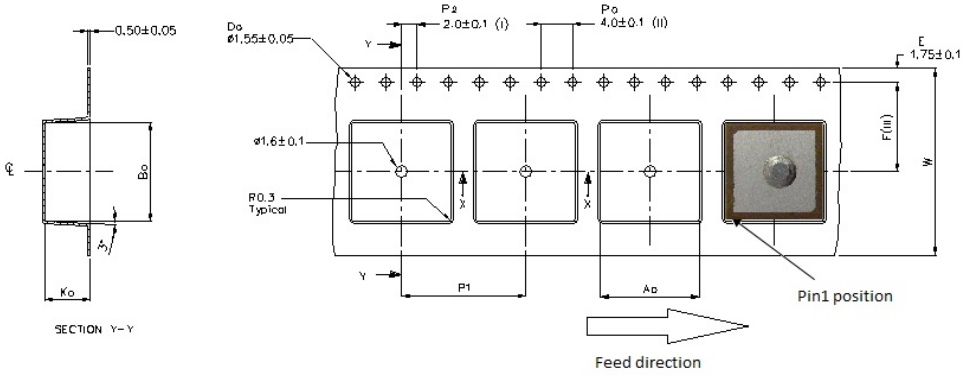

FIGURE 15 – CARRIER TAPE

	mm	inch
A_0	10.9 ± 0.1	0.429 ± 0.004
B_0	10.7 ± 0.1	0.421 ± 0.004
K_0	6.1 ± 0.1	0.240 ± 0.004
F	7.5 ± 0.1	0.295 ± 0.004
P1	12.0 ± 0.1	0.472 ± 0.004
W	16.0 ± 0.3	0.630 ± 0.012

TABLE 18 – CARRIER TAPE DIMENSIONS

26.3. REEL

Reel material - antistatic plastic.

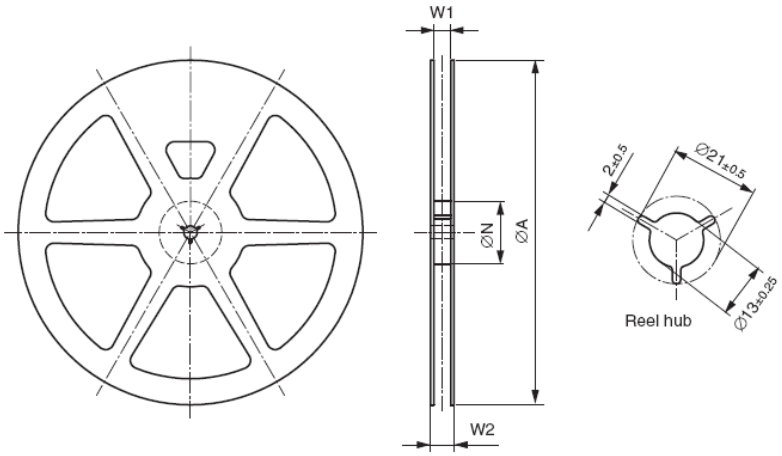

FIGURE 16 – REEL

SUFFIX	TR1		TR2	
	mm	inch	mm	inch
ØA	178.0 ± 1.0	7.00 ± 0.04	330.0 ± 2.0	13.00 ± 0.08
ØN	60.0 ± 1.0	2.36 ± 0.04	102.0 ± 2.0	4.02 ± 0.08
W1	16.7 ± 0.5	0.66 ± 0.02	16.7 ± 0.5	0.66 ± 0.02
W2	19.8 ± 0.5	0.78 ± 0.02	22.2 ± 0.5	0.87 ± 0.02

TABLE 19 – REEL DIMENSIONS

27. ORDERING INFORMATION

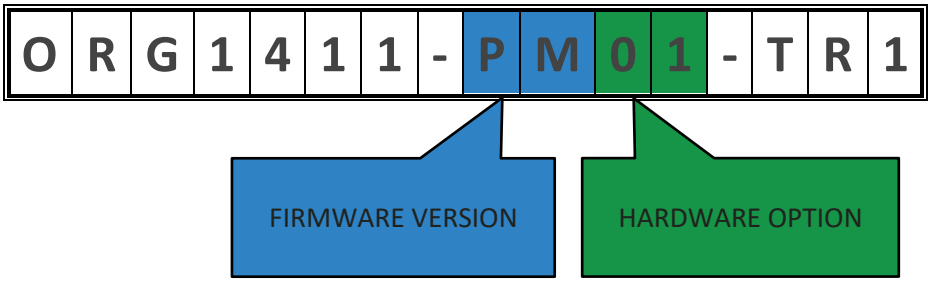

TABLE 20 – ORDERING OPTIONS

PART NUMBER	FW VERSION	HW OPTION	V_{CC} RANGE	PACKAGING	SPQ
ORG1411-PM01-TR1	3	01	1.8V	REELED TAPE	150
ORG1411-PM01-TR2	3	01	1.8V	REELED TAPE	500
ORG1411-PM01-UAR	3	01	5V USB	EVALUATION KIT	1
ORG1411-PM04-TR1	3	02	2.0V to 5.5V	REELED TAPE	150
ORG1411-PM04-TR2	3	02	2.0V to 5.5V	REELED TAPE	500

TABLE 21 – ORDERABLE DEVICES

28. I2C Appendix

Sirf 4 I2C Interface appendix

I²C host interface features are:

- I²C Multi-Master mode - module initiates clock and data, default operating speed 400kbps.
- I²C address '0x60' for commands from controller to GPS-module. (Default)
- I²C address '0x62' for the data transmits from the GPS-module to the host. (Default)
- Individual transmit and receive FIFO length of 64 bytes.
- SCL and SDA are pseudo open-drain lines, therefore require external pull-up resistors of 2.2kΩ to 1.8V, or 3.3kΩ to 3.3V.
- Multi-Master mode – the Host (MCU) can operate either in Slave mode or Multi-Master mode (more common). If MCU is acting as slave, then it can only listen to the GPS.
  If you want to send any configuration commands to GPS, then host needs to be in Master or Multi master mode.
- While Host (MCU) is in Master/Multi-Master mode, the following can be changed:

1) Clock rate can be switched to 100KHz (OSP command).
2) I²C address, (OSP command)
3) OSP/NMEA mode
4) GPS can be turn into a Slave mode by sending OSP Message ID 178, Sub ID 2 input command.

Change the GPS module from Multi master to Slave mode:

a. change from NMEA to OSP - "$PSRF100,0,115200,8,1,0*04\r\n".
b. Change to Slave mode with 400Kbps, send:
c. A0 A2 00 39 B2 02 00 F9 C5 68 03 FF 00 00 0B B8 09 0B 38 F9 00 01 03 FC 03 FC 00 04 00 3E 00 00 00 7C 00 00 00 00 00 00 00 00 00 00 00 00 00 01 C2 00 00 00 62 00 60 01 00 01 F4 00 01 0B 1D B0 B3 0D 0A
d. Read 128 Bytes at least from the GPS module, and then immediately without any delay send the next OSP message.
e. If you want to switch back from OSP to NMEA please use command
   A0 A2 00 18 81 00 01 01 01 01 01 01 05 01 01 01 01 01 00 01 00 01 00 01
   00 00 12 C0 01 66 B0 B3

GPS multi master	Host Salve
I²C address '0x60'	I²C address '0x62'
GPS slave	Host Master
I²C address '0x60'	I²C any address