Altair Logix, LLC v. SparkFun Electronics, Inc., Case No. 1:21-cv-1751
Exhibit A: '083 Invalidity Chart ("Gove")

Claim Language	Texas Instruments' US Patent No. 5,522,083 ("Gove")
1. An apparatus for processing data, comprising:	The '083 Patent, assigned to Texas Instruments, discloses all limitations of Claim 1, the only claim allowed for the asserted '434 Patent. The Gove reference is a continuation of Ser. No. 437,856, which was filed in November of 1989, *i.e.,* almost a decade before the asserted '434 patent. For example, in its complaint, Altair stated, "An exemplary block diagram of the claimed systems is shown in Figure 3 of the '434 [*sic*] patent". Complaint, ¶23. Fig 3 of the '434 Patent contains the same teachings as Fig 62 in the '083 Patent. SparkFun does not believe the preamble is limiting, but the '083 Patent clearly discloses an apparatus for processing data, as shown below.
[a] an addressable memory for storing the data, and a plurality of instructions, and having a plurality of input/outputs, each said input/output for providing and receiving at least one selected from the data and the instructions;	The '083 Patent teaches this limitation, including an addressable memory and a plurality of instructions and inputs/outputs: "A multi-processing system is shown with n processors, each processor operable from **instruction sets** provided from a memory source for controlling a number of different processes, which rely on the movement of data to or from one or more **addressable memories** with m memory sources **each having a unique addressable space**, where m is greater than n and having **a switch matrix connected to the memories and connected to the processors** and with circuitry for selectively and concurrently enabling the switch matrix on a processor cycle by cycle basis for interconnecting any of the processors with any of the memories for the interchange between the memories and the connected processors of instruction sets from one or more addressable memory spaces and data from other addressable memory spaces." 60:66-61:12 (emphasis added). Further, the asserted '434 Patent teaches that this configuration can be accomplished with a matrix, and the '083 contains the same teaching. *See* '083 FIG 4.

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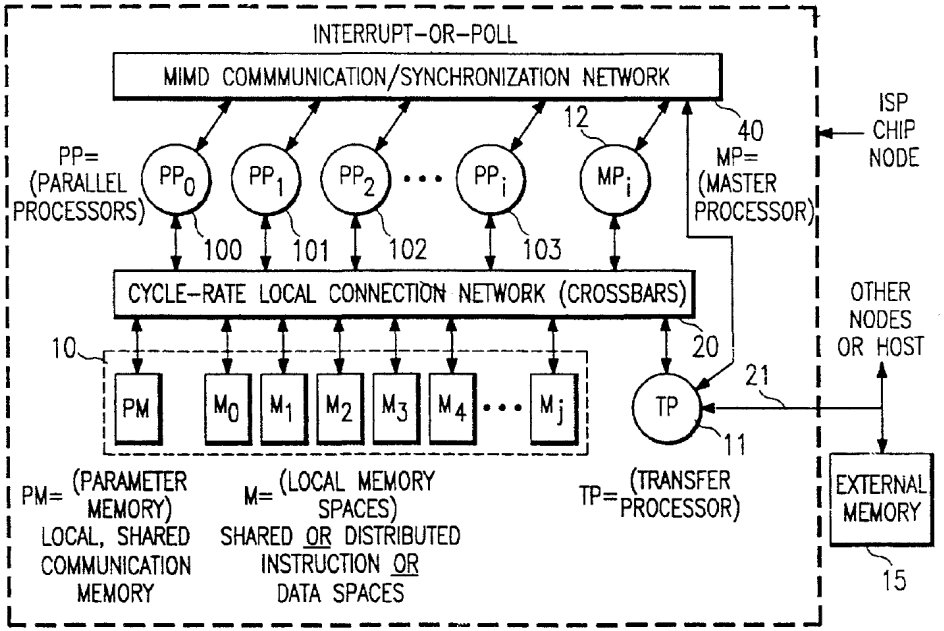
[b] a plurality of media processing units, each media processing unit having an input/output coupled to at least one of the addressable memory input/outputs and comprising:	The '083 Patent teaches this limitation, including a plurality of media processing units, each media processing unit having an input/output coupled to at least one of the addressable memory input/outputs.  *FIG. 1* "There is disclosed a **multiprocessor system** [plurality of MPUs] and method arranged, in one embodiment, as an image and graphics processor. The processor is structured with several **individual processors all having communication links to several memories without restriction**." Abstract (emphasis added). "This invention relates generally to **multiprocessor systems** and more particularly to such systems and methods where the intercommunications between the several

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	processors is adaptable to the operational mode of the processors at any point in time." 1:13-16. "SUMMARY OF THE INVENTION These problems have been solved by designing a **multiprocessing system** to handle image processing and graphics and by constructing a crossbar switch capable of interconnecting any processor with any memory in any configuration for the interchange of data. **The system is capable of connecting n parallel processors to m memories where m is greater than n**. A communication bus is established outside of the switch which allows interrupts to be transmitted between selected processors." 3:7-17 (emphasis added). "FIG. 10 shows the reconfigurable SIMD/MIMD topology of this invention where several parallel processors can be interconnected via crossbar switch 20 to a series of memories 10 and can be connected via a transfer processor 11 to external memory 15, all on a cycle by cycle basis." 10:14-19. "A multi-processing system is shown with n processors, each processor operable from instruction sets provided from a memory source for controlling a number of different processes, which rely on the movement of data to or from one or more addressable memories with m memory sources each having a unique addressable space, where m is greater than n and having a switch matrix connected to the memories and connected to the processors and with circuitry for selectively and concurrently enabling the switch matrix on a processor cycle by cycle basis for interconnecting any of the processors with any of the memories for the interchange between the memories and the connected processors of instruction sets from one or more addressable memory spaces and data from other addressable memory spaces." 60:66-61:12. *See also* preamble, *supra*.

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[b][i] a multiplier having a data input coupled to the media processing unit input/output, an instruction input coupled to the media processing unit input/output, and a data output coupled to the media processing unit input/output;	The '083 Patent teaches this limitation, including disclosing a multiplier with data input/output coupled to the MPU and instruction input coupled to the MPU: "In addition to integer execution unit (ALU-arithmetic logic unit) 2902, there is a floating point execution unit comprised of two parts. Part one is **a floating point multiplier** comprised of **multiplier 2905**, normalized circuit 2906 and exponent adder 2907. Part two is a floating point adder comprised of prenormalizer 2908 and arithmetic unit 2909 and postnormalizing shifter 2910." 35:13-19 (emphasis added).

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	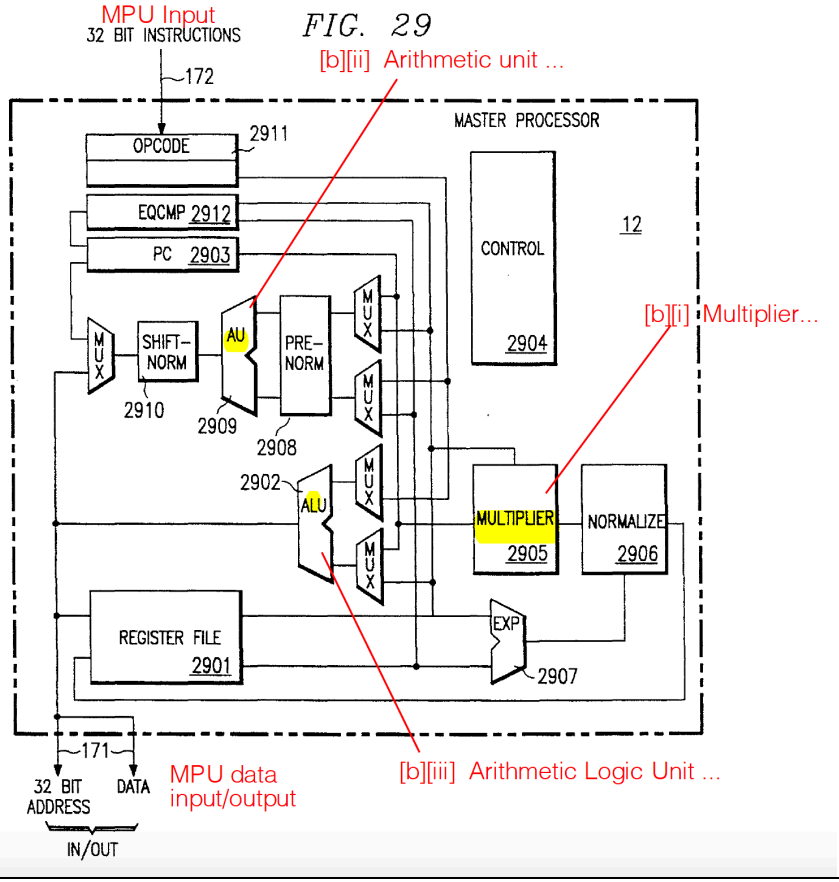

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	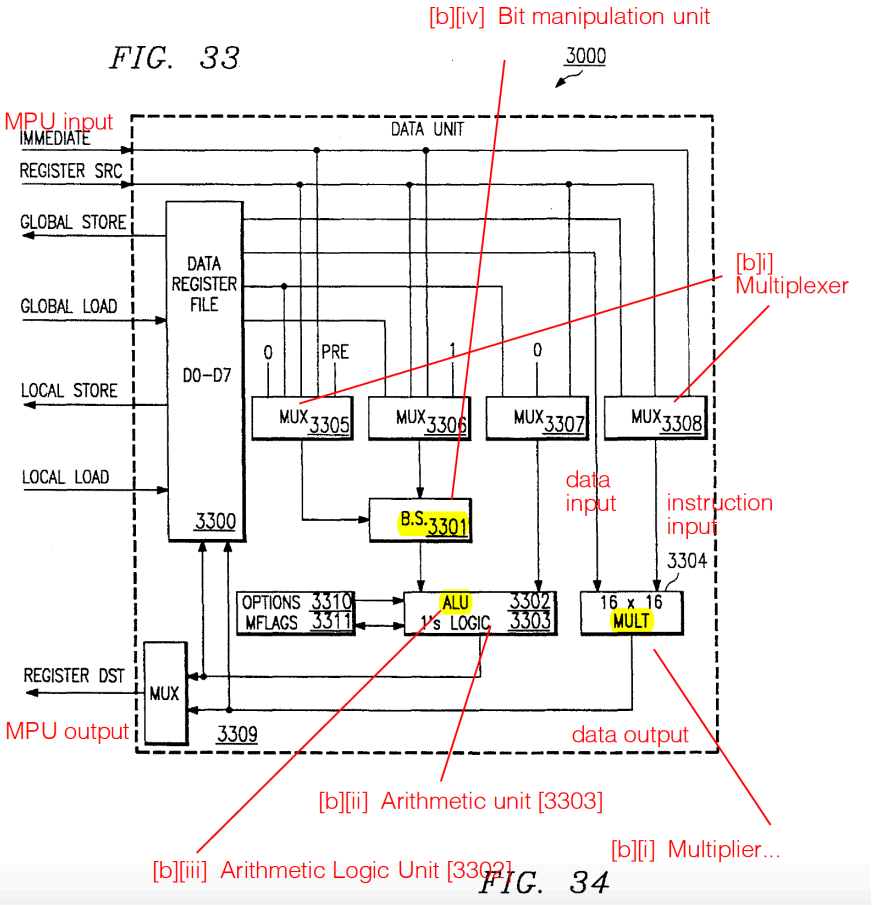
[b][ii] an arithmetic unit having a data input coupled to the media processing unit input/output, an instruction input coupled to the media processing unit input/output, and a data output coupled to the media processing unit input/output;	The '083 Patent teaches this limitation, including disclosing an AU with data input/output coupled to the MPU and instruction input coupled to the MPU: *See* arithmetic unit 2909, FIG 29, *supra*.

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	"In addition to integer execution unit (ALU-arithmetic logic unit) 2902, there is a floating point execution unit comprised of two parts. Part one is a floating point multiplier comprised of multiplier 2905, normalized circuit 2906 and exponent adder 2907. Part two is a floating point adder comprised of prenormalizer 2908 and **arithmetic unit 2909** and postnormalizing shifter 2910." 35:13-19 (emphasis added).
[b][iii] an arithmetic logic unit having a data input coupled to the media processing unit input/output, an instruction input coupled to the media processing unit input/output, and a data output coupled to the media processing unit input/output, capable of operating concurrently with at least one selected from the multiplier and arithmetic unit; and	The '083 Patent teaches this limitation, including disclosing an ALU with data input/output coupled to the MPU and instruction input coupled to the MPU, capable of operating concurrently with at least one selected from the multiplier and arithmetic unit: *See* ALU 2909, FIGS 29, 34, *supra*. "In addition to integer execution unit (**ALU-arithmetic logic unit) 2902**, there is a floating point execution unit comprised of two parts. Part one is a floating point multiplier comprised of multiplier 2905, normalized circuit 2906 and exponent adder 2907. Part two is a floating point adder comprised of prenormalizer 2908 and arithmetic unit 2909 and postnormalizing shifter 2910." 35:13-19. "There are eight D (data registers 3300) within data unit 3000. These are general purpose 32-bit data registers. They are multi-ported and therefore allow a great deal of parallelism. **Four sources can be provided to ALU 3302 and multiplier 3304 <u>at the same time</u> as two transfers to/from memory are occurring**." 55:24-29 (emphasis added).

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	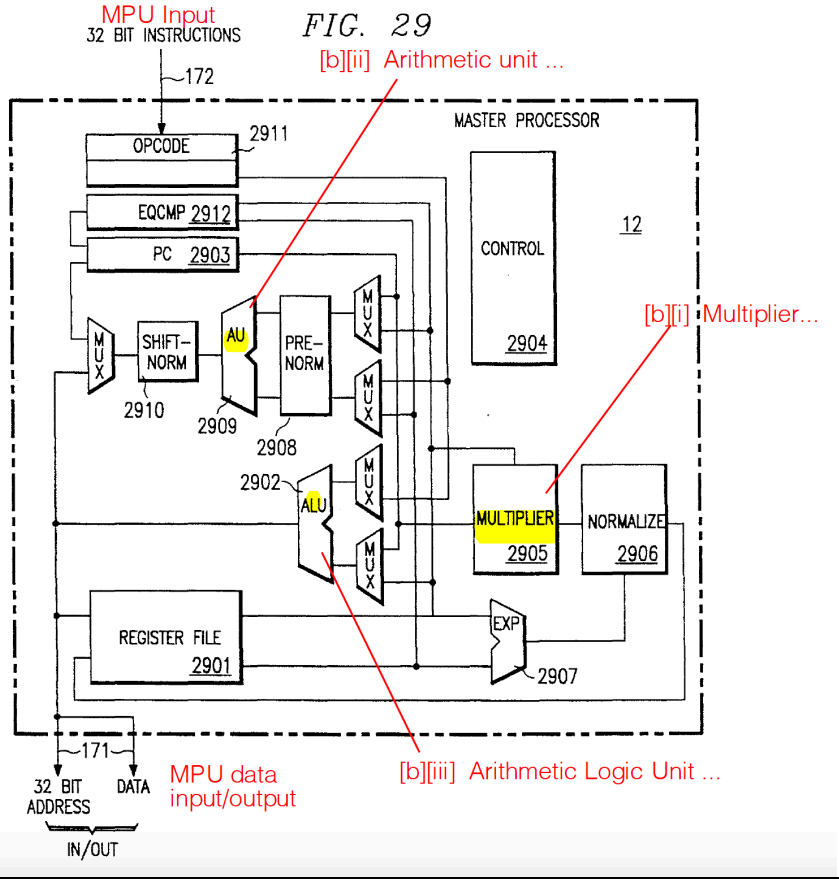

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	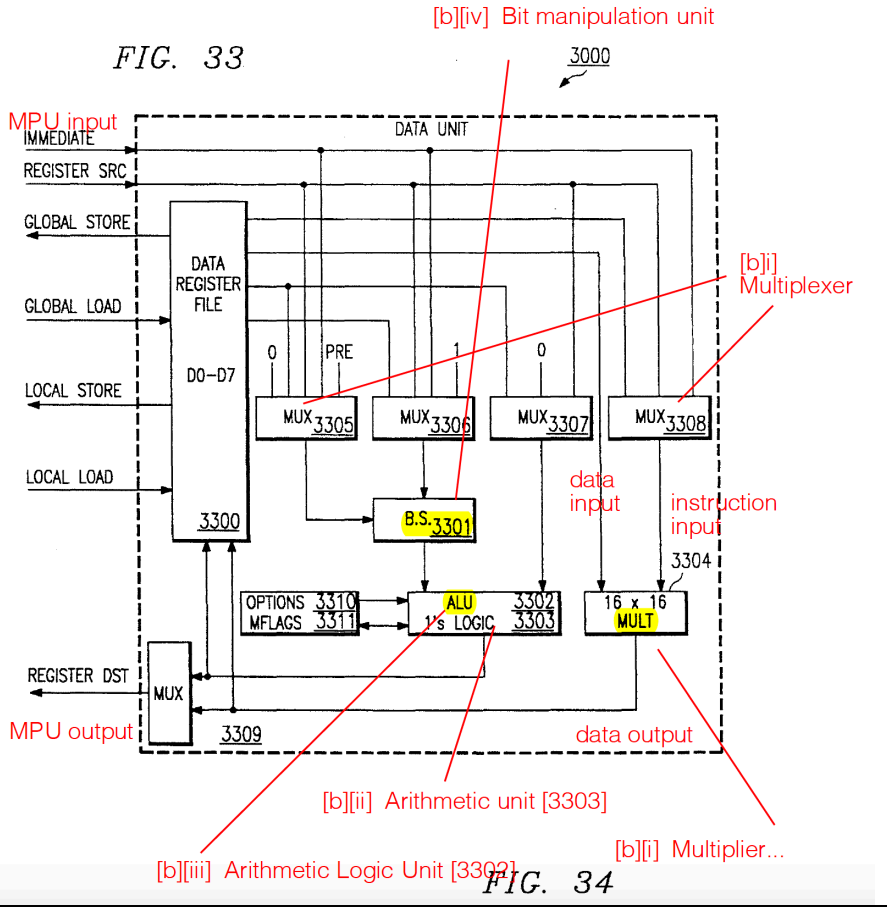

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	Pipeline control can be difficult. The reason for this is the number of concurrent operations that interrelate as demonstrated below: Instruction fetch with associated cache management. Address generations with various addressing modes. Crossbar access requests with independent contention resolution. Memory transfers. Loop address compare, with PC load/increment. Loop count decrement/reload. Looping depth count decrement/reload. Multiply. Shift. Add/subtract. Synchronization with other PPs. Interrupt detection/prioritization. The pipeline "events" that cause an "abnormality" in the straightforward execution of linear code are: Instruction cache-miss Contention on the Global and/or Local buses Loops Branches and calls Interrupts Idling Synchronization 47:9-38.
[b][iv] a bit manipulation unit having a data input coupled to the media processing unit input/output, an instruction input coupled to the media processing unit input/output, and a data output coupled to the media processing unit input/output,	The '83 Patent discloses, *inter alia,* the use of barrel shifters, which were then-common bit manipulators, in the manner claimed: *See* FIGs 29, 34, *supra*.

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capable of operating concurrently with the arithmetic logic unit and at least one selected from the multiplier and arithmetic unit;	"A block diagram of data unit 3000 is given in FIG. 33. The major components of the unit consist of 8 Data registers 3300, **1 full barrel shifter** 3301, a 32-bit ALU 3302, a single-cycle 16×16 multiplier 3304, special hardware for handling logical ones 3303, and a number of multiplexers 3305-3309. Also included are two registers 3310 or 3311 closely associated with the **barrel shifter 3301** and the ALU 3302. They control the operation of these two devices when certain instructions are executed." 38:28-32 (emphasis added). "A block diagram of data unit 3000 is given in FIG. 33. The major components of the unit consist of 8 Data registers 3300, **1 full barrel shifter** 3301, a 32-bit ALU 3302, a single-cycle 16x16 multiplier 3304, special hardware for handling logical ones 3303, and a number of multiplexers 3305-3309. Also included are two registers 3310 or 3311 closely associated with the **barrel shifter 3301** and the ALU 3302. They control the operation of these two devices when certain instructions are executed." 55:15-23 (emphasis added). "**Barrel shifter 3301 resides on the 'inverting' input to ALU 3302. This allows the possibility of performing shift and add, or shift and subtract operations using a predefined shift amount set up in the OPTIONS register 3310**. This is very useful, especially since the multiplier has no result scaler. **Barrel shifter 3301 can shift left or right by 0-31 bit positions, and can also do a 0-31 bit rotation**." 55:50-57 (emphasis added). "There are eight D (data registers 3300) within data unit 3000. These are general purpose 32-bit data registers. They are multi-ported and therefore allow a great deal of parallelism. **Four sources can be provided to ALU 3302 and multiplier 3304 at the same time as two transfers to/from memory are occurring**." 55:24-29 (emphasis added).

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	Pipeline control can be difficult. The reason for this is the number of concurrent operations that interrelate as demonstrated below: Instruction fetch with associated cache management. Address generations with various addressing modes. Crossbar access requests with independent contention resolution. Memory transfers. Loop address compare, with PC load/increment. Loop count decrement/reload. Looping depth count decrement/reload. Multiply. Shift. Add/subtract. Synchronization with other PPs. Interrupt detection/prioritization. The pipeline "events" that cause an "abnormality" in the straightforward execution of linear code are: Instruction cache-miss Contention on the Global and/or Local buses Loops Branches and calls Interrupts Idling Synchronization 47:9-38. *See* FIGs 29, 34, *supra*.
[c] each of the plurality of media processors for performing at least one operation, simultaneously with the	The '083 discloses a plurality of MPUs performing at least one operation simultaneously with another by other MPUs. The subliminations of [c] are well-known operations of any processor.

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performance of other operations by other media processing units, each operation comprising:	"Imaging systems which obtain visual images and perform various manipulations with respect to the data and then control the display of the imaged and stored data inherently require large amounts of computations and memory. **Such imaging systems are prime candidates for multi-processing where different processors perform different tasks concurrently in parallel**. These processors can be working together in the single instruction, multiple data mod (SIMD) where all of the processors are operating from the same instruction but obtaining data from various sources, **or the processors can be working together in the multiple instruction, multiple data mode (MIMD) where each processor is working from a different set of instructions and working on data from different sources**. For different operations, different configurations are necessary." 2:3-17 (emphasis added). "This is in contrast to the MIMD mode where data from various parts of the image **is being processed concurrently**, some using different algorithms. In this arrangement, **different instructions are operating on different data at the same time to achieve a desired result**. **A simple example would include many different SIMD algorithms** (like clean, enhance, extract) **operating concurrently or pipelined on many different processors**. Another example with MIMD would include the implementation of algorithms with the same data flow although using unique arithmetic or logical functions." 9:57-67 (emphasis added). "Sliced addressing is a technique for taking adjacent information from one memory space and distributing it in a manner to a number of separate different memory spaces so that the information when it has been distributed can be accessed simultaneously by a number of processors without contention." 23:2-8 "This would occur anytime when it is conceivable that several processors would be accessing the same type of information at the same time for whatever processing would be occurring at that point." 24:49-53

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	"The compact structure of the image processing system, where all of the parallel processing and memory interaction is available on a single chip coupled with a wide flexibility of processor memory configurations and operational modes, all chip controlled, contributes to the ability of the imaging PC to accept image data input as well as ASCII input and to allow the two types of data to be simultaneously utilized." 29:57-63. "Parallel Processor Operation The four processors 100-103 shown in FIGS. 1 and 2 (abbreviated PP herein) perform most of the system's operations. The PP's each have a high degree of parallelism enabling them to perform the equivalent of many reduced instruction set computer (RISC)-like operations per cycle. Together they provide a formidable data processing capability, particularly for image and graphics processing. Each PP can perform three accesses per cycle, through the crossbar switch to the memory, one for instructions and two for data. A multiply and an ALU operation can also be performed by each PP every cycle, as well as generating addresses for the next two data transfers. Efficient loop logic allows a zero cycle overhead for three nested loops. Special logic is included for handling logical ones, and the ALU is splittable for operating on packed pixels. As discussed previously, to allow flexibility of use, the PPs can be configured to execute from the same instruction stream (Single Instruction Multiple Data (SIMD) mode) or from independent instruction streams (Multiple Instruction Multiple Data (MIMD) mode). MIMD mode provides the capability of running the PPs together in lock-step allotting for efficient synchronized data transfer between processors.

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	In order to relieve the programmer of the worries of accidental simultaneous access attempts of the same memory, contention prioritization logic is included in the crossbar, and retry logic is included in the PPs." 35:45-36:6 *See* also preamble, lim[c], FIGs 29, 34, *supra*. *See also* US Patent No. 5,592,405 (Assignee Texas Instruments, also to named inventor "Gove"): "There is thus a need in the art for a system which handles multi-processors having multi-memories such that the address space from all of the memories is available to one or more processors concurrently even when the processors are handling different instruction sets." 2:5-9.

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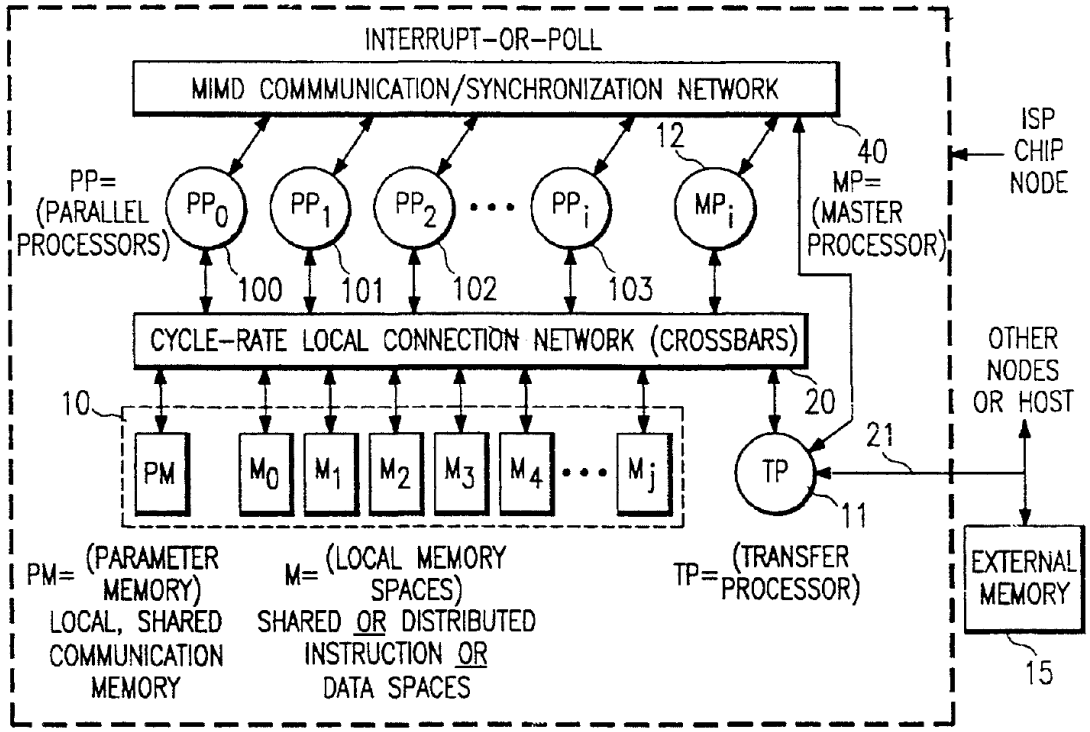
[c][i] receiving at the media processor input/output an instruction from the memory;	 *FIG. 1*

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	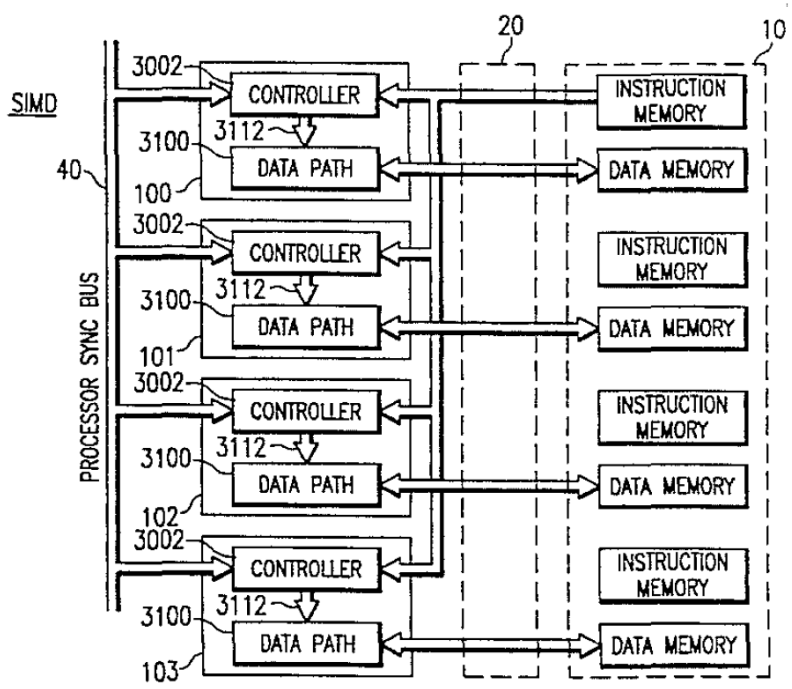 FIG 62; *see also* FIGS 61-64 and accompanying specification teachings, including: "FIG. 61 shows an embodiment of the system which is the subject of this invention where the system is configured to behave in a MIMD mode. Via the crossbar 20, **each parallel processor (100, 101, 102, or 103) can each use a memory within the memory space 10 as its instruction memory**. The controller 3002 of each parallel processor thus can get its own different instruction stream. The synchronization signals in bus 40 are ignored by each parallel processor that is configured to be in the MIMD mode of operation. Since each controller can control via control signals 3112 a different

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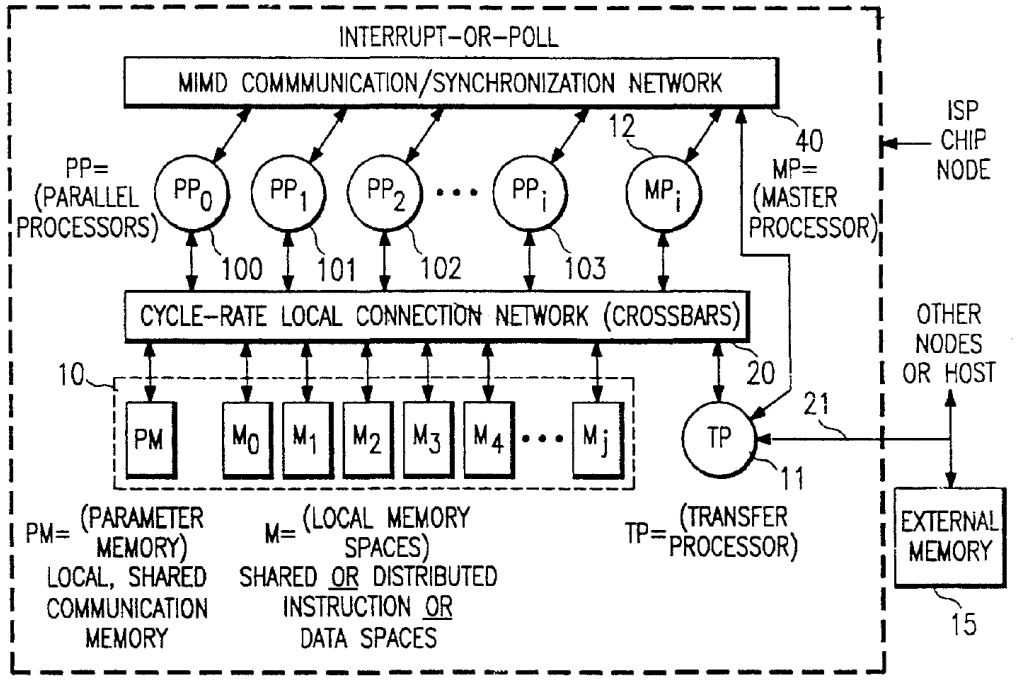
	data path 3100 and each data path can have access to a different memory via the crossbar, the system can operate in a MIMD mode." *See* also preamble, lim[c], FIGs 29, 34, *supra*.
[c][ii] receiving at the media processor input/output data from the memory;	 *FIG. 1*

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	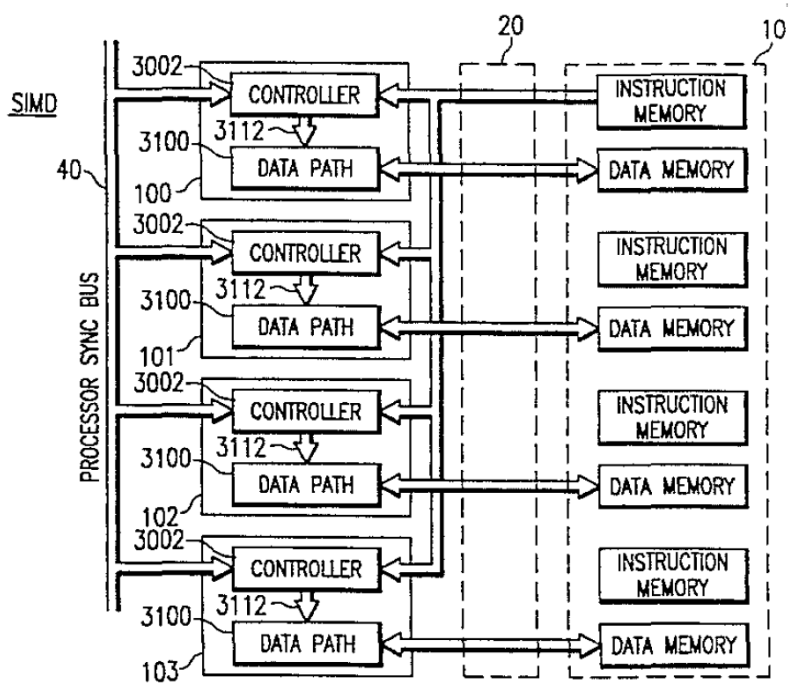 FIG 62; *see also* FIGS 61-64 and accompanying specification teachings. *See* also preamble, lim[c], FIGs 29, 34, *supra*.

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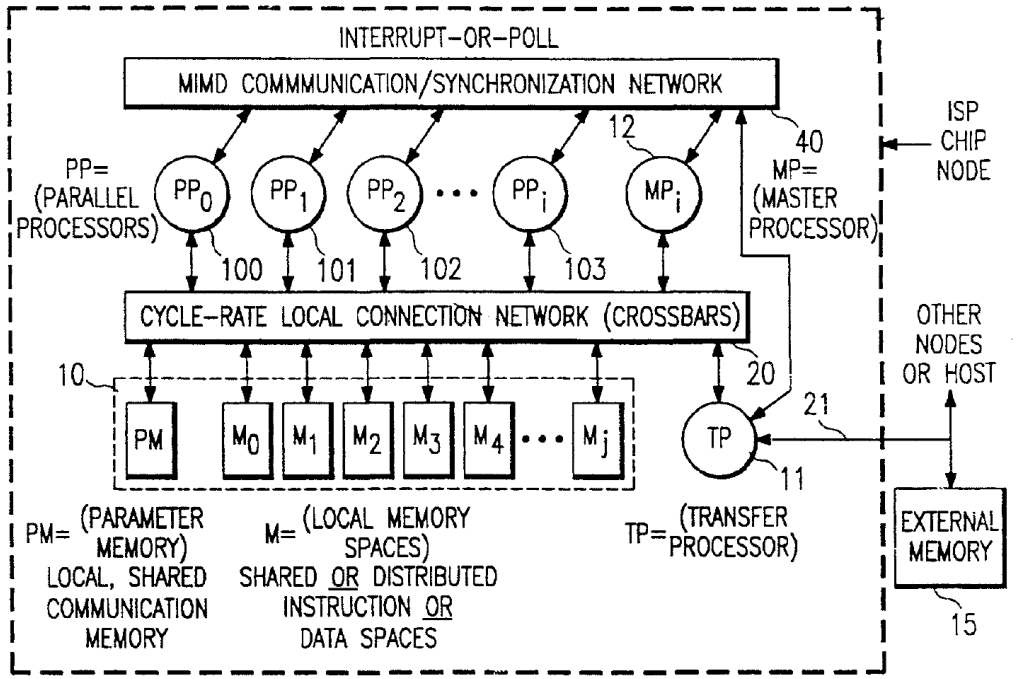
[c][iii] processing the data responsive to the instruction received to produce at least one result; and	 *FIG. 1*

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	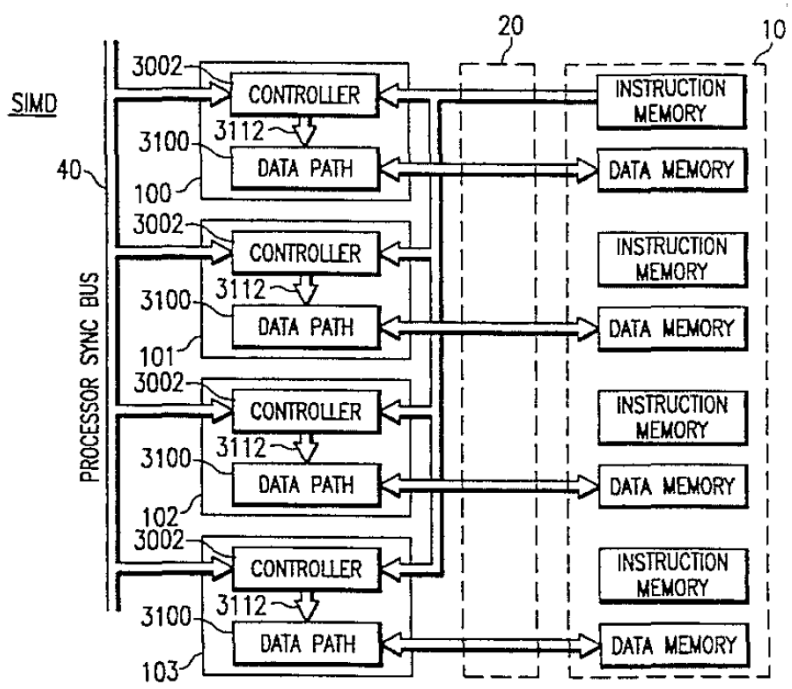 *See* FIGS 61-64 and accompanying specification teachings. *See* also preamble, lim[c], FIGs 29, 34, *supra*.

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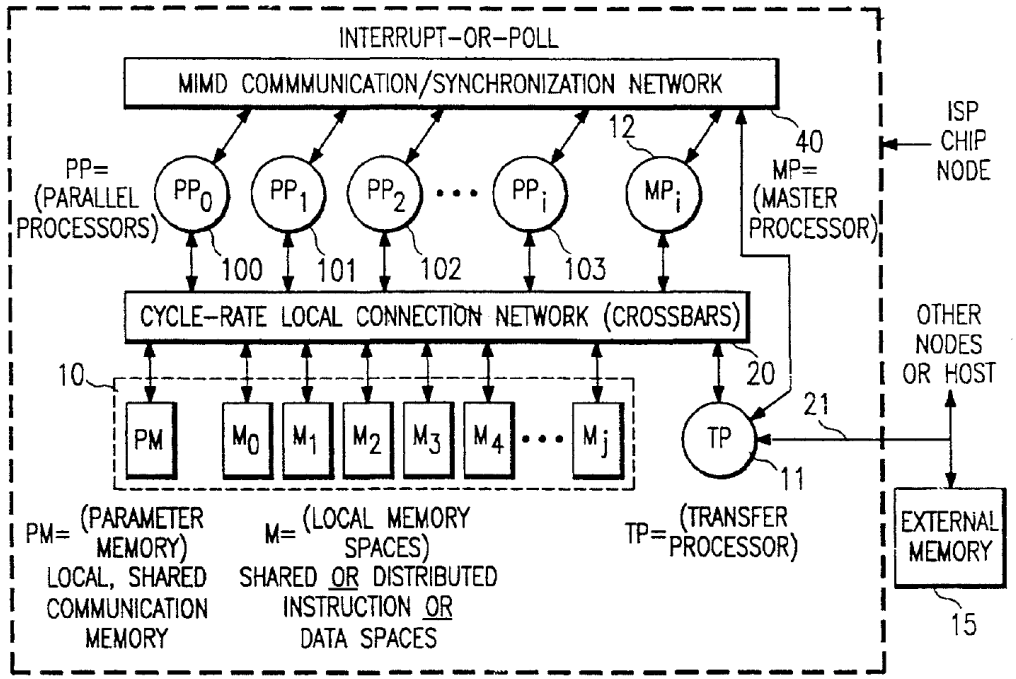
[c][iv] providing at least one of the at least one result at the media processor input/output.	 *FIG. 1*

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	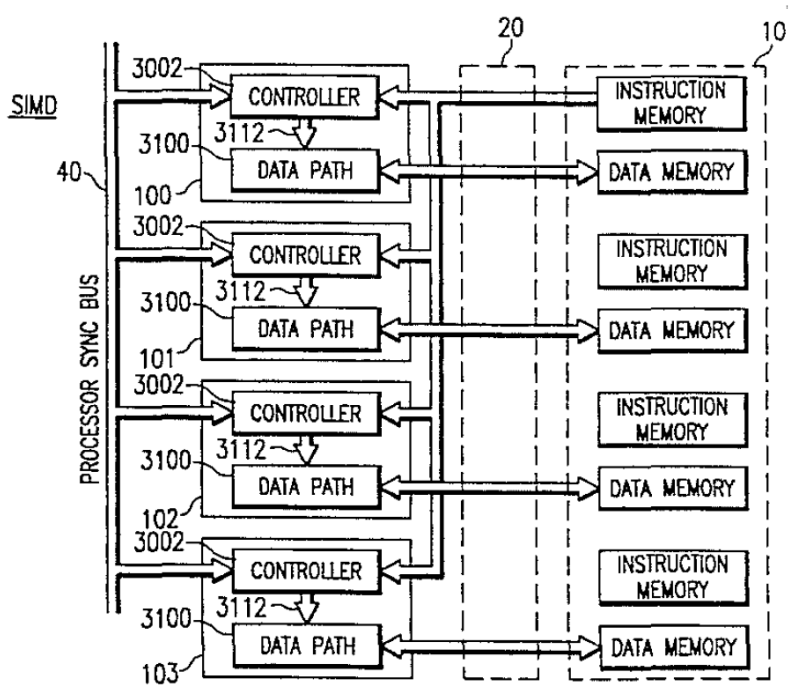 FIG 62; *see also* FIGS 61-64 and accompanying specification teachings. *See* also preamble, lim[c], FIGs 29, 34, *supra*.