Product Brief

SPARK X

rev. 0.3.1 8/4/2016

Introduction

The SP250Ψ is a Neuromorphic Processing Unit with architecture derived from generations of improvement on the "Golden Sunflower" core. Unlike its predecessors, such as the SP140σ, the SP250Ψ is the first SP-series NPU to exploit instruction level parallelism (ILP), greatly increasing overall instruction speed and reducing model degradation between layers.

The very long instruction word (VLIW) architecture of the SP250Ψ comprises as many as 256 proprietary processing cores complemented with a variety of Application Specific Instruction-set Processor (ASIP) reductions which allow the device to execute deep, feed-forward operations while maintaining agility of interaction.

Features

- Very Long Instruction Word (VLIW) Architecture
- 256 "Golden Sunflower" Processing Cores
- Power-on reset (POR) and brown-out detection (BOD)
- Idle and standby sleep modes
- Voltage Oscillation Reporting To EXternal Systems (VORTEXs) simplifies error code retrieval
- 1.62V – 3.63V Operating Voltage
- External BIOS Support
- One full-speed (12Mbps) Universal Serial Bus (USB) 2.0 interface
- Mass Storage Controller

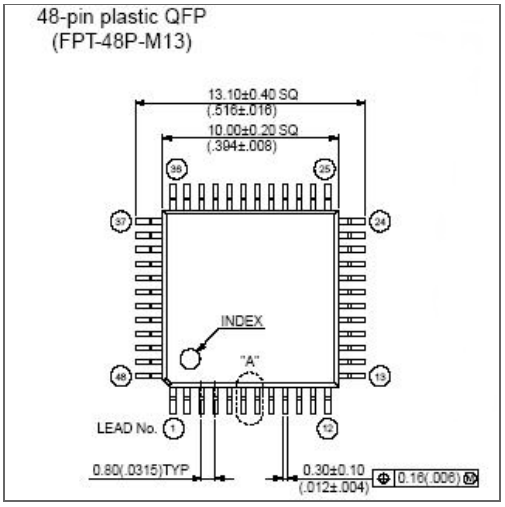

Fig.1a Mechanical Package Drawing

Contents

2. Electrical Characteristics

2.1 Electrical Specifications

Symbol	Parameter	Min	Typ	Max	Units
Electrical Parameters					
V_{DD}	Supply Voltage	1.62[1]	3.3	3.63	V
I_{DD}	Supply Current			70	mA
P	Power Consumption		120	400	mW
Electrostatic Discharge					
ESD_{HBM}	Human Body Model			±2000	V
Environmental Parameters					
T_{OP}	Operating Temp.	-40		105[2][3]	°C

Fig.2a Electrical Characteristics Table

note(s):

1. The minimum supply voltage V_{DD} is 1.8V and should not drop below this value for reliable device operation.
2. Limited by reliability of non-volatile memory.
3. See “Thermal Instability in Timing Operations” Supplemental

2.2 Block Diagram

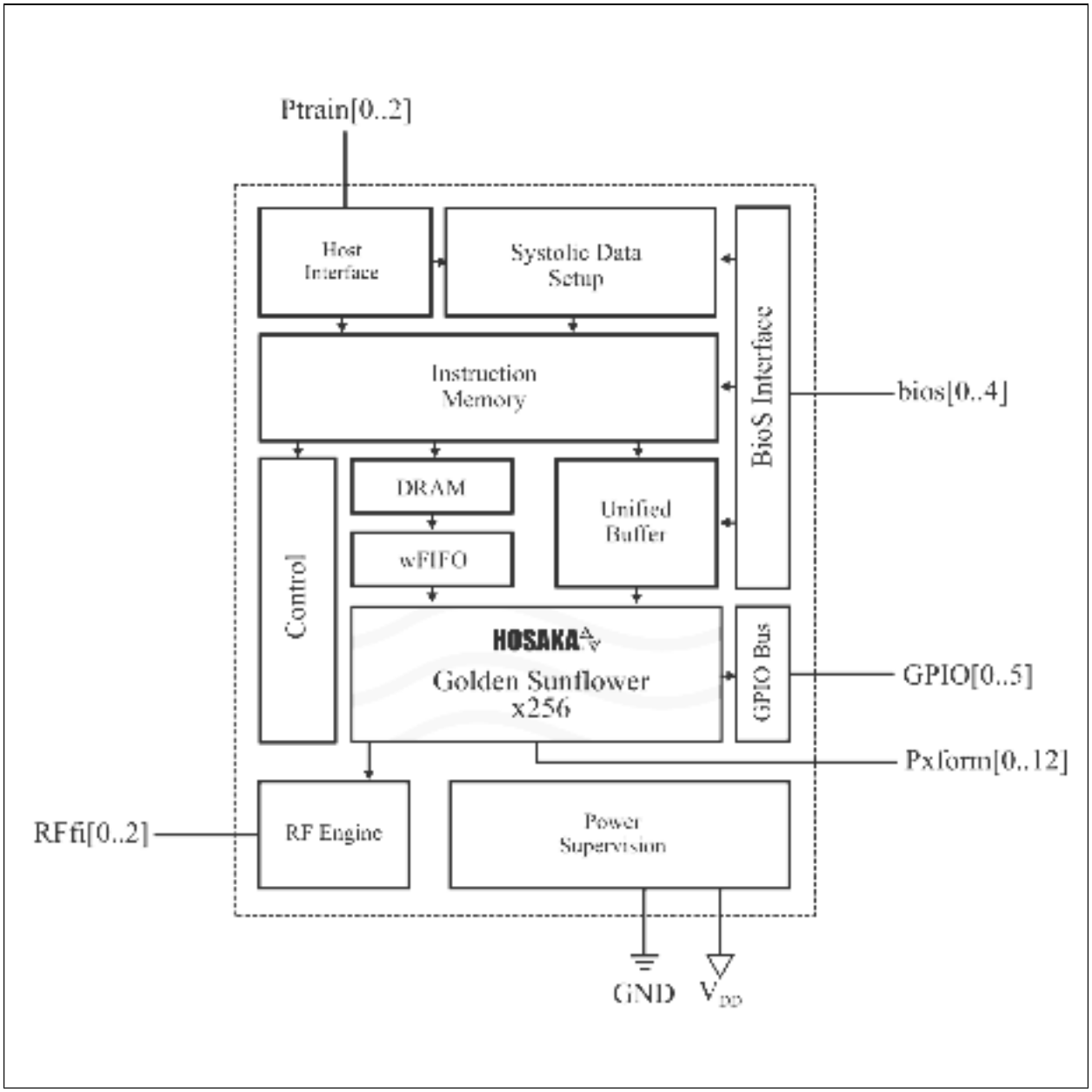

Fig.2b NPU Block Diagram

3. BioS Compatibility

3.1 BioS Overview

In order for the SP250Ψ NPU to be most effective in long duration assessments (where agent barriers are most likely to destabilize) the device must be furnished with a compatible Biological Serial IC. The BioS contains aspects of Impression (AoI) as well as Connectomic Artifacts (CArta) which allow the BioS Interface to mitigate boundary degradation in "Golden Sunflower" cores.

3.2 BioS Versioning

To order or obtain in[illegible]r to the factory or the listed sales office:

PartN[illegible]
Device, XX = NPU Series, YY = Carrier Configuration Version

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Available Devices

SP14BIOS =1024K Bit 1.4V Biological Serial IC
SP14BIOST =1024K Bit 1.4V Biological Serial IC (Tape and Reel)

SP25BIOS =1024K Bit 2.5V Biological Serial IC
SP25BIOST =1024K Bit 2.5V Biological Serial IC (Tape and Reel)

SP33BIOS =1024K Bit 3.3V Biological Serial IC
SP33BIOST =1024K Bit 3.3V Biological Serial IC (Tape and Reel)

Neuromorphic Processing Unit Series

For the 1 [One] series the release starts at 01
For the Γ [Gamma] series the release starts at 10
For the Ψ [Psi] series the release starts at 00
For the Д [Delta] series the release starts at 11

Carrier Configuration Version

There are 4 configurations of imprint carrier. The Biological Serial ID must be tailored to a specific imprint carrier version. An incorrect matching of Biological Serial with imprint carrier will result in unknown results and may damage or destroy a Biological Serial ID.

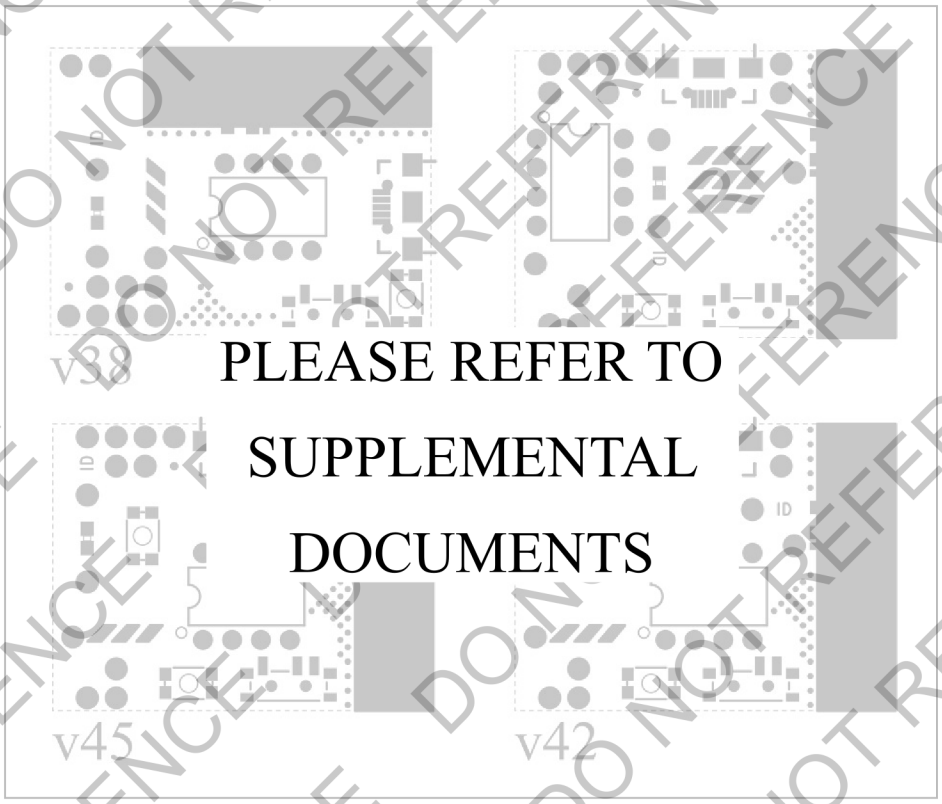

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Fig.3a Carrier Configurations by Version Number

Examples:

a) **SP33BIOS-0138-ND:** Biological Serial IC for 3.3V One carrier with hardware configuration version 38.

b) **SP14BIOS-0045-ND:** Biological Serial IC for 1.4V Psi carrier with hardware configuration version 45.

c) **SP25BIOST-1042-ND:** Biological Serial IC for 2.5V Gamma carrier with hardware configuration version 42 on Tape and Reel.

d) **SP14BIOS-1142-ND:** Biological Serial IC for 1.4V Delta carrier with hardware configuration version 42.

4. Boot Procedure

4.1 Bootloader

When power is applied to the SP250Ψ, the unit will search for a bootable volume in NVM and mount it to DRAM. If no bootable volume is present, or if the memory location of the boot volume doesn't match that of the last successful boot, a utility to reset the memory location of the boot volume is available on the debug menu while the device is in CDC mode.

4.2 Memory Table

The portion of non-volatile memory dedicated to filesystem and boot operations will have the following structure:

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0x0000	RESERVED BEGIN
0x00AA	RESERVED END
0x00AB	BACKUP BUFFER
0x12CF	BACKUP BUFFER
0x12D0	IDENTITY PRIMERS BEGIN
0x14A1	IDENTITY PRIMERS END
0x14A2	BOOT SECTOR BEGIN
0x14FF	BOOT SECTOR END
0x1500	IMPRINT PRIMITIVES BEGIN
0x2000	IMPRINT PRIMITIVES END
0x2001	RESERVED BEGIN
0x[redacted]	RESERVED END

4.3 Carrier Subsystem

The carrier subsystem consists of the boot sector, imprint primitives and reserved memory blocks as well as the "Golden Sunflower" block, wFIFO block and portions of the GPIO controller. This system carries out learning functions based on initial data from the BioS and Connectomic Record. Because the Carrier Subsystem encompasses the boot sector it is possible for those addresses to be spontaneously rewritten. In the event of a boot sector rewrite the CDC debug menu can be used to set the boot location to an external table.

5. VORTEXs System

5.1 System Overview

Voltage Oscillation Reporting To EXternal Systems (VORTEXs) is a subsystem of the SP250Ψ which allows engineers and field technicians to retrieve error codes from other SP250Ψ subsystems without specialized training or equipment. Error codes generated by the VORTEXs system are numerical codes represented by voltage fluctuations on a dedicated test point. Error codes and their corresponding definitions can be found in a table at the end of this section. Because the VORTEXs system is integrated with the SP250Ψ flow control block, the carrier subsystem can not directly access error codes generated from VORTEXs. Please take this into account when desi

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5.2 Reading an Error Code

Error codes are repo n the dedicated VORTEXs test point, referenced to GN the appropriate DC voltage scale is all that is required to retrieve an error code. With the ground probe contacting any of the SP250Ψ GND pins probe the VORTEXs test point and observe the reported voltage. If an error code is present the voltage will vary to represent the error code. Because VORTEXs reports will vary with system voltage it is suggested to round each reported voltage either up or down to the nearest whole integer.

NOTE FOR SPARKX CARRIER BOARDS

As of carrier configuration v40, the position of the VORTEXs test point has been fixed beside the micro-b connector and can be identified by its smaller drill diameter in comparison to the rest of the GPIO header.

5.3 Code Reference Table

The following are common error codes generated by the VORTEXs system. For a comprehensive list, please refer to index [redacted] of the document titled [redacted]

1:	1 2 3 4 -		25:	0 2 3 4 -			
2:	1 2 4 3 -		26:	0 2 4 3 -			
3:	1 3 2 4 -		27:	0 3 2 4 -			
4:	1 4 2 3 -		28:	0 4 2 3 -			
5:	1 3 4 2 -		29:	0 3 4 2 -			
6:	1 4 3 2 -		30:	0 4 3 2 -			
7:	2 1 3 4 -		31:	0 1 3 4 -			
8:	2 1 4 3 -						
9:	3 1 2 4 -						
10:	4 1 2 3 -						
11:	3 1 4 2 -						
12:	4 1 3 2 -						
13:	2 3 1 4 -						
14:	2 4 1 3 -						
15:	3 2 1 4 -		39:	0 2 1 4 -			
16:	4 2 1 3 -		40:	0 2 1 3 -			
17:	3 4 1 2 -		41:	0 4 1 2 -			
18:	4 3 1 2 -		42:	0 3 1 2 -			
19:	2 3 4 1 -		43:	0 3 4 1 -			
20:	2 4 3 1 -		44:	0 4 3 1 -			
21:	3 2 4 1 -		45:	0 2 4 1 -			
22:	4 2 3 1 -		46:	0 2 3 1 -			
23:	3 4 2 1 -		47:	0 4 2 1 -			
24:	4 3 2 1		48:	0 3 2 1			

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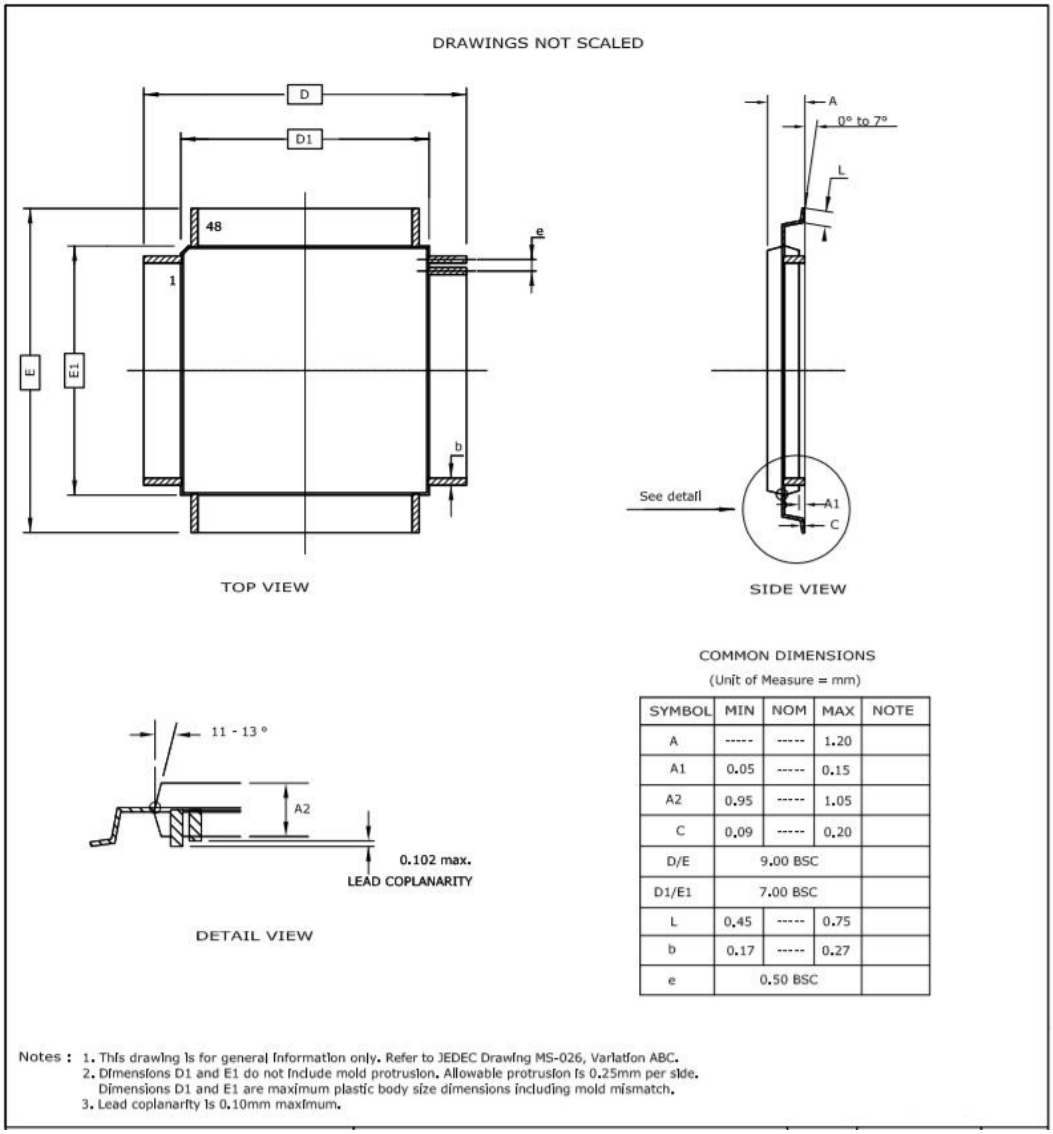
6. Mechanicals

6.1 Package



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.05	-----	0.15	
A2	0.95	-----	1.05	
C	0.09	-----	0.20	
D/E	9.00 BSC			
D1/E1	7.00 BSC			
L	0.45	-----	0.75	
b	0.17	-----	0.27	
e	0.50 BSC			

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

6.2 RF Considerations

The RF Engine integral to the SP250Ψ operates very efficiently with a properly matched F-Style PCB trace antenna. It is imperative to keep uncontrolled impedance traces as short as possible because they can be lossy and inductive. Long feed traces also increase the risk of mechanical failure interrupting RF transmission. The following is a reference antenna design which has shown satisfactory performance in tests with the SP250Ψ.

PLEASE REFER TO SUPPLEMENTAL DOCUMENTS

Fig.6a Trace Antenna Reference Design

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