

Eagle Layout Reference SparkFun Electronics Summer Semester

PCB LAYOUT SETTINGS:

0.05" Grid turned ON

0.02" Round Vias

0.01" Trace width

15% Ratio for Text

PCB SHORTCUTS:			
KEY	ICON	COMMAND	DESCRIPTION
F1	•	Show	Highlights the selected object and all similar.
Alt +F1	i	Info	Shows the attributes of an object.
Alt +F2	Q	Zoom to ft	Redraws the window to ft all of the objects in the layout.
F3	×	Delete	Deletes an object from the PCB
F4	R2 ION	Name	Allow the renaming of components or 'Nets' (Signal)
F5	#2 10k	Value	Used to set the value of a component
F6	EŽ.	Smash	Allows the component name and value to be repositioned independent of the component
F7	+	Move	Moves a component (Hint: Hold "Control" while moving to move a selected group)
Alt +F7		Group	Use this to select a group of objects
F8	×	Ratsnest	Finds all the 'airwires' in the design (unconnected signals!)
F9	٦	Route	Use this to create a 'wire' connecting different signals
Alt +F9	8	Ripup	Deletes a trace
F10	!!!	Set Small Grid	Changes the grid to 0.05"
Alt +F10	!!!	Set Metric Grid	Changes the grid to 1mm
F11	•	Change Layers 1	Shows the 'Routing' layers
Alt +F11	•	Change Layers 2	Shows the layers to create an assembly sheet
F12		Turn on polygons	When the ratsnest is processed, polygons will be included (often takes much longer, but required before the design can be finished)

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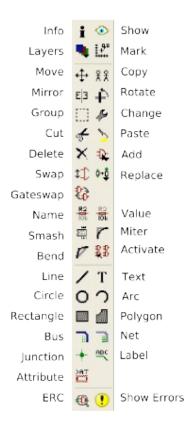


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on the board (false airwires will appear). Copy Copies a component (Like text or polygons). Cut Copies a group of components. Paste Paste Pastes a group of components that have been cut. Generate Gerbers Generates the design files for the PCB.			
Cut Copies a group of components. Paste Pastes a group of components that have been cut. Generate Gerbers Generates the design files for the PCB.	Alt +F12	Turn of polygons	Polygons not included in ratsnest. Faster, but won't connect signals to the signal planes on the board (false airwires will appear).
Paste Pastes a group of components that have been cut. Generate Gerbers Generates the design files for the PCB. DBC Burs the Design Bule Check.		 条	Copies a component (Like text or polygons).
Generate Gerbers Generates the design files for the PCB. DBC Burs the Design Bule Check.		₹ Cut	Copies a group of components.
DRC Burs the Design Bule Check		Paste	Pastes a group of components that have been cut.
DRC Runs the Design Rule Check		Generate Gerbers	Generates the design f les for the PCB.
€		⊕ DRC	Runs the Design Rule Check.
Text Adds text to the PCB		Text	Adds text to the PCB
Adds a Via to the board (can be used to transfer a route from the top layer to the botto layer).		Via	Adds a Via to the board (can be used to transfer a route from the top layer to the bottom layer).
Alt + Backspace Undo	Alt +Backspace	Undo	

SCHEMATIC TOOLBAR



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TIPS AND TRICKS

Try placing all components on a 0.1" grid

For signals use at least a .008" (8mil) trace width

For power traces use at least .01" (10mil) trace width, but if there's room to make it bigger then do so.

LABEL, LABEL. Label switches (and their states), LEDs, buttons, and headers. Use the silkscreen to designate the purpose of these items.

If a label interferes with a via, either move the via or make sure that the via will be tented.

Put a Date Code on the back of the board. This will help when you've got multiple versions of the same board.

Create Ground Pours on the top and bottom layer

Change the Isolation of the Ground Pour to 12 mil. This prevents manufacturing errors

Group components on the PCB according to how they are grouped in the schematic.

Keep at least 8mil between traces

Only use 45 degree angles on the traces. Never put a 90 degree angle on a trace.

Traces on the same layer (same color) must not intersect unless they are the same signal!

Route traces from the middle of the pad.

While routing a trace, press the middle mouse button to insert a via and transfer the route from one layer to the other.

Use the 'Ratsnest' to find out if there are airwires (unconnected signals).

If you can't find the airwires, open the 'layers' window and click 'none' to turn off all of the layers. Then find the 'Unrouted' layer in the window and turn that layer on. This will show you where the airwires are. After you find them, press F11 to turn all of the layers back on.

When a board is first created there are 16 layers; typically only 2 layers are used on a board. To get rid of the extra layers (a very annoying bug in Eagle):

- 1. Open the DRC
- 2. Go to the 'Layers' tab
- 3. In the 'Setup' text box erase the parenthesis around 1*16.
- 4. Press 'Check'.
- 5. Open the DRC again.
- 6. Put the parenthesis back around 1*16 in the Setup box of the lavers tab.
- 7. Press check again

Hold the 'Alt' key while routing a trace to place the route on a fine grid. (This also works while moving components, but the components should stay on the major grid when possible).

Use the DRC to check the board for design errors.

ALWAYS ALWAYS print a 1:1 copy of the layout and make sure that the parts ft the way they should.





