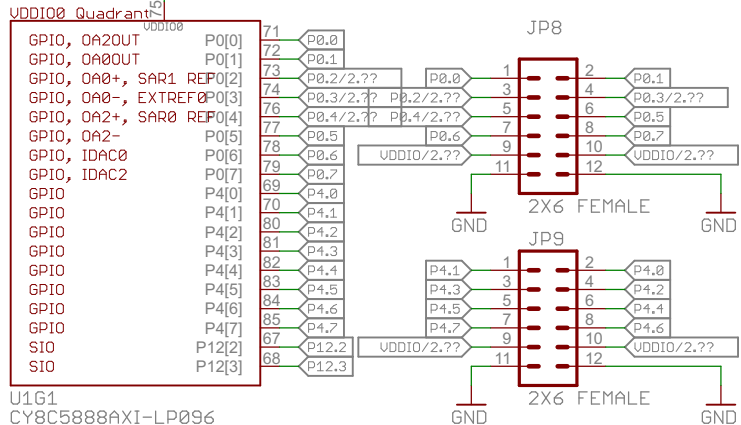
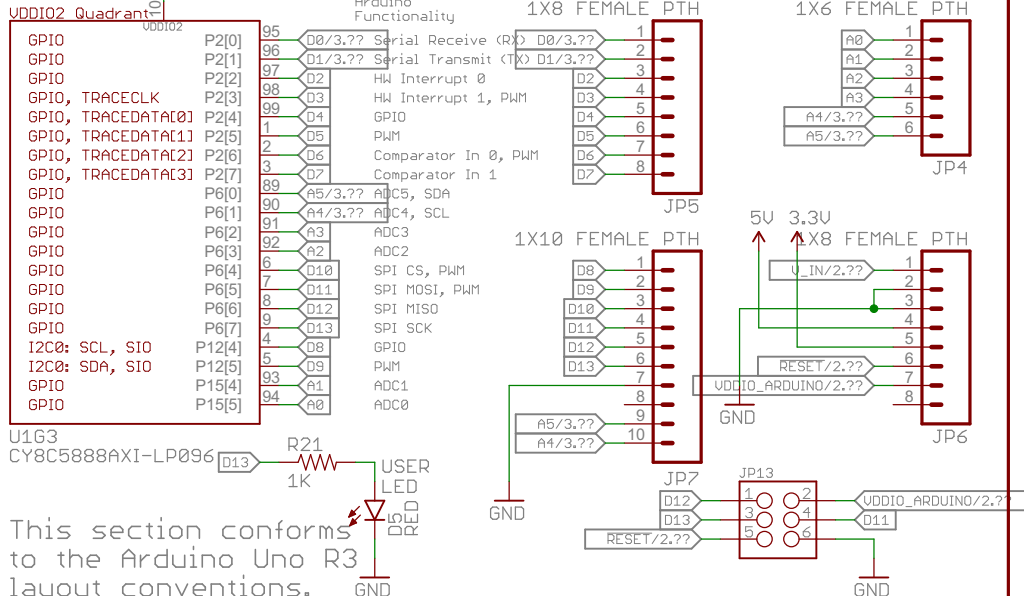


Quadrant 0



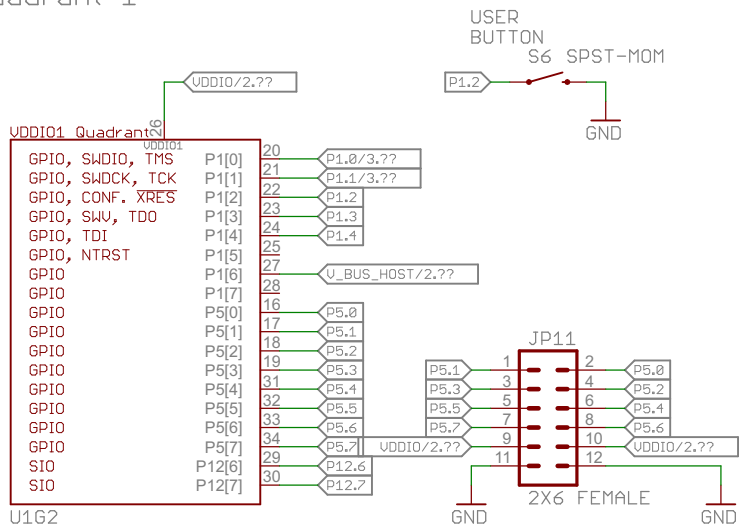
U1G1  
CY8C5888AXI-LP096

Quadrant 2



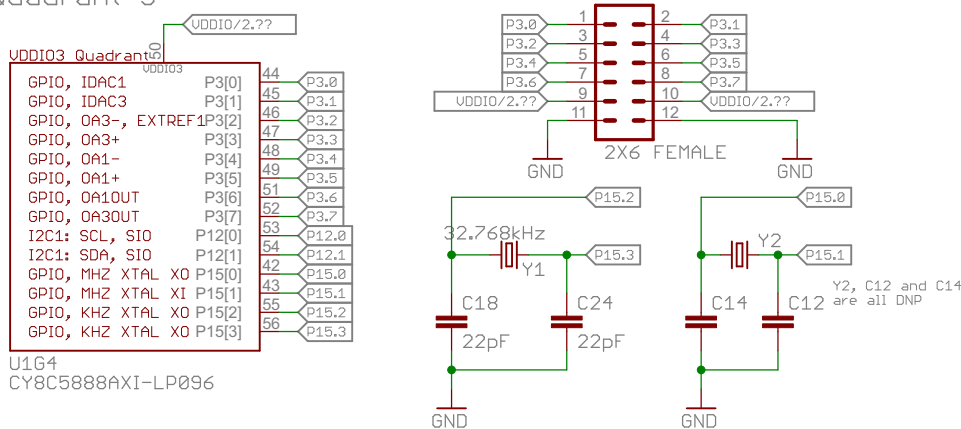
U1G3  
CY8C5888AXI-LP096

Quadrant 1



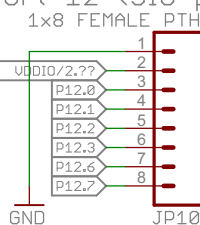
U1G2  
CY8C5888AXI-LP096

Quadrant 3



U1G4  
CY8C5888AXI-LP096

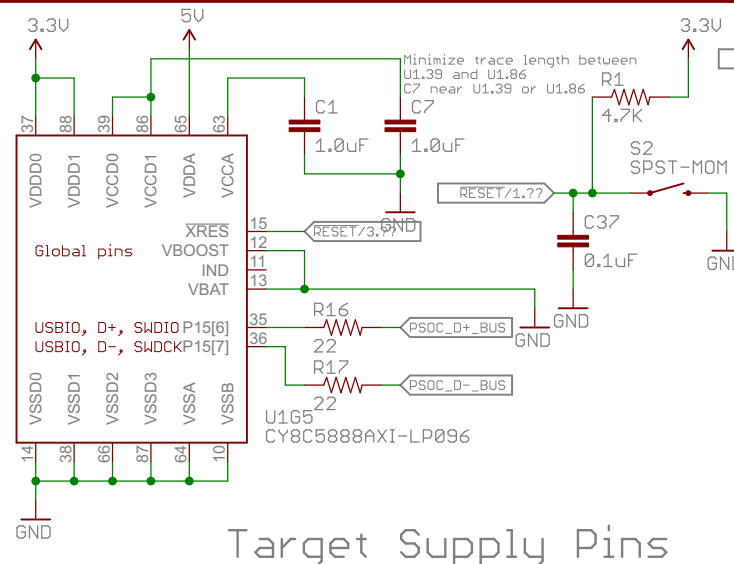
Port 12 (SIO pins)



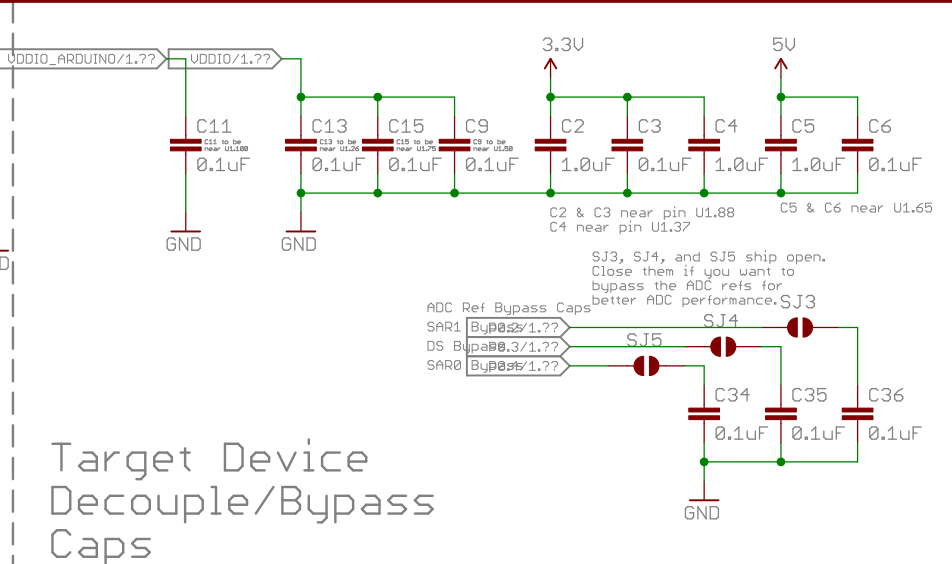
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Design by: Mike Hord	REV: 11
Date: 9/16/2015 10:27:24 AM	Sheet: 1/3

Developed with help from Jon Moeller and Cypress Semiconductor

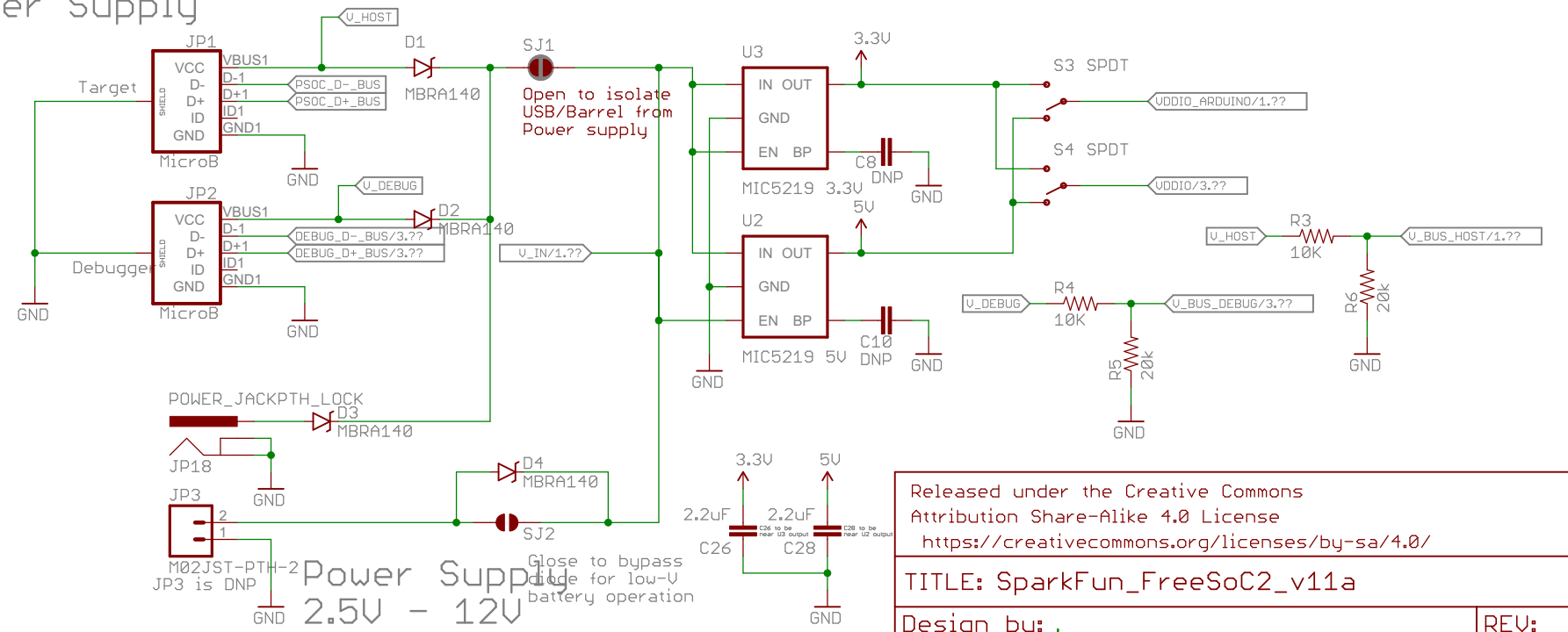


Target Supply Pins



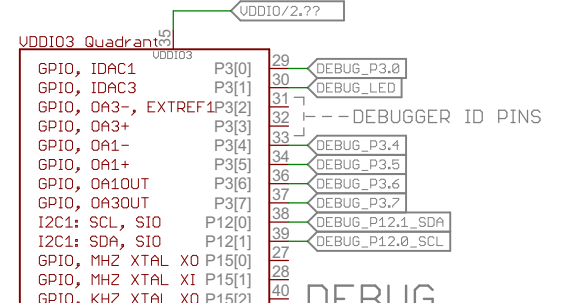
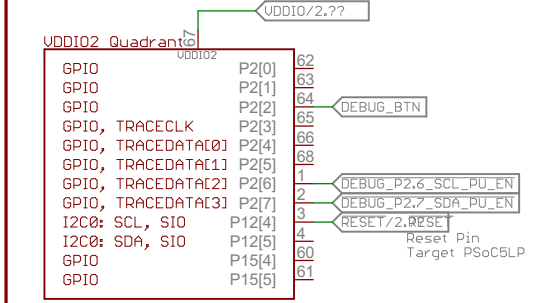
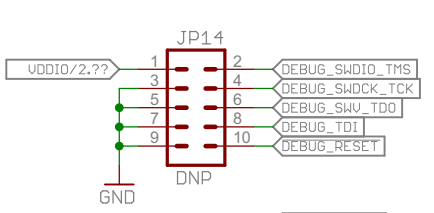
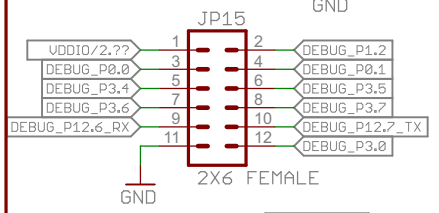
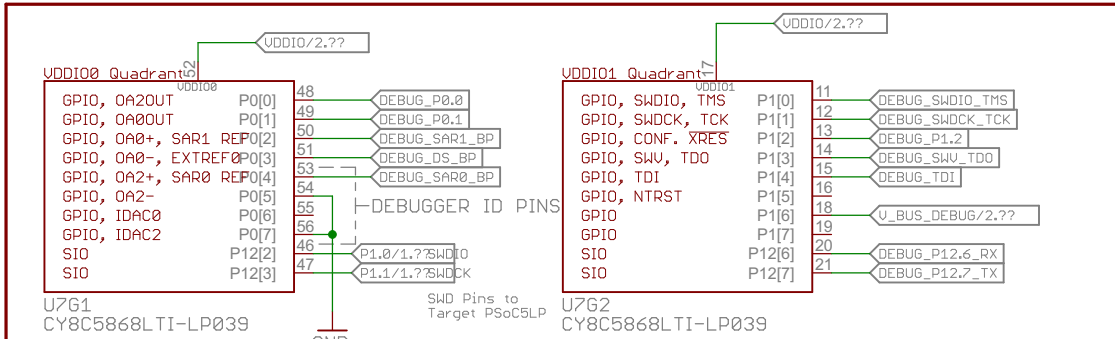
Target Device Decouple/Bypass Caps

Power Supply

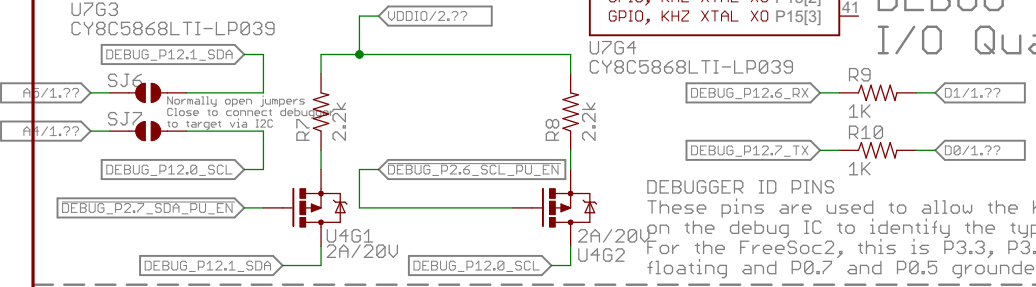


Power Supply 2.5V - 12V

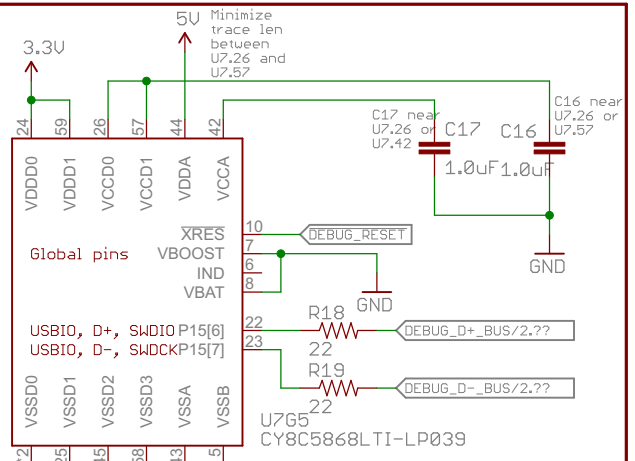
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TITLE: SparkFun_FreeSoC2_v11a	
Design by: <b>Mike Hord</b>	REV: <b>11</b>
Date: 9/16/2015 10:27:24 AM	Sheet: 2/3



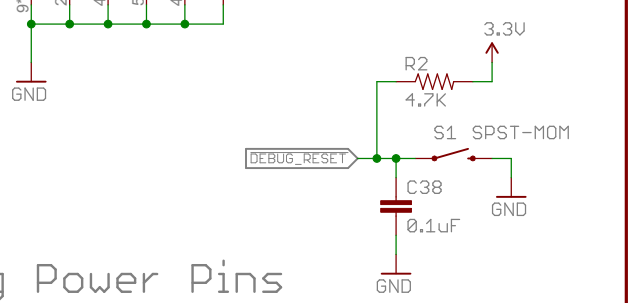
### DEBUG I/O Quadrants



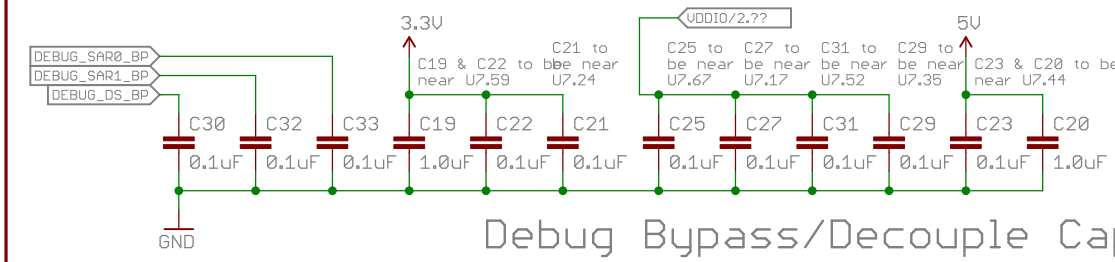
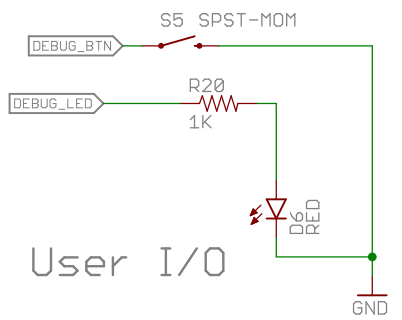
**DEBUGGER ID PINS**  
 These pins are used to allow the KitProg firmware on the debug IC to identify the type of kit.  
 For the FreeSoc2, this is P3.3, P3.2, P0.6 and P0.4 left floating and P0.7 and P0.5 grounded.



### Debug Power Pins



### Debug User I/O



### Debug Bypass/Decouple Caps

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Design by: **Mike Hord**

REV: **11**