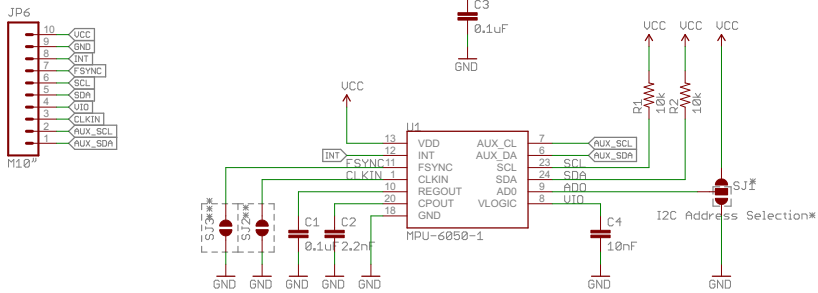


Changes to U11
 SCL and SDA were switched on U10, fixed on U11
 Broke out VLOGIC line
 C2 was mislabeled as 10nF, should have been 2.2nF.
 Added selectable jumpers to CLK, FSYNC and AD0
 Minor layout changes
 Played around with IC footprint.
 Added 4 small tcream squares to middle pad.
 Rounded and elongated pads.

BOM changes
 YES
 C2 is now 2.2nF instead of 10nF

New Stencil
 YES

Changes to U12:



* Two MPU-60X0s can be connected to the same I2C bus
 The LSB bit of the 7 bit address is determined by the logic level on pin AD0.
 Default Address = 0x68 (pin AD0 is logic low)
 Alternative Address = 0x69 (pin AD0 is logic high)

** Optional external reference clock input. Connected to GND by default.
 Cut trace for external clock

*** Frame synchronization digital input. Connected to GND by default
 Cut trace for external sync



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TITLE: Triple_Axis_Accelerometer-Gyro_Breakout_-_MPU-6050_v12

Design By: J. Bartlett

Revision By: E. Orosel

REV:

v12

Date: 7/23/2013 2:47:34 PM

Sheet: 1/1