bladerRF - USB 3.0 Software Defined Radio

![Diagram of bladerRF - USB 3.0 Software Defined Radio with various components and connections, including DAC, GPIF 2, USB3, SPI FLASH, and power supply information (1.2V SMPS max 3A 90% eff, 3.58V SMPS max 1.3A 95% eff, 3.3V Analog 280mA/500mA Linear LDO for LMS TX, 3.3V Analog 220mA/500mA Linear LDO for LMS RX, 3.3V Digital 106mA/200mA Linear LDO for LMS RX/TX, 2.5V Analog 30mA/100mA Linear LDO VCO/PLLs, 1.8V Analog 100mA/200mA Linear LDO for LMS, 1.8V Digital 190mA/400mA Linear LDO for signalling).]
MSEL[3..0] pins should be connected directly to VCCA or GND.

MSEL[3..0] = PS-FAST = "1100" @ 3.3/3.0/2.5V
MSEL[3..0] = PS-STD = "0000" @ 3.3/3.0/2.5V
MSEL[3..0] = FPP-FAST = "1110" @ 3.3/3.0/2.5V
MSEL[3..0] = FPP-FAST = "1111" @ 1.8/1.5V (default)

MSEL pins should be connected directly to VCCA or GND.
FPGA "RIGHT" BANK

LMS_SIGNALS GO TO THE "RIGHT" OF THE C4 BANKS 4, 5, 6, 7

Avoid VREF pins due to their slow IO times.
This power condition is for the 115KE part at 3A.
In 32-bit GPIF mode UART is (FX3 data pg 33):
- GPIO[55](C2)=UART_TX
- GPIO[56](D5)=UART_RX

UART_CS was added to allow the FPGA to use the MISO/MOSI lines to communicate via UART with the FX3.

US can also be deasserted to write to flash after boot.
FX3 DEBUG + CLOCK SEL

DEBUG TPs

TCK  TDO  TMS  TRST_N
FSLC[2..0]

FX3 JTAG

JTAG ICE_CONN

FX3 DEBUG + CLOCK SEL

.Debug LED

FSLC2  FSLC1  FSLC0

FSLC[2..0]

FX3 datasheet pg 8:
38.4MHz input CLK - FSLC[2:0] = "110"

FSLC2  FSLC1  FSLC0

30kΩ pullup clk = FSLC[2:0] = "110"

FPGA Version Resistor

R3 10K

VT_REF 1
N_TRST 3
N_SRST 5
DBGQ 7
DBGACK 9

V_SUPPLY 2
GND1 4
GND2 6
GND3 8
GND4 10
GND5 12
GND6 14
GND7 16
GND8 18
GND9 20

C232 0.01uF
USB CONNECTIONS

USB3.0 MICRO TYPE B

USB Positive Overvoltage Protection Controller

ESD DEVICE

PART_NUMBER = SP3010-04UTG
Manufacturer = Littlefuse
These caps have to be close to their respective Vref pins.
**POWER DISTRIBUTION**

The idea is to drop to 1.2V and 3.58V with SMPS. Then drop to 3.3, 2.5, 1.8 from the 3.58V SMPS.

**1.2V**  
(min:200mA, typ:800mA) / 3100mA / 90% eff

**Analog 3.3V**  
280mA / 500mA

**Digital 3.3V**  
220mA / 500mA

**Analog 3.58V**  
~800mA / 1300mA / 95% eff

**Digital 3.58V**  
106mA / 200mA

**Analog 1.8V**  
~100mA / 200mA  
Ceramic caps will suffice

**Digital 1.8V**  
190mA / 400mA

**Analog 2.5V**  
30mA / 100mA

**Power Distribution Diagram**

- **3.58V** (~800mA / 1300mA / 95% eff)
- **1.2V** (min:200mA, typ:800mA) / 3100mA / 90% eff
- **Analog 3.3V** 280mA / 500mA
- **Digital 3.3V** 220mA / 500mA
- **Analog 1.8V** ~100mA / 200mA
- **Digital 1.8V** 190mA / 400mA

**Notes:**

- Analog 3.3V
- Digital 3.3V
- Analog 1.8V
- Digital 1.8V

**Components:**

- Resistors: R300, R301, R302, R303, R304, R305, R280, R281, R282, R283, R284, R285
- Inductors: L49, L45, L45
- Other Components: U48, U53, U54, U55, U56

**Key:**

- **Vcc:** Power Supply
- **Gnd:** Ground
- **Vin:** Input
- **Out:** Output
- **Fb:** Feedback
- **Avin:** Analog Input
- **Pgood:** Power Good
Jumpered power selection
DC barrel vs USB3 bus

Scatter these testpoints throughout the design.
Testpoints will be PTH

C121 100uF_10V
C122 100uF_10V
C123 330uF_10V
C124 330uF_10V

PART_NUMBER = RAPC712X
Manufacturer = Switchcraft Inc.

J70 PWR_HDR6

TP23
TP24